DESIGN EVOLUTION OF DUAL-MATERIAL GATE STRUCTURE IN CYLINDRICAL SURROUNDING DOUBLE-GATE (CSDG) MOSFET USING PHYSICS-BASED ANALYTICAL MODELING

Thesis submitted for the fulfillment of requirements for the degree of

DOCTOR OF PHILOSOPHY

in

Electronic Engineering

by

ABHA DARGAR

UNIVERSITY OF
KWAZULU-NATAL

INYUVESI
YAKWAZULU-NATALI

HOWARD COLLEGE,
COLLEGE OF AGRICULTURE, ENGINEERING AND SCIENCE
UNIVERSITY OF KWAZULU-NATAL, DURBAN - 4041
SOUTH AFRICA.

STUDENT NO.: 218087138

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Student:

Abha Dargar

Supervisor:

Prof. (Dr.) Viranjay M. Srivastava

This thesis submitted in fulfillment of the requirements

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University of KwaZulu-Natal, Durban

South Africa.

As the candidate's supervisor, I have approved this thesis for submission.

Signed…….. .. Date: 13 April 2021

Name: Prof. (Dr.) Viranjay M. Srivastava

DECLARATION 1 – PLAGIARISM

I, **ABHA DARGAR** with Student Number **218087138** with the thesis entitled **"DESIGN EVOLUTION OF DUAL-MATERIAL GATE STRUCTURE IN CYLINDRICAL SURROUNDING DOUBLE-GATE MOSFET USING PHYSICS-BASED ANALYTICAL MODELING"**
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DETAILS OF CONTRIBUTION TO PUBLICATIONS that form part and/or include research presented in this thesis (include publications that have been submitted, *in the press* and published and give details of the contributions of each author to the experimental work and writing of each publication).

JOURNAL PUBLICATIONS

1. **Abha Dargar** and Viranjay M. Srivastava, "Thickness Modeling of Short-Channel Cylindrical Surrounding Double-Gate MOSFET at Strong Inversion using Depletion Depth Analysis," *Micro and Nanosystems*, vol. 13, no. 3, pp. 319-325, 2021. **(Included in Chapter 6).** ***[DoHET, Scopus]***

2. **Abha Dargar** and Viranjay M. Srivastava, "Analytical Modeling of Dual-Material Gate Structure in Cylindrical Surrounding Double-Gate MOSFET," *Journal of Computational Electronics*, under review, March 2021 (**Included in Chapter 7**). ***[DoHET, Scopus]***

3. **Abha Dargar** and Viranjay M. Srivastava, "Performance Comparison of Gate-Metal Engineered Cylindrical Surrounding Double-gate MOSFET," *International Journal of Electronics and Telecommunication*, vol. 67, no. 1, pp. 29-34, January 2021. (**Included in Chapter 7**). ***[DoHET, Scopus]***

4. **Abha Dargar** and Viranjay M. Srivastava, "Cylindrical Surrounding Double-Gate MOSFET and Orientation of Dual-Material Gate- a Review," *Journal of Engineering Science and Technology Review*, under review, Feb. 2021 (**Included in Chapter 2 and Chapter 8**). ***[DoHET, Scopus]***

CONFERENCES PUBLICATIONS

5. **Abha Dargar** and Viranjay M. Srivastava, "Capacitive Model of CSDG MOSFET at Pinch-off for Switching Characteristics," *IEEE 10th International Conference on Computing, Communication and Networking Technologies (ICCNT-2019)*, Kanpur, India, 6-8 July 2019, pp. 1-4. **(Included in Chapter 3). [IEEE]**

6. **Abha Dargar** and Viranjay M. Srivastava, "Analysis of Electrical Field in Uniformly Doped Cylindrical Surrounding Double-Gate MOSFET," *IEEE 10th International Conference on Computing, Communication and Networking Technologies (ICCNT-2019),* Kanpur, India, 6-8 July 2019, pp. 1-4. **(Included in Chapter 4). [IEEE]**

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9. **Abha Dargar,** Shashi K. Dargar, and Viranjay M. Srivastava, "Effect of Gate-Underlap Lengths in High-k Dielectric Based Silicon-Nanowire Gate-All-Around TFET," *7th International Mathematics-Engineering-Science and Health Sciences Congress*, Rome, Italy, pp. 18-21, 14-16 June 2019. (**Included in Chapter 5)**

10. **Abha Dargar,** Shashi K. Dargar, and Viranjay M. Srivastava, "Comparative Analysis of Single and Double-Gate Amorphous-IGZO Thin-Film Transistors," *7th International Mathematics-Engineering-Science and Health Sciences Congress*, Rome, Italy, pp. 5-10, 14-16 June 2019.

PREFACE

The research work in this thesis was implemented by Abha Dargar, under the supervision of Prof. (Dr.) Viranjay M. Srivastava at the Discipline of Electrical, Electronic and Computer Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa.

The content of research outcome included in chapter 3 to chapter 6 of this thesis have been published in the form of a research article in the Journals including Micro and Nano Systems, full-text proceeding in IEEE Xplore digital library, and the remaining in chapter 7 have been submitted to the consideration of publication.

This thesis's content in chapters 3 and 4 have been presented in the 10th International Conference on Computing, Communication, and Networking Technologies (ICCNT-2019), held in India.

This thesis's content in chapter 5 has been presented in the 7th International Mathematics-Engineering-Science and Health Sciences Congress (IMES-HSC 2019) held in Italy.

This thesis's partial content of chapter 7 has been presented in the symposium titled Postgraduate Research and Innovation Symposium (PRIS- 2019) held in the University of KwaZulu-Natal, South Africa.

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I bow my head in all my humility for the blessings of my parents Dr. Om Prakash Nyati and Mrs. Manju Nyati, my loving in-law's parents, Mr. Mahaveer Prasad Dargar and Mrs. Basanti Devi Dargar, who stood as a source of light, always inspiring me to achieve. I shall forever remain indebted for their unconditional love and blessing, which they always shower on me.

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ABHA DARGAR

218087138

ABSTRACT

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the fundamental component in present Micro and Nano-electronics device applications, such as switching, memory devices, communication devices, etc. MOSFET's dimension has shrunk down following Moore's law to attain high-speed operation and packing density integration. The scaling of conventional MOSFET has been the most prominent technological challenge in the past few years because the decreasing device dimensions increase the charge sharing from the source to the drain and that in turn give rises to the reduced gate-control over the channel, hot carrier induced degradation, and other SCEs. These undesired effects devaluate the device performance that compels optimum device design analysis for particular operating conditions.

Therefore, several innovative device design/architectures, including Double-gate, FinFET, Surrounding gate MOSFET, etc., have been developed to mitigate device scaling challenges. Comprehensive research can be traced long for one such promising gate-all-around MOSFET, i.e., Cylindrical Surrounding Double-Gate (CSDG) MOSFET centrally hollow concentric structure, provides an additional internal control gate that improves the device electrical performance and offers easy accessibility. There have been several developments in terms of improvements, and applications of CSDG MOSFET have been practiced since after its evolution.

This thesis's work has been targeted to incorporate the gate material engineering in the CSDG structure after appropriate analysis of device physics-based modeling. In particular to the proposed structure, the electric field, pinch off capacitance, and after that thickness of the device parameters' dependence have been mathematically derived from attaining the objective. Finally, a model based on a dual-material gate in CSDG MOSFET has been proposed. The electrical field in CSDG MOSFET has been analyzed in detail using a mathematical derivation of device physics, including the Surface-Potential, threshold voltage, and the gate-oxide capacitances of the internal and external part of the device. Further, the gate-oxide capacitance of CSDG MOSFET, particularly to the device pinch-off condition, has been derived. Since the device operation and analysis at the shorter channel are not similar to conventional long-channel MOSFETs, the depletion-width variation has been studied.

The identified notion has been applied to derive the approximate numerical solution and silicon thickness inducing parameters for CSDG MOSFET to deploy the improvements in the device performance and novel design modifications. As the gate-material and gate-stack engineering is an alternative to overcome the device performance degradation by enhancing the charge transport efficiency, the CSDG MOSFET in a novel Dual-Metal Gate (DMG) structure design has been proposed and analyzed using the solution of 2D Poisson's equations in the geometrical boundary conditions of the device. The model expressions obtained solution using the proposed structure has been compared with a single metal gate structure.

Finally, it has been analyzed that the proposed model exhibits an excellent match with the analytical model. The obtained DMG device structure advances the carrier velocity and transport efficiency, resulting in the surface-potential profile caused by dissimilar gate metal work-function. The superior device characteristics obtained employing a dual-material structure in CSDG are promising and can reduce the threshold voltage roll-off, suppress the hot-carrier effects and SCEs.

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Fermi level potential	ϕ_{f}
Intrinsic carrier concentration of silicon	n_{i}
Bandgap energy	E_g
Boltzmann's constant	K_T
Built-in potential	V_{bi}
Carrier drift velocity	v_d
Channel flat-band voltage	$V_{fb,\mathrm{int}}$
Gate-length	L
Channel thickness	d_c
Depletion layer thickness under drain	W_{dD}
Depletion layer thickness under source	W_{dS}
Depletion thickness under the gate terminal	$\mathrm{d_{dG}}$
Drain to Source voltage	V_{DS}
Effective channel length	L_{eff}
Electron affinity	X
Electric filed	E
Electron charge	Q
Free space permittivity	ε_0
Gate-capacitance	C_G
Gate-oxide voltage	V_{ox}
Gate to Source voltage	V_{GS}
Gate-metal work-function	ϕ_m
Junction depth	X_j
Mobility	M
Optimum thickness of semiconductor	t_{smin}
Oxide Capacitance	C_{ox}
Over-drive voltage	V_{ov}
Permittivity of Silicon	ε_{si}
Planar depth	W_p

Relative permittivity	ε_ρ
Semiconductor thickness	t_{si}
Substrate doping concentration	N_{sub}
Surface concentration	N_s
Surface-Potential	ϕ_σ
Temperature independent pre-exponent	D_o
Thickness of Gate-oxide Materials	t_{ox}
Threshold voltage shift	ΔV_{TH}
Transconductance	g_m
Transit time	τ_r
Transit frequency	f_T
Uniform Charge Density	ρ_l

List of Abbreviations

Buried Oxide	BOX
Boltzmann Transport Equation	BTE
Cylindrical Gate All-Around	CGAA
Channel Length Modulation	CLM
Complementary Metal Oxide Semiconductor	CMOS
Cylindrical Surrounding Double-Gate	CSDG
Cylindrical Surrounding Gate	CSG
Double-gate	DG
Drain Induced Barrier Lowering	DIBL
Dual-metal CSDG	DM CSDG
Dual-metal Gate	DMG
Dual-material Surrounding Gate	DMSG
Fin Field Effect Transistor	FinFET
Gate-All-Around	GAA
Gradual Channel Approximation	GCA
Gate Induced Drain Leakage	GIDL
Gate Induced Source Leakage	GISL
Hot Carrier Injection	HCI
Integrated Circuit	IC
Metal Oxide Semiconductor Field Effect Transistor	MOSFET
Quantum Confinement Effect	QCE
Radio Frequency	RF
Short-Channel Effect	SCE
Single-Metal Gate	SMG
Semiconductor on Insulator	SEMOI
Surrounding Gate	SG
Silicon on Insulator	SOI
Technology Computer-Aided Design	TCAD
Ultrathin Channel	UTC
Very Large Scale Integrated	VLSI

Chapter-1

INTRODUCTION

In electronics, the miniaturization of devices and components has been the most significant invention. The semiconductor technology has played a substantial role in the consistent progression of Very Large Scale Integrated (VLSI) devices. Thus far, the current microelectronics engineering has been facing a continuous challenge of increasing system complexity and speed. Over the last 30 years, the most prominent technology element, i.e., transistor, has reduced in size from the micron to submicron and now in a nanometre scales. Such technological advancements have directed the craving for several improvements in the transistor's performance parameters to decrease operating voltage, increase speed, and realize higher packaging densities.

The Complementary Metal-Oxide Semiconductor (CMOS) transistor is a vital device in digital circuits that is the most promising element of an Integrated Circuit (IC) for being a switching component to produce digital logic representation. This chapter provides an introduction starting with the MOSFET as a device with a brief background, challenges associated with the scaling, the evolution of the CSDG MOSFET structure that lays the foundation of the research problem addressed in this thesis.

1.1. MOSFET Overview

The Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) is the heart of the integrated circuit, is generally used to switch and amplify electronic signals. A MOSFET is an electronic component with a 4-terminal device, namely Source (S), Drain (D), Gate (G), and Body (B) terminals as shown in Fig. 1.1. The body terminal is generally connected internally to the source segment, making it effectually a three-terminal device [1].

In current scenarios, the MOSFET has been the most popular device in the application that has replaced almost all traditional bipolar junction transistors both in analog and digital circuitries. In a MOSFET, the channel's conductivity is developed due to carrier inversion by the augmented oxide field at increasing gate voltages. The forming channel contains electrons or holes, depending on the type of substrate used. They are known as n-type if the substrate is p-type and similarly p-type if it is an n-doped semiconductor.

1.2. Operation Mechanism of a MOSFET

Depending on the mode of operation, the MOSFET is of two types: enhancement and depletion. In an enhancement mode, a potential caused by the field-effect drops across the gate insulator produces the channel conduction through the source and drain contacts. The depletion-mode MOSFETS are in which the channel comprises of carriers at the surface of opposite type to the substrate, and channel conduction destroys with the applied field that diminishes the carriers from the surface layer [2].

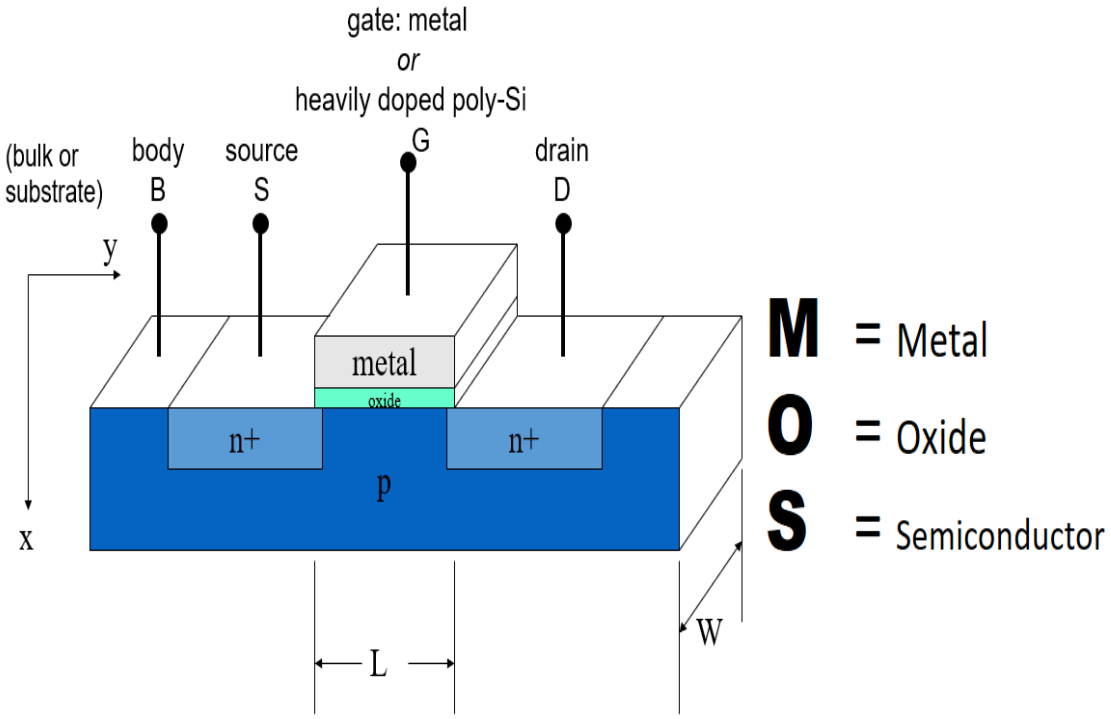


Fig. 1.1. Structure of a conventional MOSFET [1].

The depletion-mode MOSFETs are rarely used over the enhancement type because of the uncontrolled conduction irrespective of the applied gate voltage. The metallic gates and the oxide material of a MOSFET have undergone several experiments over the years to improve the device's speed and operation.

1.2.1. Metal-Oxide-Semiconductor Structure

A Metal Oxide Semiconductor (MOS) structure is formed of a silicon dioxide (SiO_2) layer grown over a silicon substrate and metal or poly-Si layer deposition. The SiO_2

dielectric sandwiched between the metal and semiconductor construct a planar capacitor structure. The semiconductor charge sharing gets modified with the application of voltage to a MOS device. In a p-type form, a positive voltage at the gate builds a depletion region produced owing to the movement of holes away from the oxide-semiconductor boundary. Such occurrence results in an area of immovable charges due to negative acceptor ions.

When the gate voltage is increased adequately, the negative charge layer (inverted charge) exists adjacent to the interface oxide-semiconductor interface. In the MOSFET structure, the inversion layer helps in the fast movement of electrons from the source to drain; on the contrary, the MOS capacitor structure has quite a gradual movement due to thermally generated carrier recombination. Typically, the threshold voltage is the term which describes the amount of applied gate voltage to equalize the number of electrons in the inversion layer, same as the holes in the body of the MOSFET device and further increase of the gate voltage after the threshold voltage is identified as gate overdrive voltage.

1.2.2. MOSFET Structure and Channel Formation

The carrier modulation in a MOSFET takes place due to the existence of MOS capacitor structure between the semiconducting substrate and the gate electrode separated by an oxide insulator. The terminal from which the charge carriers (i.e., electrons for an n-channel MOSFET, or holes for a p-channel MOSFET) are originated to stream into the channel is known as the source end, on the contrary the terminal through which charge carriers are leaving out via the channel is known as the drain end.

The occupied energy bands in the semiconducting materials are well defined by their relative situation of the Fermi level. Fig. 1.2 shows channel formation in an n-channel MOSFET. The applied gate bias above the threshold voltage drift the holes present in the substrate away from the gate and results in the shifting of the valence band away from the predominant Fermi energy level [3].

If the gate bias continues to increase further, it results in carrying the conduction band nearer to the Fermi level, which inhabits the surface with more of the charges inversion layer and forms the channel of n-type. The conducting channel expands between the source and the drain through which progressive current conduction takes place. With the increase

of the gate voltage, the electron density populates in the inversion layer, which further results in the flowing current between the source and the drain. The channel is lightly populated if the gate voltage is below the threshold voltage and only a negligibly small subthreshold leakage current is attained.

The channel becomes p-type if the negative gate to source voltage is applied and operates similar to the n-type device except for opposite polarities of charges and voltages. At low negative gate bias with magnitude below the threshold value vanishes the p-channel, and a small leakage current can flow.

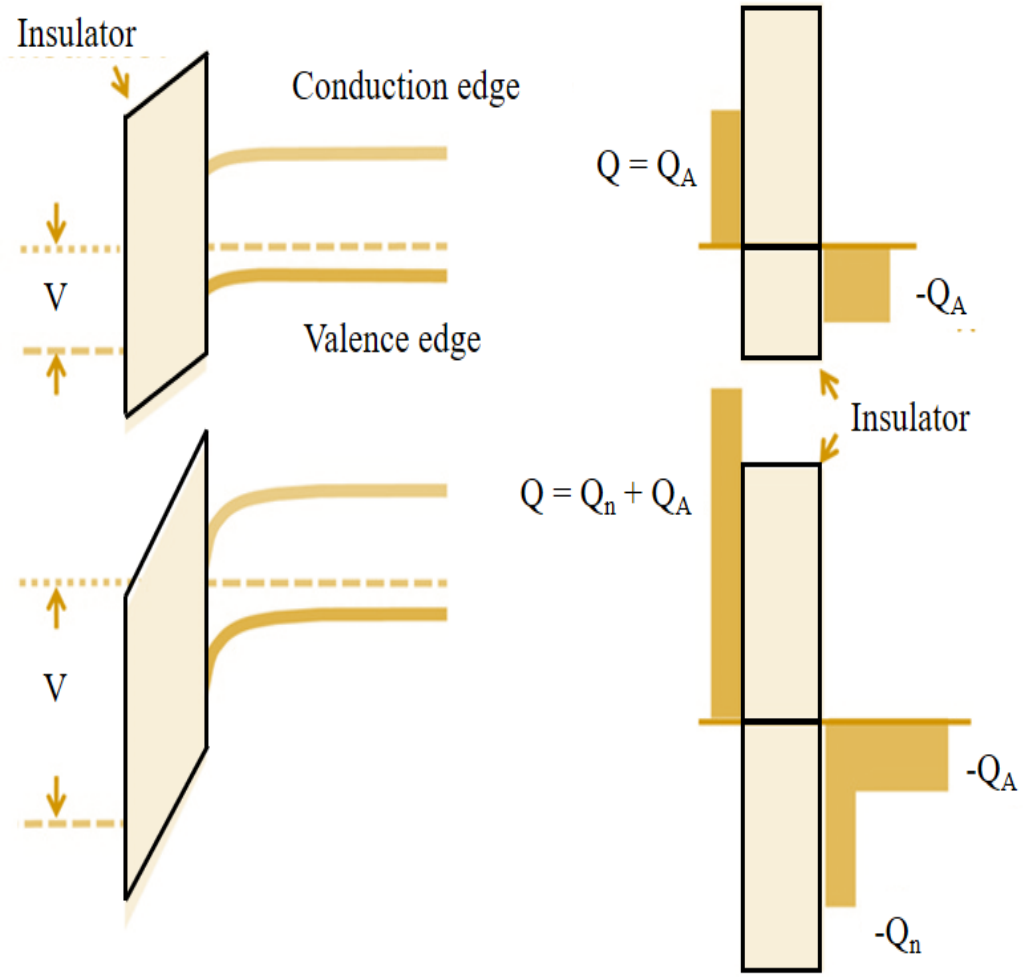


Fig. 1.2. Channel formation in n-channel MOSFET [3].

The MOSFET device can be made in a manner in which the semiconductor layer is over a buried-oxide (BOX) known as Silicon on Insulator (SOI) design. When the channel positioned in the middle of the BOX and gate insulator is precisely thin, then such arrangement of the device is known as an ultrathin channel (UTC). Alternatively, in another configuration, the device is made above a non-silicon semiconducting material layer is a semiconductor on insulator (SEMOI) device.

1.3. Scaling of Transistor

At reducing transistor size for attaining higher complexity of integration, the fabrication of the device becomes cumbersome. For example, the ICs turn out to be denser when the devices undergo downscaling, the lithographic process, interconnections, or processing steps of device manufacturing becomes challenging. Therefore, increased device performance, such as improved switching speed and reduced power consumption, are desirable while scaling down the device to a smaller size.

The device downscaling has captured significant attention in microelectronics device research, and the current progress of CMOS-based electronics has witnessed this in the last few decades. The density of transistors in a chip has been firstly predicted by the co-founder of Intel Inc. Gordon Moore, which is well-known as Moore's law [4]. His law has driven the industrial projection starting from 1975 for more than forty years with the assumption of number of transistors per chip getting double every year. It has been a successful era in the semiconductor industrial growth that the prediction reported well in advance about the possible integration of 6.5×10^4 components into a single chip achieved in 2007. Fig. 1.3 (a) illustrates the follow-up of the predicted progress trend of the semiconductor industry. About 32 actual transistors in the first anticipation of this law have reached nearly 0.5 billion transistors integrated in the present, as shown in Fig. 1.3 (b). Such an enormous growth of component integration has proven that the idealistic prediction was incredible, following which it has been vital to facilitate the reduction of the discrete transistors.

The MOSFET scaling has been the essential constituent in the digital, semiconductor technological revolution, leading us to the present age with immensely multifaceted

devices and systems [5]. It is noteworthy that “Moore’s law” has been inferred in another way at the different progressive phases of the technology growth. A consensus accepted that “the number of components per chip doubles every 1.5 years”.

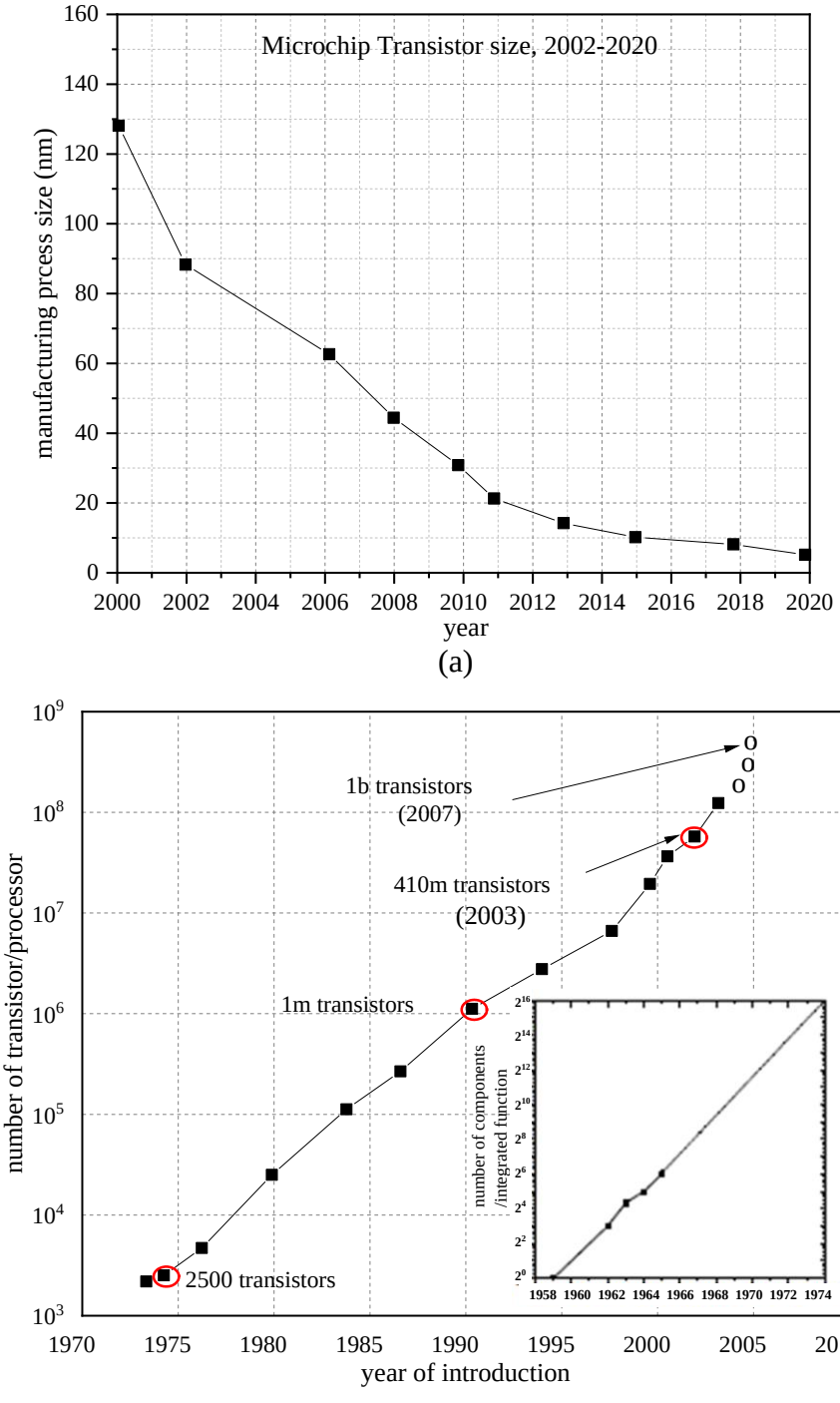


Fig. 1.3. Visualization of Moore’s Law (a) microchip transistor size (b) the transistors' numbers commercially integrated into the processor. Source: Intel Inc. [4].

However, as in the inset shown in Fig.1.4, the original speculation of Moore was components per chip doubling up every year. Indeed, in the beginning, the stated rate of development was well retained up till the 1970s and continued to the early 1980s. Later, in the last three decades, the device dimensions have experienced been an extensive reduction.

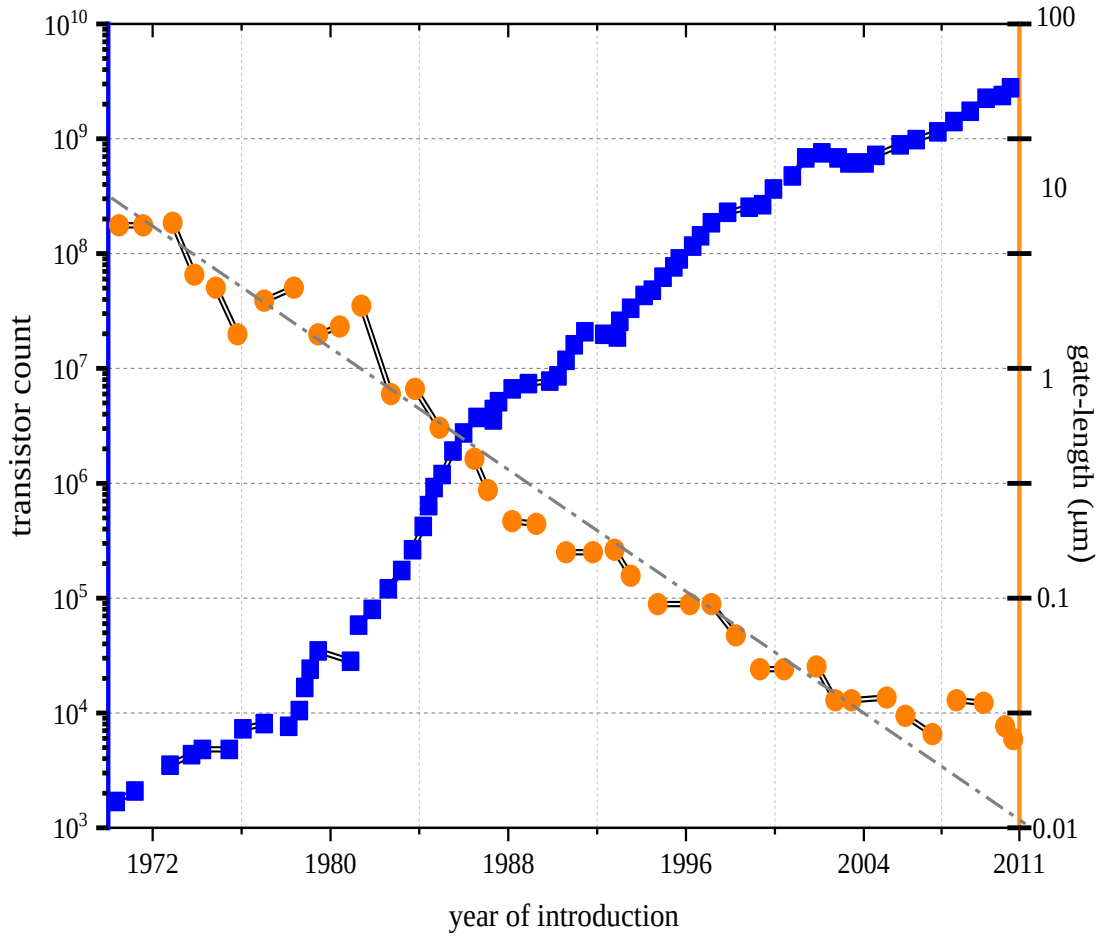


Fig. 1.4. Number of transistors and gate-length reduction over the years [5].

The trend of reducing the number of transistors and gate-length over the years is shown in Fig. 1.5. It can be perceived that since its initiation, the device design in the 1970s that having the least feature-length of 10 μm had a steady reduction down the line up till 2000 to 0.15 μm of the size. It was an approximate reduction at a 13% rate during those years [6]. However, the appropriate scaling does not only mean a decrease in the gate-length and width, but all the other dimensions such as gate/source and gate/drain alignment, oxide thickness, and depletion-widths are also involved.

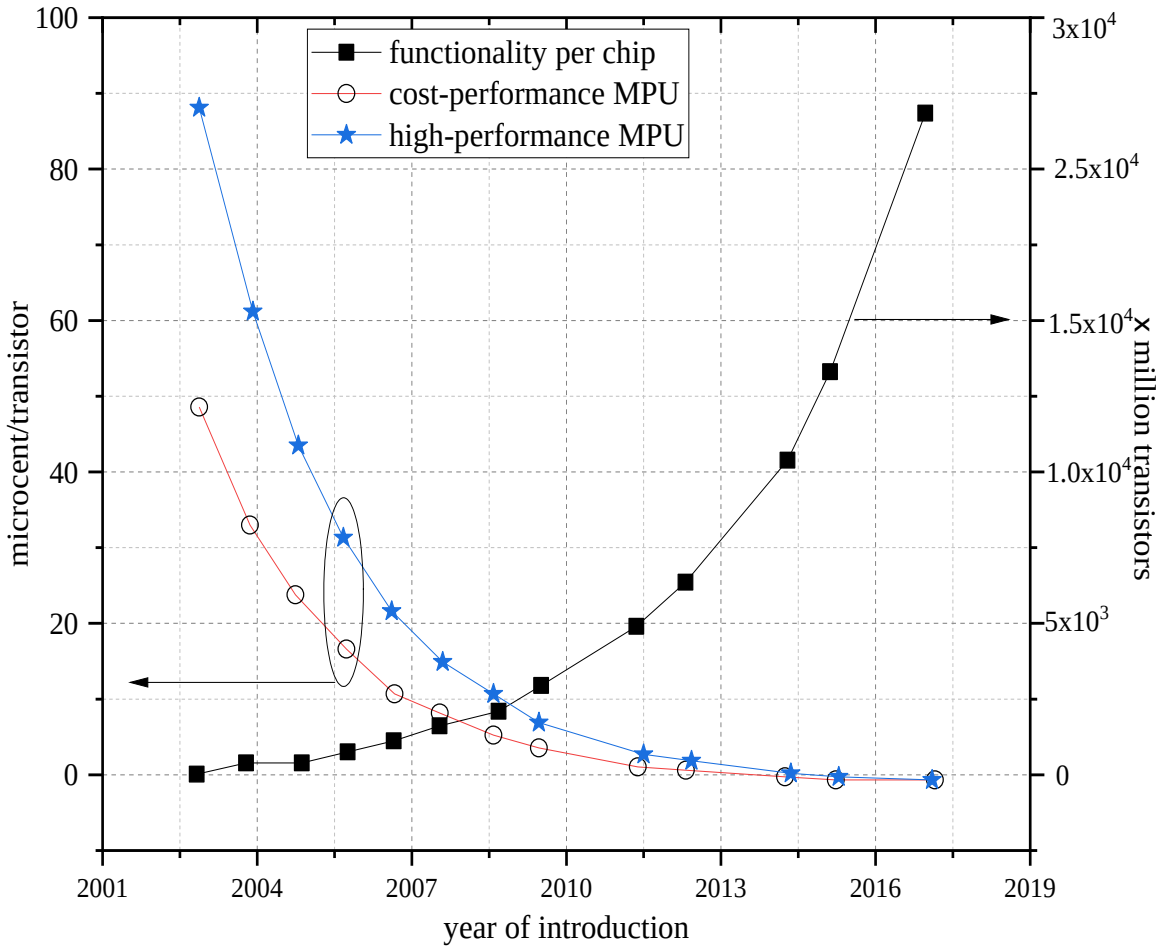


Fig. 1.5. Performance of high-speed Microprocessor unit and the functionality versus the year of technology nodes: source ITRS 2004 update [6].

1.3.1. Benefits of Scaling

The data rate capacity depends on the number of logical transistors in a memory chip, termed as functionality in the microprocessor units [7]. Integrating components in a single chip has been growing day by day. Such increasing compactness is in the form of increasing functionality per chip and increasing density, as shown in Fig. 1.5. Therefore, the primary benefit of scaling can be given as follows:

1) To achieve high device packing density,

2) To improve frequency response, and

3) To improve the current drive (transconductance g_m).

1.3.2. Types of Scaling

There are two types of commonly known scaling methods: constant-field scaling and constant-voltage scaling [8]. The constant electric field scaling is based on reducing the operating voltage such that the magnitude of the electric field (vertical or horizontal) stays constant while the transistor dimensions, including the gate-length, the gate oxide thickness, and the supply voltage, are scaled by the identical factor $\kappa < 1$.

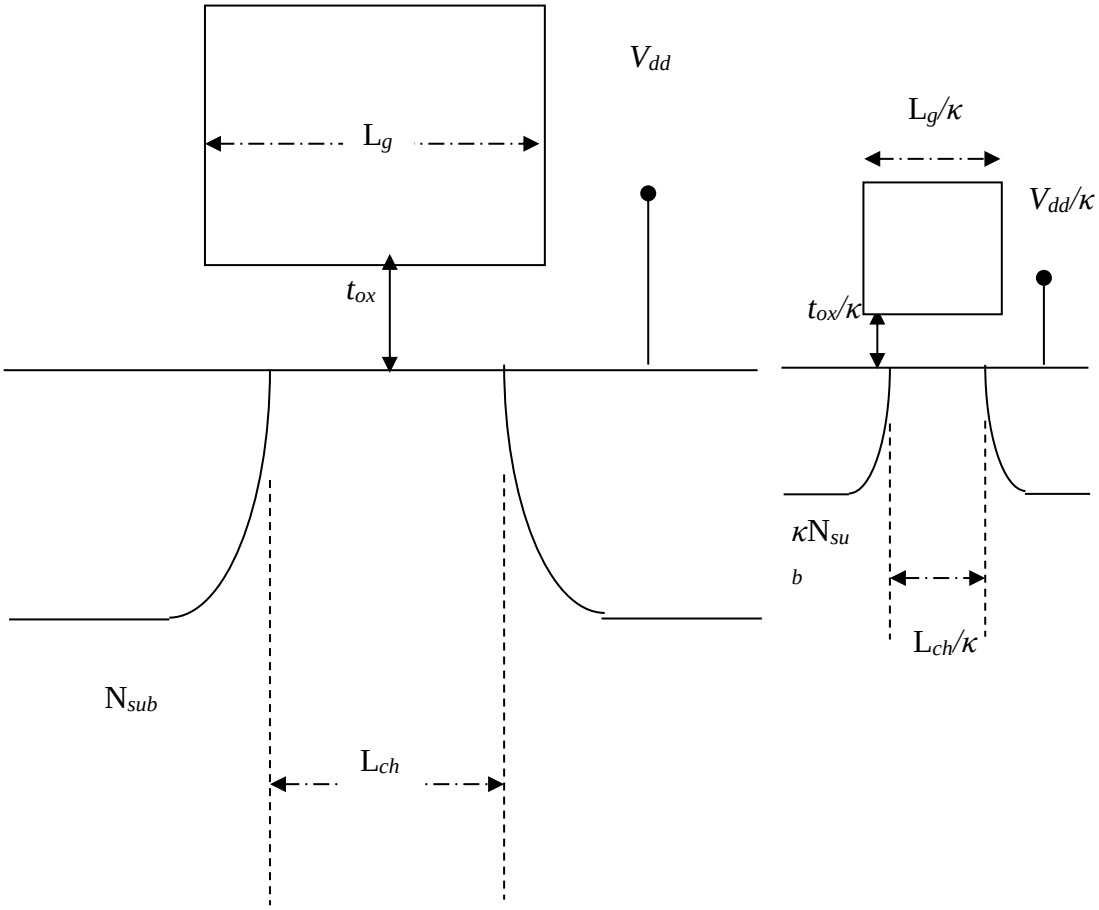


Fig. 1.6. Sketch of MOSFET Scaling [8].

The scaling approach of the constant electric field scaling situation proposed by *Dennard* et al. [9] is shown in Fig. 1.6. However, it produces an enormous decline in the power-delay product of a different transistor. On the contrary, a constant-voltage scaling is conceived on voltage compatibility with previous circuit topologies keeping the supply and the terminal voltages are kept unaltered.

Table 1.1. Comparison of scaling methods in a MOSFET device.

Parameter (Symbol)	**Constant-field Scaling**	**Constant-voltage Scaling**	**Constant-voltage scaling with velocity saturation**
Gate-Length (L)	$1/\kappa$	$1/\kappa$	$1/\kappa$
Gate-Width (W)	κ^2	κ^2	κ^2
Gate insulator thickness (t_{ox})	$1/\kappa$	$1/\kappa$	$1/\kappa$
Electric filed (E)	1	κ	κ
Substrate doping (N_{sub})	κ^2	κ^2	κ^2
Gate-capacitance (C_G)	$1/\kappa$	$1/\kappa$	$1/\kappa$
Insulator capacitance (C_{ox})	κ	κ	κ
Transit time (τ_r)	$1/\kappa^2$	$1/\kappa^2$	$1/\kappa$
Transit frequency (f_T)	κ	κ^2	κ
Voltage (V)	$1/\kappa$	1	1
Current (I)	$1/\kappa$	κ	1
Power (P)	$1/\kappa^2$	κ	1
Power delay ($P\Delta t$)	$1/\kappa^3$	$1/\kappa$	$1/\kappa$

The comparative list of design factors and parameters of different scaling methods is shown in Table 1.1. It has a drawback that the electric field rises when the minimum feature-length is compacted. Several second-order effects such as velocity saturation, mobility degradation, increased leakage currents, and lower breakdown voltages exist at reduced device's dimension.

The comparison is shown among the constant-field scaling, constant-voltage scaling, and the constant voltage scaling in the presence of velocity saturation [8].

1.3.3. Scaling Challenges

The challenges in scaling the device include the need for strategies to reduce subthreshold conduction, leakage minimization in gate-oxide and junctions, reduced output conductance and transconductance, and diminishing interconnect capacitance, normalizing heat production, and other process and modeling complexities [2-4]. The issues that arise in scaling the device involve overcoming the trade-off among the power consumption, short-channel effects (SCEs), and the low current. As the traditional MOSFETs fail to attain the desired device performance, alternative device structures for further scaling had been continuously explored.

1.4. Short-Channel Effects (SCEs)

The gate-length is one of the most significant constraints associated with transistor scaling. Smaller gate-length allows the more significant drive current and subsequently fast-speed operation as the parasitic capacitances are also scaled. Therefore, high performance at the lower voltages is operational [13].

The actual channel length is determined by deducting the over-all lateral diffusions of the source and the drain from the device's physical gate length. The physical gate length is more than the actual length; however, the difference ($Lg - L_{ch}$) cannot be computed exactly. When the actual length is scaled down, at specific consented points, so-called SCEs appear, which is not experiential otherwise.

The SCEs are abandoned if the device is a long-channel; nevertheless, the device performances are badly affected [14]. The MOSFETs at short-channel encounter the following significant phenomenon. In short-channel devices:

1) Two-dimensional electric field profile that results in the reduction in the threshold voltage and Drain-Induced-Barrier-Lowering (DIBL),
2) Very high electric field strength in the channel introduces impact ionization Hot Carrier Injection (HCI), and the breakdown and parasitic effect,
3) Limitation imposed on electron drift characteristics brings mobility degradation and carrier velocity saturation,

4) Physical separation between the source and the drain decreases, familiarizing channel length modulation, and Punch-through phenomena.

1.4.1. Two-Dimensional Field Profile (V_{TH} Reduction and DIBL)

The potential field distribution turns into a 2-dimensional form instead of a uni-dimensional profile due to channel length reduction with scaling. Consequently, the channel's charge-control, i.e., charge sharing among the gate, substrate, source, and drain, originates. Further, the region's depletion depth is supplemented by a high surface-potential that attracts more conducting charge and current from the channel, influencing the threshold voltage reduction.

The effect on threshold voltage due to reducing channel size is depicted in Fig. 1.7. The arc that represents decreasing threshold voltage with the declining effective length is known as V_{TH} roll-off, which is probably an intimidating barrier in future MOSFET design. The minimum acceptable length for the channel is mainly decided using the roll-off characteristics.

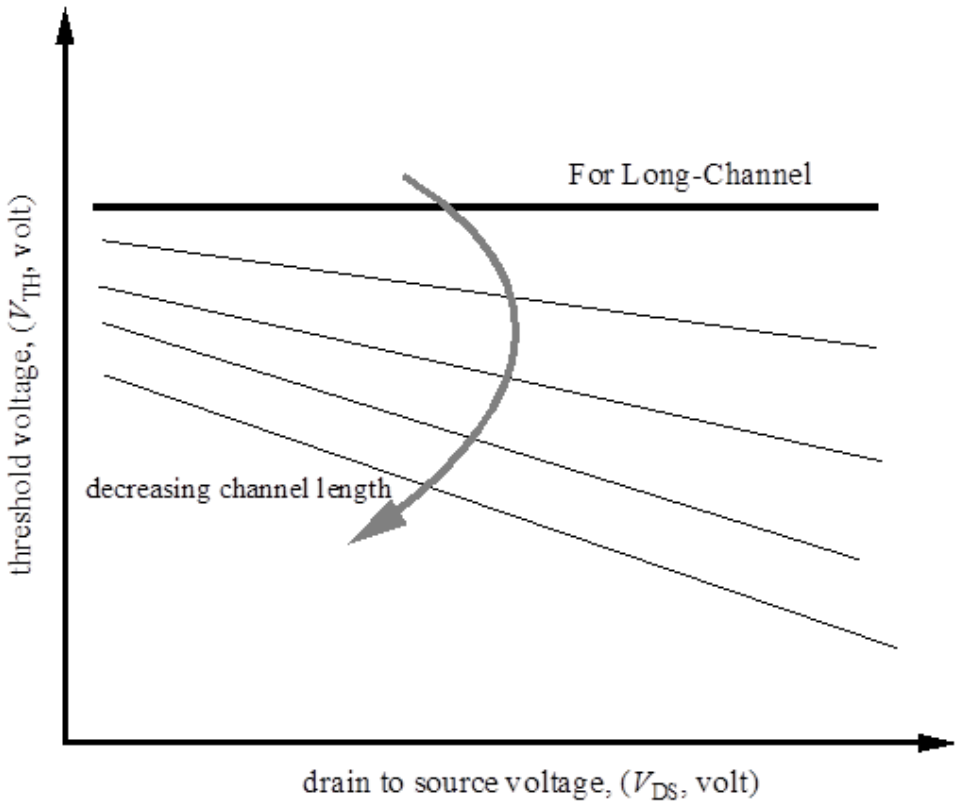
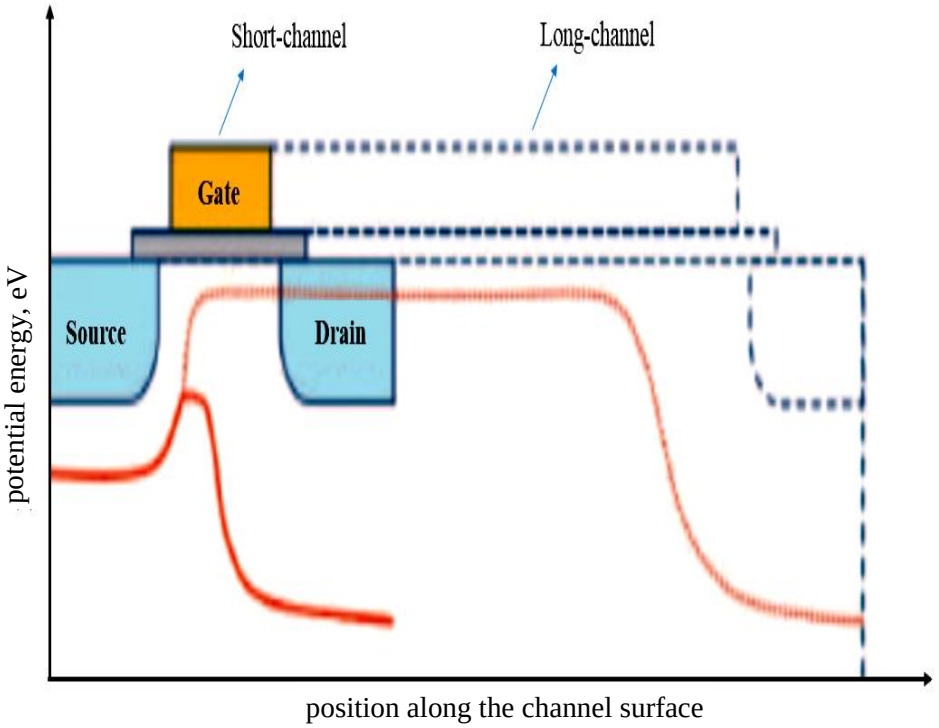
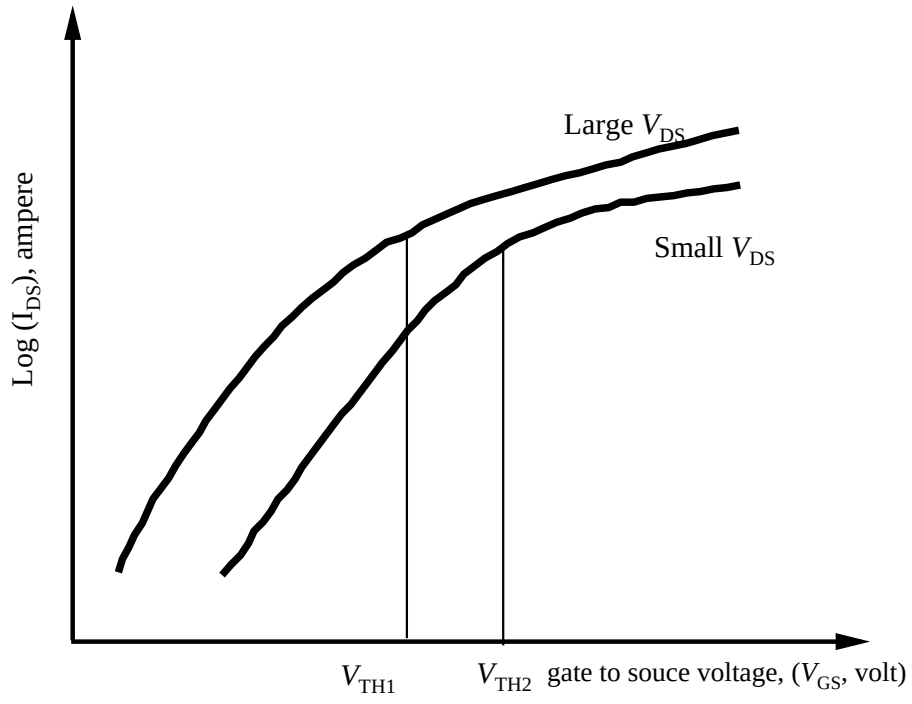


Fig. 1.7. Effect of channel length reduction on threshold voltage [15].



(a)



(b)

Fig. 1.8. DIBL (a) illustration of the effect, (b) effect on the current characteristics.

As illustrated in Fig. 1.8 (a), a variation of the threshold voltage at a shorter gate-length device is controlled by the applied drain voltage to affect the inversion charge initially caused by the high drain voltage [16].

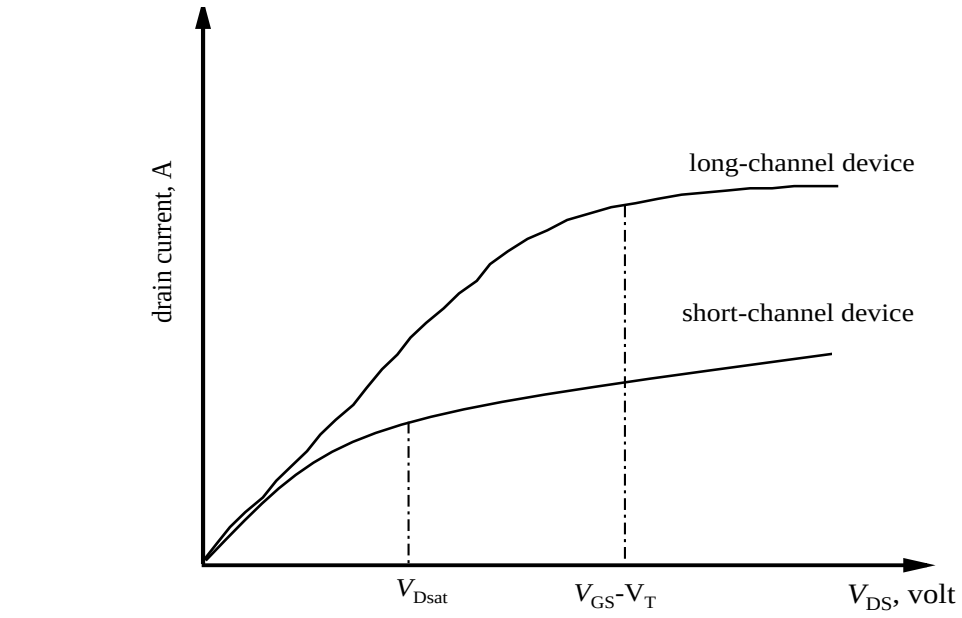
Accordingly, the gate voltage or turn tin voltage V_{TH} is influenced due to the field distribution close to the drain. Such occurrence can be omitted using an appropriate scaling of the drain and source depths, maintaining the substrate doping concentration. The Drain-Induced-Barrier-Lowering (DIBL) effect exists if the gate-length reduction occurs in the absence of accurate scaling of the other device dimensions, then the drain affects the output conductance and threshold voltage as shown in Fig. 1.8 (b).

1.4.2. Very High Electric Field Strength (Impact Ionization)

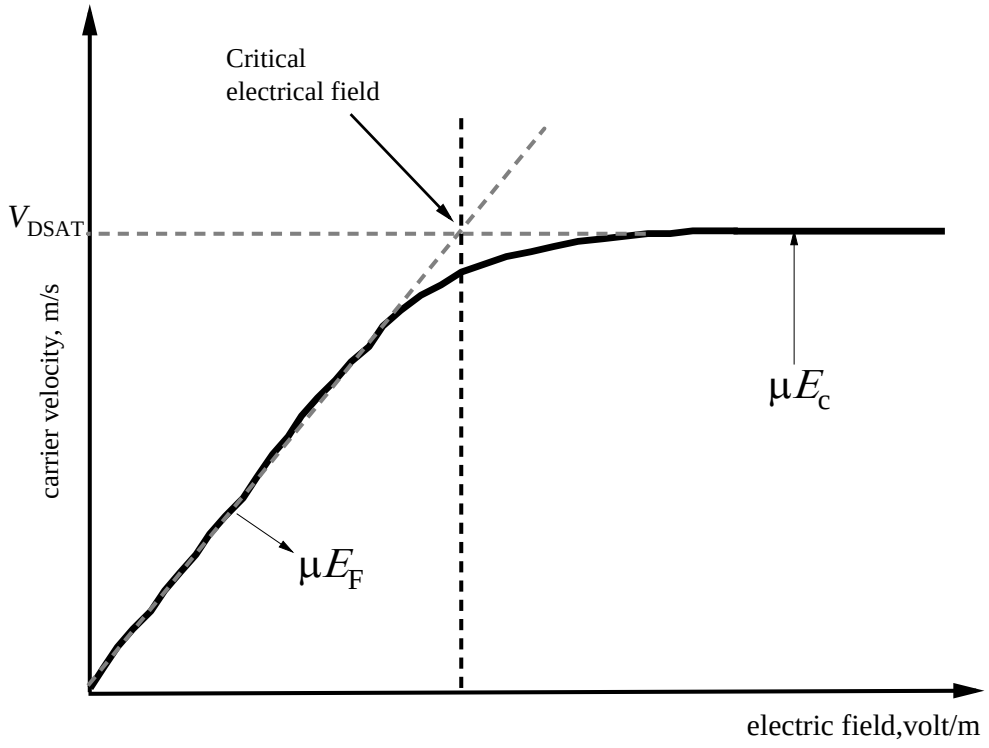
The longitudinal field in the device channel is inclining and increases from the source to the drain region. In the scaled device, source and drain adjacent junctions lead to the highest field at the drain that deteriorates alongside the channel. The charge carriers gain extra-energy due to increased field and get accelerated with an increased velocity. A charge that passes through the inversion channel at the pinch-off condition in the direction of the drain accelerates faster to attain maximum kinetic energy when in saturation. High energy charge-carriers are referred to as hot-carriers and can create silicon lattice-collision with their acquired power that impacts impact ionization [17].

1.4.3. Mobility Degradation and Carrier Velocity Saturation

In particular, the inversion layer's mobility in the device is lesser than that of the substrate due to electron wave function expansion over the low mobility gate insulator. Typically, the surface electric field is higher in the short-channel devices, bringing an extra-impulsion to the electron wave-function into the gate insulator known as field-dependent mobility. Therefore, the mobility at the surface weakens with the electric field, known as mobility degradation. It happens in two ways: mobility reduces with the increasing gate voltage due to the vertical electric field and the other when the mobility decreases with the drain potential by the parallel electric field [18].



(a)



(b)

Fig. 1.9. Velocity saturation in short-channel device (a) nonlinear operation, (b) critical electric field [18].

In general, the electric field's combined effect altogether drives the electron transport, the lattice-scattering, the impurity, and the other charge control in the device. When the electric field (E) is low, the mean velocity of charges (v_{drift}) is proportional to the electric field, i.e., $v_{drift} = \mu E$ with proportionality constant as charge mobility (μ). The drift velocity at saturation (v_{SAT}) for the critical electric filed (E_C) is given by:

$$v_{drift} = v_{SAT} = \mu E_C \tag{1.1}$$

However, the relationship does not follow linearity at the higher electric field due to scattering delays across the channel length (L), therefore drain saturation voltage (V_{DSAT}) can be written as:

$$V_{DSAT} = E_C.L = \frac{v_{SAT}.L}{\mu} \tag{1.2}$$

$$\text{and, } I_{DSAT} = v_{SAT} C_{ox} W \left[(V_{GS} - V_{TH} - \frac{V_{DSAT}}{2}) \right] \tag{1.3}$$

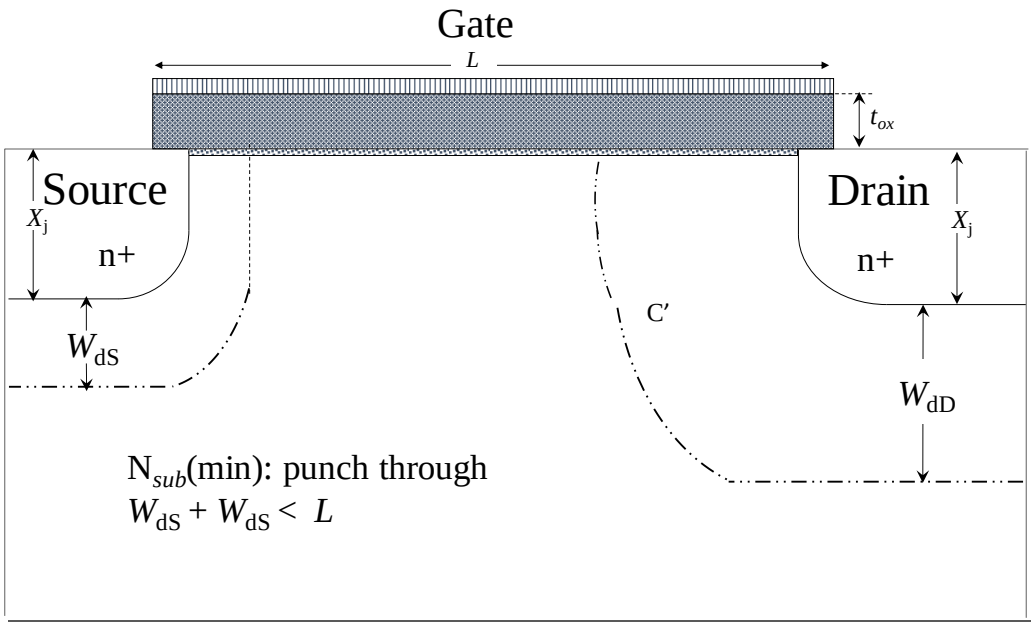
where I_{DSAT}, C_{ox}, and W are the drain saturation current, oxide capacitance, and the channel width of the MOSFET, respectively. When electric field energy is more than the carrier energy, the velocity gets saturated to v_{SAT}. The situation concerns the drain current shifting to the nonlinear operation, as shown in Fig. 1.9 (a). E_c, known as the critical field, introduces velocity saturation in the short-channel device as depicted in Fig. 1.9 (b).

The critical field is of order ~10^6 V/m. Due to velocity saturation, results in saturation current (I_{DSAT}) to endure smaller values than to the idealistic correlation, yielding further for a reduced saturation current (V_{DSAT}) [19]. The velocity saturation occurs before reaching the pinch-off condition, and accordingly, the saturation appears even at the low drain voltage values. Therefore, the short-channel devices are more frequently inclined to switch operation in extended saturation conditions.

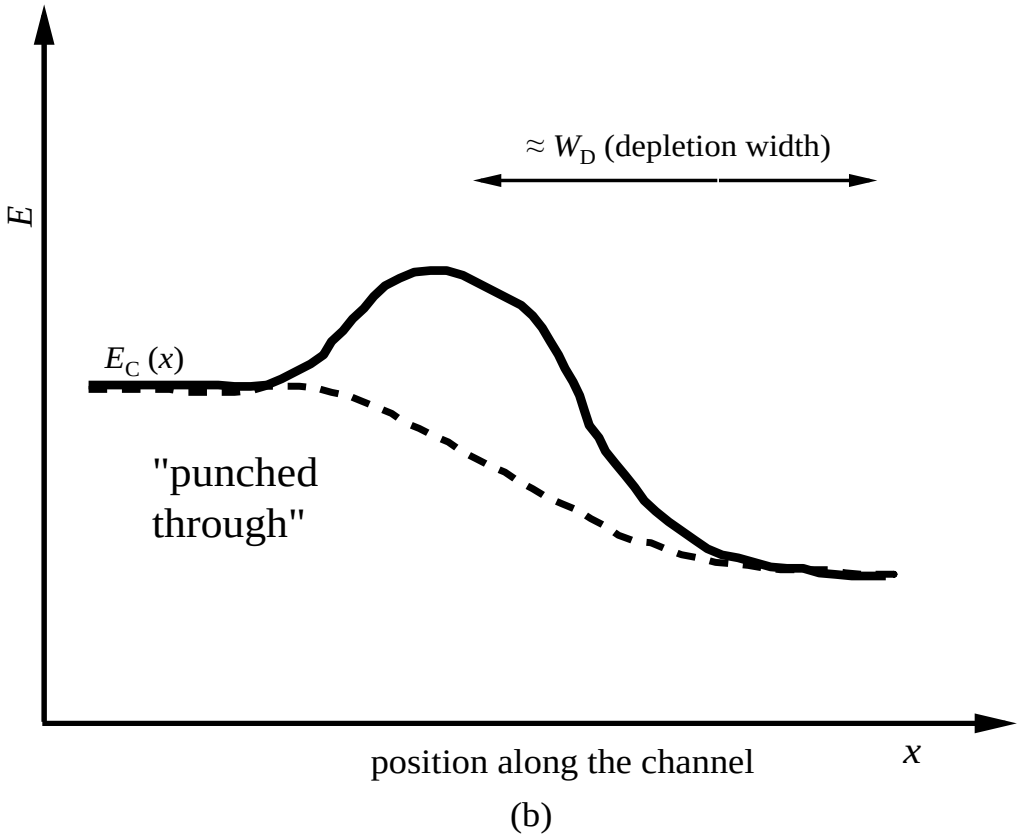
1.4.4. Channel Length Modulation (CLM) and Punch-Through

The channel's actual length tends to reduce with increasing drain potential as the drain depletion region widens, known as the channel length modulation (CLM). Referring to Fig. 1.10 (a), in the long channel devices, actual length decrement is insignificant compared to the total channel length, while it is highly affected in a short-channel device

that reduces the channel length towards zero. Also, both the depletion width regions can touch, resulting in a massive drain current as depicted in Fig. 1.10 (b).



(a)



(b)

Fig. 1.10. (a) Representation of Channel length Modution and (b) punch-through condition in short-channel MOSFET[21].

The drain comes very close to the source due to the drain depletion region's extension and forms a distinct depletion region [21]. Consequently, the source-drain potential makes a stronger field under the gate region, which opens the obstruction of current undesirably to switch the transistor to an abrupt turn-on. This is essentially equivalent to reducing the transistor's threshold voltage, which leads to a higher leakage current.

The resultant actual length is equivalent to the metallurgical size minus the depletion widths of the source/drain part. An extreme case of the CLM is known as punch-through.

1.5. Background and Evolution of CSDG MOSFET

As the most critical device component of modern electronics, the MOSFET has a persistent history of rigorous reforms and phenomenal scaling traced from Moore's prediction of shrinking device size and package density.

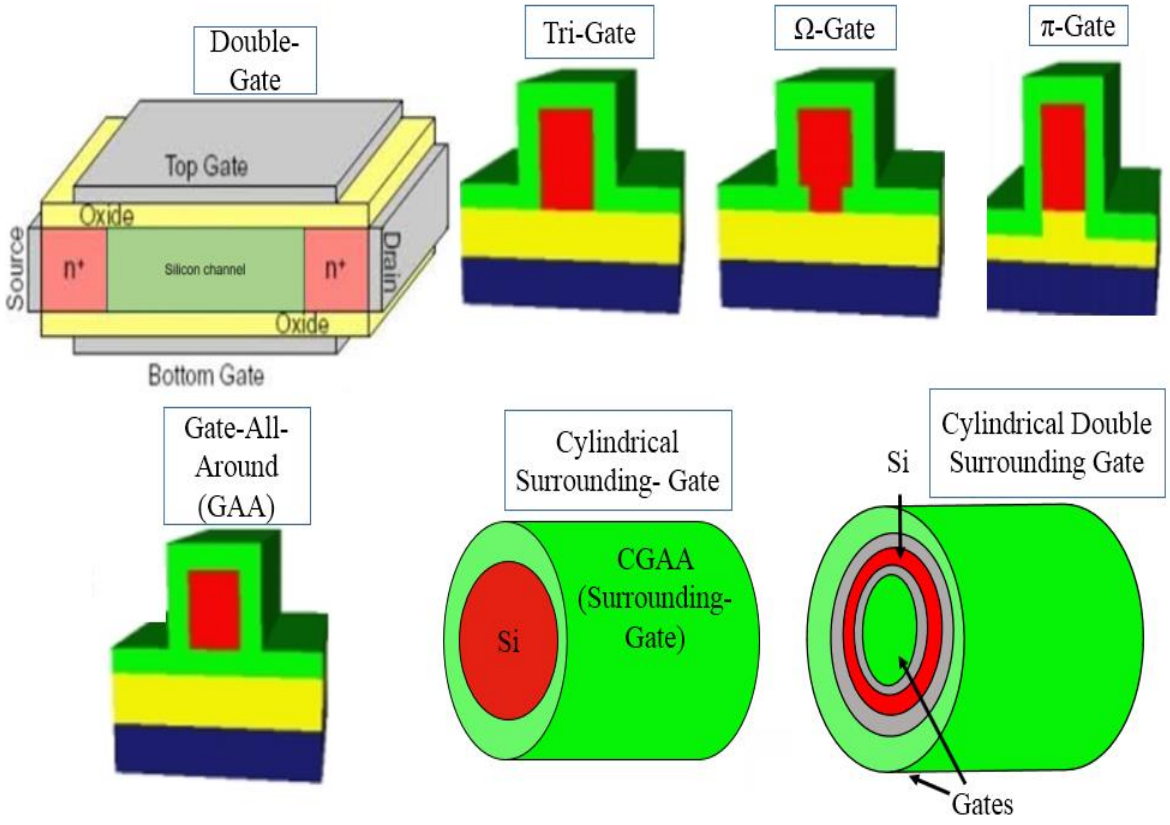


Fig. 1. 11 Multigate and surrounding gate MOSFET structures [26].

The scaling of dimensions which exceeds two orders of magnitude in the past decades has undergone extensive physical modifications besides addressing the gate-control for optimum performance of the device [22]. The rapid decrease in the device dimensions with Moore's law's advent follows several problems such as Short-channel Effects (SCE's) and Hot Carrier Effects. In the last three decades, there have been extreme efforts to minimize the SCEs and the improved gate controllability utilizing various structural modifications [23, 24]. These problems have been mitigated by the introduction of multiple gates in the structure and invention of different geometries for MOSFETs. Fig. 1.11 shows the sketches of various multigate structures such as Double-Gate (DG), Triple Gate, Omega-Gate, FinFETs, Surrounding Gate (SG), Cylindrical Surrounding Gate (CSG), and so forth [25-27]. The Surrounding Gate (SG) structures have attained much popularity among the multiple-gate forms as the gate has been exhaustively enclosed by the entire semiconductor channel, which significantly enhances the gate control over the channel. As proposed by Srivastava et al. [28], the Cylindrical Surrounding double-gate MOSFET has been one of such prominent gate-all-around devices.

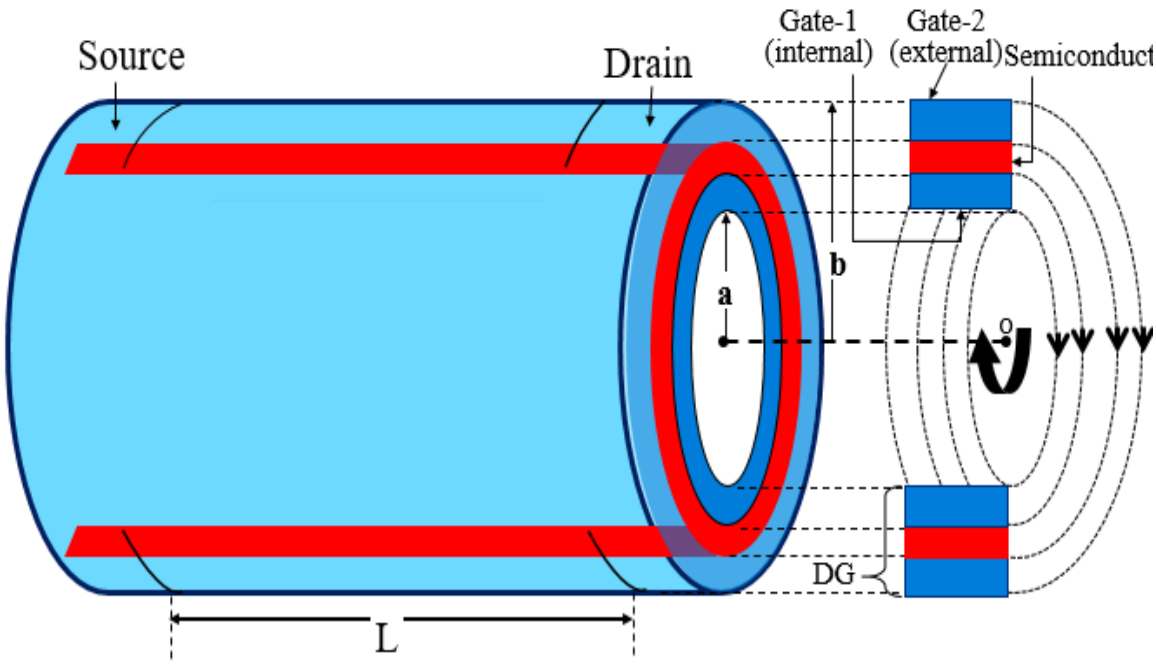


Fig. 1. 12 (a) Schematic of Cylindrical Surrounding Double-Gate (CSDG) MOSFET structure.

The device with superior control over the channel with a large driving current has been highly anticipated. The structure, proposed initially has been featured as two concentric cylindrical gates accommodated in a single transistor, enabling the device with improved control over the channel.

In particular, the structure can be perceived as a double-gate MOSFET wrapped up from the end to end founding in a cylinder as shown in Fig. 1.12. The device's inherent characteristics, including the small-signal analysis, electrical parameters, and several other applications, have been conveyed in recent years [29]. Past research confirms the potential of the CSDG for inventive circuits, wherein independent adjacent gates of CSDG enhances circuit design flexibility. The electrical and physical parameters analyzed at the device's operating conditions can control the device behavior in circuit design, resulting in improved performance. The effect of doping, analytical modeling, and enhanced characteristics have been obtained using CSDG MOSFET [30].

The analysis for obtaining improvements in the device parameters based on explicit, low frequency, equivalent capacitance model in CSDG MOSFET has potentially been reported as a significant contribution to microelectronic device research [31, 32]. A device must have higher carrier transport and drive current; therefore, either a more inventive design or the modified device physics of the existing CSDG structure seems necessary. The device modification can primarily realize enhanced electrical performance in terms of the low electric field towards the drain side, surface-potential, drain current, I_{on}/I_{off}, transconductance, and input gate-capacitance.

1.6. Device Compact and Analytical Modeling

A physics-based device model is defined as a depiction of device actions described in analytical, numerical, or mathematical terms. On the contrary, the device simulations approximate numerical expressions to explain some complex equations, such as partial differential equations. Moreover, device models may be characterized as compact if described in terms of analytical and explicit terms. The compact models can also cover reproductions that involve pre-processing of model expressions using iterative procedures to result in lookup variables for a fast recovery for a solution in the simplified models. The

compact models have the feature of intelligent computation in the event of circuit models and simulation.

1.7. Objective of the Research Work

The research objective is to analyze the gate material engineering in the Cylindrical Surrounding Double-Gate MOSFET structure with a device physics-based modeling. Moreover, mathematical derivation and analysis of the electric field and pinch-off capacitances are to be established. Further, numerical solution and silicon thickness inducing CSDG MOSFET parameters can lead to the understanding of thickness optimization. To derive and analyze the optimum semiconductor thickness depletion depth under the source-drain region, the channel's depth in the semiconductor of a CSDG MOSFET at strong inversion for recognizing the dependence parameters at drain-source bias. Finally, the model analysis of a dual-material gate in CSDG MOSFET is obtained by comparing surface-potential and electric field profiles in gate-metal research designs.

1.8. Research Questions

This section contains and describes the questions with their answers posed and investigated during this research work.

Q1: What will be the shape of the gate-oxide capacitor of the CSDG MOSFET structure at the device pinch-off operation?

Answer: In the cylindrical Metal-Oxide-Semiconductor structure of CSDG, at the device pinch-off, the semiconductor electrode becomes a cone shape region of conducting effectively. Therefore, unlike other cylindrical capacitor shapes, it assumes a truncated cone. The research problem has been addressed, and the actually anticipated sketch of the structure is demonstrated in Chapter-3.

Q2: How does the gate oxide-capacitance depends on the device dimension in CSDG MOSFET?

Answer: The expression reveals that the capacitance at pinch-off is not a direct rationale of cylindrical sizes of the device; instead, it takes a complex algebraic and logarithmic fractional form as resulted in the expression, which is comprised of the external, internal

dimensions, thickness, and material properties of the capacitive layer in the CSDG structure.

Q3: Is the gate-oxide capacitance of CSDG MOSFET is identical in all region of operation?

Answer: No, the oxide capacitance is affected by the physical capacitor plate's shape change at a pinch-off operation due to charge sharing.

Q4: How to calculate electric field due to oxide capacitance in a typical CSDG MOSFET geometry having distinct gate-assembly?

Answer: The electric field analysis due to oxide capacitance in CSDG MOSFET evolves with its structure that has a combination of two cylindrical capacitors. Therefore, first deducing the electric field's expression of each capacitor individually and further taking the algebraic sum of the specific solution is a convenient method to calculate, which results in the total electric field due to oxide capacitances.

Q5: What are the approximate device physics parameters on which the silicon (or semiconductor) thickness of CSDG MOSFET depending upon?

Answer: The CSDG MOSFET structure needs to incorporate analysis based on existing firm device physics or models to understand the variability.

Q6: How the gate-metal work function affects the electrical characteristics in CSDG MOSFET?

Answer: As the work-function is a prominent electronic property of metal, the gate metal can directly move the changes in ionic behavior of the channel, affecting the flat-band voltage and hence the device's threshold characteristics. By an appropriate pursuit to the gate-metal work-function, the internal gate's threshold voltage could be transformed to a lower than the external gate with correspondingly lower the work-function of internal gate-metal.

Q7: What will be the effect of two different gate work functions on characteristics in CSDG MOSFET?

Answer: The physics and behavior change in the source and the device's drain side takes place with different gate metals. The gate metal engineering tends to increase the undesired off-current; however, it also increases the current in a similar proportion. Furthermore, the metal with low work-function on the drain side drops the drain bias across the region. It

tends to decay in the direction of the drain end, which leads to a decline of Drain-Induced-Barrier-Lowering (DIBL) and channel length modulation effects. Further, the internal gate's threshold voltage (V_{TH1}) could be reduced compared to the external gate (V_{TH2}) by arranging the gate metal work-function in Double-Gate devices.

Q8: What gate metal architecture in CSDG MOSFET can be thought of for SCEs improvement?

Answer: As the device design and analysis in a gate-stacked and dual-metal gate structure can be found in the previous literature; therefore, it would be insightful to primarily implicate an unstacked and stacked gate metal design in CSDG MOSFET.

Q9: How is the surface-potential distribution affected by changing the length of specific metal in a dual-metal stacked structure of CSDG MOSFET?

Answer: In the dual-metal stacked structure, the surface-potential step-change is anticipated, which leads to a growth in the carrier velocity and a further increase in carrier transport efficiency of the device. The effect, in turn, increases the drain current of the device. Furthermore, it can be practical that the minima of surface-potential shifts towards the source side, which lies underneath the region of higher work-function metal.

Q10: How is the electric field distribution affected by changing the length of a specific gate metal portion in the dual-metal stacked structure of CSDG MOSFET?

Answer: In a MOSFET device, changing the length of specific metal causes relocation of the lateral electric field closer to the source region, and the uniformity of the electric field in the channel enhances. Moreover, the electric field minima distributed along the channel positions of metal interfaces are changed with the specific metal region's length. If the CSDG MOSFET analysis is done with a dual-metal gate design, the advantages of gate-metal engineering can be replicated.

Q11: Which methods can be relevant to approximate the channel thickness?

The depletion depth theory to develop thickness analysis for the CSDG MOSFET structure would be appropriate based on the well-known Dang's model approach of charge sharing.

Q12: How can the thickness dependence be compared in the CSDG MOSFET structure with the planar MOSFETs?

Answer: The CSDG structure is a unique structure derived from the cylindrical orientation of double-gate MOSFET. The device design has several benefits as it provides better gate

control due to surrounding gate geometry. A planar structure and CSDG MOSFET depletion-width computation, including doping and bias voltages, should be made side-by-side to accomplish the firm estimation.

1.9. Research Contribution of this Thesis

This thesis aims to analyze and incorporate the impact of gate material engineering in the CSDG structure with a device physics-based modeling to combat the effect of SCEs. To attain the objective, in particular to the proposed design, an electric field, capacitance, and other characteristics parameters have been calculated at a pinch-off to analyze the capability of CSDG MOSFET. Further, this thesis work provides insights into the thickness of the device parameter dependence that has been mathematically analyzed in detail at the onset of strong inversion. Finally, a design and numerical analysis of dual-material gate and gate-stack in the CSDG MOSFET have been explored.

1.10. Organization of the Thesis

The research work presented in this thesis has been organized in chapters as follows:

Chapter 1 provides an introduction starting with an overview of MOSFET and a brief background, challenges associated with the scaling, understanding the short channel effects, development of the CSDG MOSFET structure, research questions, and objective places the foundation of the research addressed in this thesis.

Chapter 2 details the literature review, including the trace of the research progress made in analytical model developments, gate-capacitance modeling, progress in CSDG MOSFET research, gate material engineering, and motivation thesis research work.

Chapter 3 describes the analytical research of gate-oxide capacitance in CSDG MOSFET, particularly at the device pinch-off condition by deducing the oxide capacitance for the internal gate and external gate assembly the device and summarized the obtained results.

Chapter 4 deals with the electrical field analysis due to gate-oxide capacitances explaining the model derivation for CSDG MOSFET and the summary results.

Chapter 5 specifies the research work of the depletion width analysis in MOSFET device with details of depletion depth in MOSFET.

Chapter 6 includes the analysis of thickness in CSDG MOSFET founded upon the depletion depth model concept at the onset of strong-inversion, including the evolution of depletion depth, optimum semiconductor thickness, and result from analysis with a chapter summary.

Chapter 7 comprises the details of the novel Dual-Metal Gate architecture included in the CSDG MOSFET. The detailed description of the stacked designs concept, model formulation, derivation of the surface-potential, the gate charge, and the threshold voltage has been elaborated with the comparative results.

Finally, Chapter 8 concludes the research work presented in this thesis and recommends the future work scope.

Chapter-2

REVIEW OF LITERATURES

This chapter provides detailed research progress in developing analytical, explicit, or compact models for various MOSFET structures. This chapter's subsections describe the comprehended literature study organized to portray the background of chronological progress in reaching the analytical models of different device structures, understanding progress made in CSDG MOSFET, and other relevant efforts made that laid the foundation of the research problem and motivation of this research work.

2.1. Review of Analytical Models Developments

Oh et al. (2000), in their work, have compared the electrostatic potential confined by the gates of DG and CSG MOSFET using the Evanescent-Mode Analysis (EMA) solution. They have notified that the device dimension of cylindrical surrounding-gate (CSG) MOSFETs is much reduced (to 35 percent shorter of the actual lengths than double-gate MOSFETs) Silicon, the insulator thicknesses in the CSG MOSFETs can be better scaled up for mitigation of SCE [33].

Jimenez et al. (2004) have presented a validated a simplified, compact model for lightly doped CSG MOSFETs based on the meticulous solution of the Poisson's and the continuity equation deprived of the charge-sheet approximation to describe the inversion charge distribution in the channel.

Further, it was confirmed that a simple analytical *V-I* model is suitable for compact modeling of undoped (lightly doped) SGT MOSFETs. The model was reportedly capable of an accurate description of all regions of operation. Specifically, the inability to capture volume inversion using the charge-sheet approximation had been well addressed in their work [34].

Aouaj et al. (2005) have deduced the 2-D analytical model using EMA for an fully depleted. cylindrical/surrounding gate device structure to compare Surface-Potential and threshold voltage with the other models. Their work revealed characteristic length dependence, which is governed by silicon and oxide thickness [35].

Quenette et al. (2009) have proposed an innovative, dynamic charge sharing model for 45 to 65 nm technology nodes for electrical characterization and compared it with the charge sharing V_{TH} model to enhance the device performance at low power consumption memory application. They reported the electrostatic characteristics of experimental data in terms of SCEs DIBL, subthreshold slope variations, and V_{TH} dependence and suggested improved capacitive response of the device in non-volatile memory applications [36].

Verma et al. (2015) have proposed a physics-based model for their surrounding double-gate nanowire MOSFET structure based on the solution of 2-D Poisson's equation and superposition of the coordinate system. Using the simultaneous validated simulation, they reported the influence of channel length variation on the double surrounding gate device's electrical behavior and indicated double-gate CSG's superior performance over the single CSG MOSFET [37].

Jena et al. (2015), in their research of scaling comparison of the device design, have explored and described an undoped Cylindrical Gate All Around (CGAA) structure. Further, based on their device results [38], they suggested the utility of the device structure's undoped nature for suppressing SCEs and other scaling complications.

Verma et al. (2016), in the research work [39], have presented the modeling and simulation of CSDG MOSFET with an alternative gate insulator as vacuum than SiO_2 for improvement of hot-carrier reliability and radiofrequency RF performance. They concluded that the vacuum as a gate dielectric could substitute the double surrounding gate in a CSG form for evading the inconsistencies raised by the hot-carrier injection.

Sood et al. (2016) have analyzed the performance of various parameters for the surrounding-gate MOSFET device and informed the influence of Gaussian doping on the undoped device's electric potential and electron density [40]. They reported that the surrounding-gate devices have been better in terms of unilateral and maximum power gain in the RF applications.

Basu et al. (2017) have proposed an analytical model for the electrical characteristics of surrounding gate MOSFET in strong inversion by solving simplified 1-D Poisson's equation in conjunction with the rectangular and cylindrical coordinates for device boundary condition. The designed device was reported with a high concentration of

inversion charges that significantly influenced their research to obtain more excellent gate controllability [41].

Nandi et al. (2017), in a paper, have developed an analytical model of double-gate MOSFET using Green's function approach in the subthreshold regime of operation [42]. The method was reported useful for forecasting the electrostatics of devices in which the S/D lateral electric field is of prime significance.

Taur et al. (2018) have demarcated a double-gate MOSFET model that pushes substantial revisions in the gradual-channel estimation approach using lateral field gradient.

It has been specified in their model that when saturation occurs and goes beyond, the channel pinch-off does not happen, which leads to only limited output conductance [43]. The method proposed by them can improve the output conductance in the saturation region of operation.

Agarwal et al. (2018) have described a two-dimensional surface-potential model in gallium-arsenide-based nanowire GAA MOSFET using appropriate boundary conditions and informed the performance parameters. Their efforts have been promising for the utilization in compact modeling [44].

Uchechukwu et al. (2019) have analyzed the threshold voltage and subthreshold swing of a CSDG MOSFET using EMA and compared the other models such as polynomial exponential and parabolic potential approximation (PPA) [45]. As a significant gain, the threshold voltage roll-off has been optimized in their research by reducing the oxide thickness and diameter of the Silicon of the device structure.

Sharma et al. (2004) have explained the current conduction progression using fabrication of nanowire wrap-around-gate Silicon MOSFET to investigate and compare SOI top-only-gate planar MOSFET. It was suggested that a significant increase in current density is possible in the nanowire devices compared to the planar devices [46].

In their work, a semi-empirical carrier mobility relation for the non-planar device was used by them. The experimental results showed that the current was a linear function of the number of wires.

2.2. Review of Progress in Gate-Capacitance Analysis

Moldovan et al. (2006) have developed gate-capacitance analytical expressions for undoped surrounding gate MOSFETs using a unified charge control approach to derivate the small-signal model. They have verified the model parameters' boundless continuity in desirable proximity with the 3-D numerical simulations of modeled capacitances. They have described the correlation mobile charge sheet density among current, total charges, and capacitances for the channel boundaries [47].

Ruiz et al. (2010) proposed and comprehended a comparison of the model for total gate-capacitance of the CSG transistor and DG, accounting for both dielectric capacitance and the inversion capacitance [48]. Their study explained the mobility degradation due to capacitive charges in the two devices, increasing short-channel device consideration. Moreover, they have highlighted the impact of gate insulator's low thickness in modifying the inversion and gate-capacitance.

Cousin et al. (2011) have enlightened research on a unified compact model of undoped short-channel GAA MOSFETs and established a continuous explicit method that endorsed all regions' operation [49]. Their proposed approach was convenient, as reported in the validated model simulations.

Marin et al. (2013) have demonstrated effective gate-capacitance modeling of nanowire structure devices, including the quantum confinement of oxide-capacitance, density of energy states, and the charge scattering in the nanowire [50]. They showed a comparison of device capacitive behavior with III-V group material nanowires and the Silicon-based alternatives. Their work suggests an accurate description of gate-capacitance and defines the current drain model at device pinch-off.

2.3. Research Progress in CSDG MOSFET

Srivastava et al. (2011) have shown the analysis of CSDG MOSFET design operational in radio frequency switching [51]. They emphasized the circuit-level equivalence of parameters for ON and OFF conditions of switching in the microwave sub-system. They have treated the device approximation with lumped-circuit elements to concluded their observation of the drain current behavior to point device compatibility in RF switching applications.

Srivastava et al. (2013), in their other work, have predicted an explicit-function-based device model of undoped CSDG MOSFET built upon fundamentals of unified charge control by a side-by-side comparison of properties of double-gate and single-gate MOSFET [52]. *Srivastava et al.* (2016) have analyzed and disseminated the switching speed of CSDG devices and recommended the device for faster-switching in the device-nanoscales using a circuit model of parasitic resistance and capacitances [53].

Uchechukwu et al. (2017) have shown a typical rectifier circuit's possible low power operation using the CSDG basic structure's customization into the conventional diode bridge rectifier arrangement [54].

Srivastava et al. (2017) have enumerated the scaling advantages of CSDG devices beyond 22-nm nodes and predicted optimizing the device parameter for small-sized transistors [55].

Oyedeji et al. (2017) have deliberated an amplifier circuit perspective in the research paper [56]. They have also proposed CSDG MOSFET in mixer circuits application and reported the device competency in reducing thermal noise effects for the nanotechnology applications [57].

Naidoo et al. (2018) has presented research on circuit simulation of 0.3 TeraHertz active high pass filter involving the electrical characteristics of CSDG MOSFET with high-k gate-dielectric material in the device layout [58].

Shunqukela et al. (2018) have discussed a two-dimensional model using gradual channel approximation for the Surface-Potential model of the fast-switching CSDG MOSFET to circumvent the SCE [59].

Uchechukwu et al. (2020) have described the natural-length scaling for the potential profile in CSDG MOSFET's channel to quantify the impact of SCEs in the nanometer regime to determine the scaling factor [60].

2.4. Review of Gate Material Engineering

Baishya et al. (2007), in a paper, have presented a Surface-Potential model with two material gates for DMG MOSFET of submicron scaling, assuming a varying depth of the

channel depletion region caused by the difference in flat band potentials, and the deposits about the source/drain junctions. The work advised close contract and well-prediction for subthreshold current improvement based on their model comparison with the device simulator [61].

James et al. (2010) have presented a fabrication and simultaneous simulation of Double-Gate MOSFETs with different metal gate work functions to attain the device characteristics using 2D quantum transport and Poisson equations [62]. They reported their observation of more significant suppression of SCEs in atomic-layer deposited p-type device in terms of slighter DIBL, low subthreshold characteristics, and the improved on-off current ratio (of the order of 10^4) and linear increased threshold voltage with the metal gate of work functions ranging 4.2 to 4.5 eV.

Ghosh et al. (2012) have proposed a metal gate-stack design in the surrounding gate structure MOSFET to demonstrate the impact of stack combinations is getting enhanced SCE immunity [63]. The outcome presented by them ensures improved carrier transport efficiency using the stacked architecture of metal gates.

Pal et al. (2014) have researched on development of a model for the Dual-material Surrounding Gate MOSFET (DMSG) for the analytical treatment of electrical parameters using parabolic approximation. A good match of their model results has been reported using simulation that delivers a significant suppression of adverse short-channel effects [64].

Mohapatra et al. (2014) have demonstrated a quantifiable evaluation of gate stacked junctionless double-gate MOSFET with numerical computation keeping gate metal work functions of 4.52 eV, 4.6 eV, and 4.7 eV. The results have optimized the value of the device dimension's gate work function, considering the trade-off between subthreshold slope and DIBL. Improvement in the device sensitivity and the electrical behaviors have been informed y tuning the other device parameters with the device design guideline [65]. Further, they analyzed the drain model involving the pinch-off and reported that the model could accurately determine the exact characteristics in wide-ranging biasing conditions and device dimensions. Moreover, their model's validity in the entire region of device operation, including subthreshold, linear, and saturation, appears quite encouraging.

Jouri et al. (2015), in their paper, have discussed a methodical model for the short-channel tri-metal gate CSG MOSFET with high-k dielectric over SiO_2 is derived based on a center-potential solution. They showed that the high-k material in the gate-metal engineered device could surprisingly amend the impact on DIBL characteristics. Further, a trade-off between gate lengths, DIBL, and high-k material oxide has been exemplified in their work [66].

Hui et al. (2016) have described a model for symmetrical double-material strained silicon MOSFET having two-gate. They disseminated the comparative analysis of the electric field and the Surface-Potential with single-material double-gate MOSFETs. Their work added a more in-depth insight into the design with impact analysis of various device parameters [67].

Fairouz et al. (2019) have experimented with triple material in junction-less CSG MOSFET as an exceptional alternative of conventional MOSFET. They reported the benefit of convenient fabrication with the elimination of the p-n junctions. The impact of channel length and high-k dielectrics materials on the subthreshold features and low power optimization was reported to suggest SCE mitigation and device reliability [68].

Hasan et al. (2019) have implemented simulation to explain the modification of the work function of gallium nitride-based DG-MOSFETs to obtain the adjustment of V_{TH} shifting using simulations performance at gate-length 9.7 nm, adequate oxide thickness of 0.56 nm [69]. The most crucial observation reported was the extreme suppression of SCEs using a double-gate compared to the single-gate by tuning the work function to trigger subthreshold characteristics.

2.5. Motivation

The detailed literature review accomplishes that several innovative device design geometries, architectures, and modifications in the transistor have been developed using simplified and compact modeling to mitigate device scaling challenges.

The GAA and SG structure have a close match with CSDG MOSFET device geometry for the analytical approach, and the corresponding insights can be well-treated with CSDG

MOSFET with appropriate boundary conditions for analyzing device physics and electrical characteristics.

The availability of contemporary computational, analytical model and simulation tools provides significance in early detection and prediction of device characteristics without going through the expensive and long fabrication cycle. There have been plenty of efforts that have been done to explore gate-material engineering with different short-channel MOS structures in recent years, yet the analysis of CSDG MOSFET device physics has an excellent opportunity to improve device characteristics.

An appropriate analysis of device modeling of the electric field, gate-capacitance, and surface-potential is essential to include the benefit of gate material engineering. The enhanced device characteristics are expected using a dual-material structure in CSDG MOSFET is promising and can reduce the threshold voltage roll-off, overcome HCEs, and Short-channel effects (SCEs).

Chapter-3

CAPACITANCE ANALYSIS OF CSDG MOSFET AT PINCH-OFF

The gate-capacitance parameter of CSDG be vital in the role and drive the electrical performance. Moreover, the saturation region of a MOSFET, which is beyond gradual channel approximation [70], introduced by Shockley [71], has been a challenging region to analyze. It becomes imperative to know the device behavior at pinch-off for switching response of the device operation. Although capacitance parameters have been significantly discussed in the past, particularly to the CSDG structure, the oxide capacitance formation and its contribution to the overall capacitance appear essential. The oxide capacitance is a crucial parameter that influences the device's switching characteristics and the applications in high frequency, and RF switching is greatly affected due to the capacitance [72].

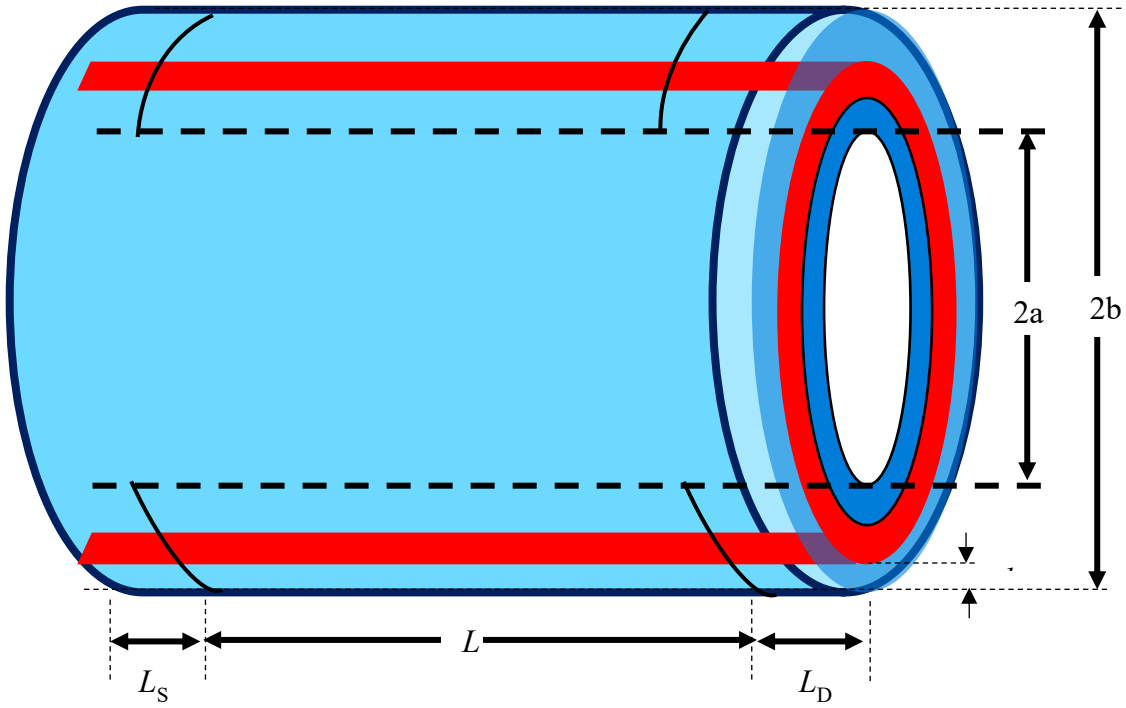
In this chapter, a physics-based analysis of gate-oxide capacitance of Cylindrical Surrounding Double-gate (CSDG) MOSFET has been presented at device pinch-off condition [73-75]. The analogy of gate-capacitance for the Cylindrical Surrounding Double-Gate MOSFET operating in saturation has been considered.

3.1. Gate-Capacitance in CSDG MOSFET

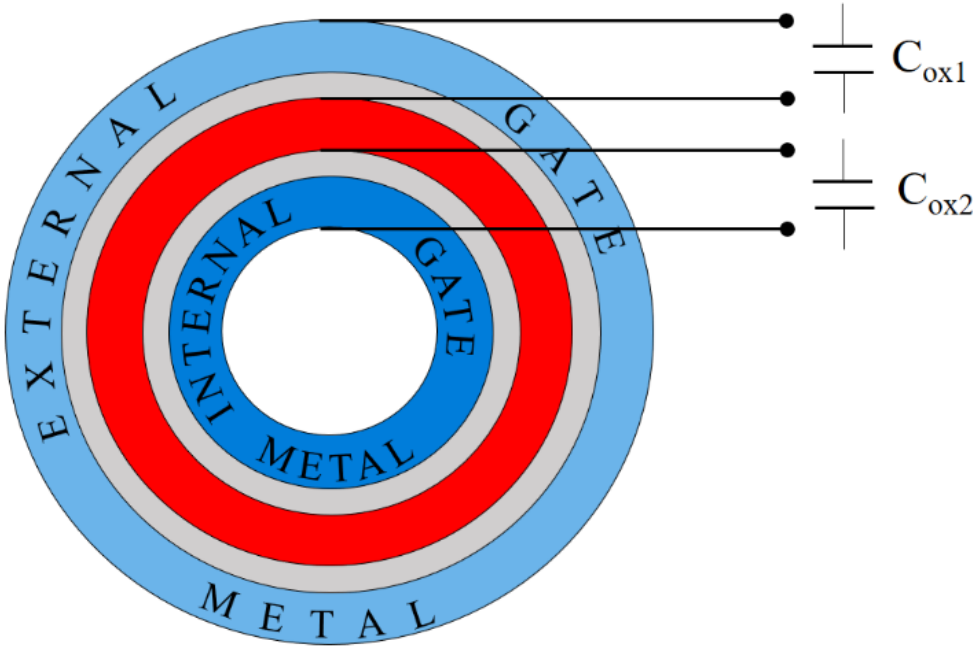
The double-gated (DG) MOSFET is the starting point of realizing the model of the CSDG MOSFET. If the DG MOSFET is rotated by 360^0 to turn up in the form of a cylinder, it becomes CSDG MOSFET. The structure of CSDG similar to those of the DG MOSFET; however, the analysis differs as the cylindrical coordinates system is most suitable for performing the study for the newly generated structure. Fig. 3.1(a) shows the structural description of the CSDG device, where the internal and the external gate has radius are a and b, respectively.

The CSDG structure has a double-gate, which forms two capacitances due to the oxide between the metal-semiconductor electrodes. These two capacitors are concentric to each other. Fig. 3.1 (b) shows the cross-section of the CSDG MOSFET cylinders. For the ease of analysis same gate-oxide materials of thickness, t_{ox} was assumed for both the gates of

the CSDG MOSFET. The capacitance C_{ox1} and C_{ox2} exist between the internal and external gate metal-oxide-semiconductor layers, respectively.



(a)



(b)

Fig. 3.1. The geometry of (a) a CSDG MOSFET structure, and (b) representation of oxide capacitance in CSDG MOSFET [28].

As the exceeding value of drain to source voltage (V_{DS}) above overdrive voltage (V_{OV}), i.e., pinch-off, it reduces the channel depth into a triangular shape from a regular homogeneous shape, sloping down from source to drain along the length [76,77]. The CSDG MOSFET is a cylindrical structure, so the channel is homogeneously surrounded. However, it applies only before the pinch-off condition is reached.

3.2. Analysis of Oxide Capacitance

Based on the analogy of gate-capacitance, Cylindrical Surrounding Double-Gate MOSFET can be analyzed in saturation conditions mainly. It is noteworthy that the channel does not follow uniformity at the increased saturation regime, hence considering the device capacitive structure to be cylindrical goes erroneous. Instead, the channel takes a truncated conical shape, which accounts for the device's gate-capacitance more accurately.

It is noteworthy that beyond pinch-off, the CSDG channel would assume a truncated cone shape for each gate individually, as shown in Fig. 3.2 and Fig. 3.3. Deriving the truncated conical shape's capacitance would result in oxide capacitance of CSDG MOSFET at pinch-off, which have been analyzed in the subsequent sections.

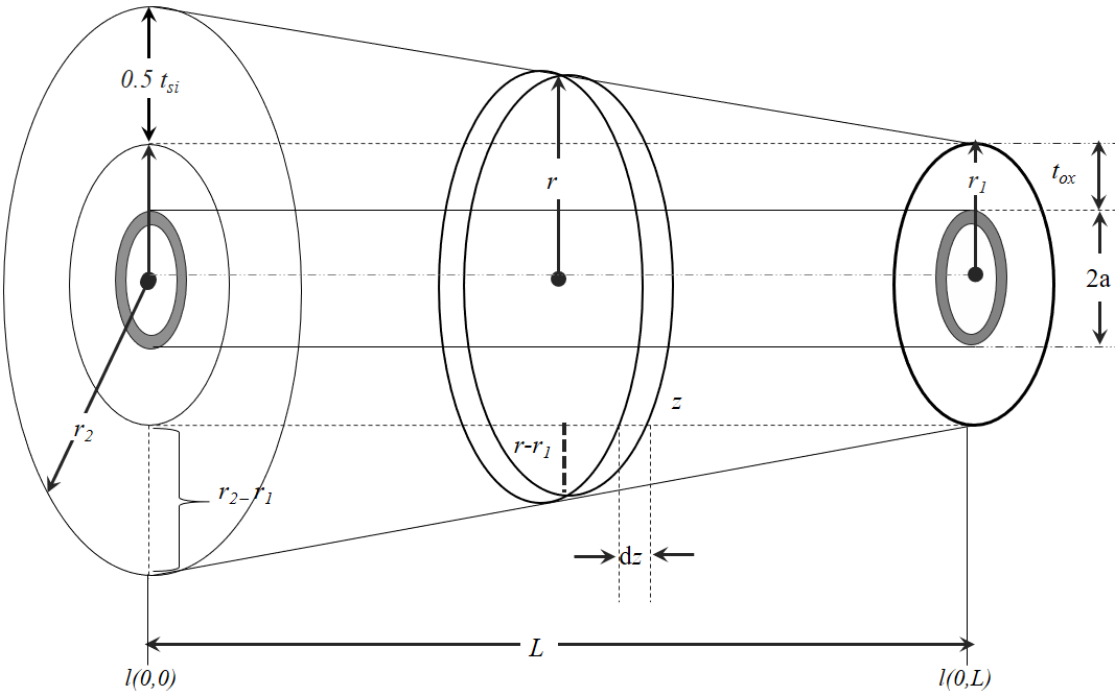


Fig. 3.2. Calculation of internal gate-oxide capacitance at pinch-off.

3.3. Oxide Capacitance of the Internal Gate

Considering the internal gate metal having radius *a* and thickness of oxide around the metal is $t_{ox.}$ So truncated cone shape channel in semiconductor, oxide, and internal gate metal forms a capacitor. We need to analyze the internal gate-oxide capacitance at a pinch-off point. t_{si} is the thickness of the semiconductor.

Referring to Fig. 3.2, radius r_1 is varied from the axis point *l* (0, 0) to the highest point at the right-hand side end *l* (0, *L*). It is to note that:

1) At *l*=0, Truncated cone radius $r_1 = \mathrm{a} + t_{ox}$;
2) At *l*=*L*, Truncated cone radius $r_2 = \mathrm{a} + t_{ox} + t_{si}/2$;

For deducing the expression, this truncated cone has been divided into annuli of segment length *dz*, which forms infinitesimal capacitances of annuli width *dz*. Therefore, all the annuli capacitors are arranged in parallel. So infinitesimal incapacitance of such annuli [78] is:

$$dD = \frac{1}{\varepsilon_0} \frac{dz}{\pi(r^2 - \mathrm{a}^2)} \tag{3.1}$$

where *D* is the inverse of capacitance (incapacitance of the capacitor) in Farad^{-1}. Using the property of similarity of the triangles depicted in Fig. 3.2 [79, 80]:

$$\frac{z}{L} = \frac{r - r_1}{(r_2 - r_1)} \text{ also, } dz = \frac{L}{(r_2 - r_1)} dr \tag{3.2}$$

Substituting Eq. (3.2) into Eq. (3.1):

$$dD(r) = \frac{1}{\pi\varepsilon_0} \left(\frac{L}{r_2 - r_1} \right) \frac{dr}{(r^2 - \mathrm{a}^2)}$$

$$= \frac{1}{2\pi\varepsilon_0 \mathrm{a}} \left(\frac{L}{r_2 - r_1} \right) \left(\frac{1}{r - \mathrm{a}} - \frac{1}{r + \mathrm{a}} \right) dr \tag{3.3}$$

Integrating Eq. (3.3) for the radius range from r_1 to r_2 will be written as:

$$D_1^{'}(r) = \frac{1}{2\pi\varepsilon_0 \mathrm{a}}\left(\frac{L}{r_2 - r_1}\right)\int_{r_1}^{r_2}\left(\frac{1}{r-\mathrm{a}} - \frac{1}{r+\mathrm{a}}\right)dr$$

$$D_1 = \frac{1}{2\pi\varepsilon_0 \mathrm{a}}\left(\frac{L}{r_2 - r_1}\right)\left[\ln\frac{r_2-\mathrm{a}}{r_2+\mathrm{a}} - \ln\frac{r_1-\mathrm{a}}{r_1+\mathrm{a}}\right] \tag{3.4}$$

Substituting $r_1 = \mathrm{a} + t_{ox}$ and $r_2 = \mathrm{a} + t_{ox} + t_{si}/2$ in Eq. (3.4), yields:

$$D_1 = \frac{L}{\pi\varepsilon_0 \mathrm{a}.t_{si}}\left[\ln\left\{\left(\frac{t_{ox}+0.5t_{si}}{2\mathrm{a}+t_{ox}+0.5t_{si}}\right)\left(1+\frac{2\mathrm{a}}{t_{ox}}\right)\right\}\right]$$

$$C_{ox(\mathrm{int})} = \frac{1}{D_1} = \frac{2\pi\varepsilon_0 \mathrm{a}}{L}\frac{0.5t_{si}}{\ln\left\{\left(\frac{t_{ox}+0.5t_{si}}{2\mathrm{a}+t_{ox}+0.5t_{si}}\right)\left(1+\frac{2\mathrm{a}}{t_{ox}}\right)\right\}} \tag{3.5}$$

If $r_2 = r_1$, i.e., cylindrical shape, D_1 appears to be infinity, and capacitance can be calculated using L' Hospital's rule [81]:

$$D_1^{'} = \frac{L}{2\pi\varepsilon_0 \mathrm{a}}\lim_{r_2 \to r_1}\left[\ln\frac{r_2-\mathrm{a}}{r_2+\mathrm{a}} - \ln\frac{r_1-\mathrm{a}}{r_1+\mathrm{a}}\right]$$

$$C_1^{'} = \frac{\pi\varepsilon_0(r_1^2 - \mathrm{a}^2)}{L}$$

where C_1' represents the capacitance of a plane capacitor due to internal, which is a general capacitor formula.

3.4. Oxide Capacitance of the External Gate

The oxide capacitance in the external gate radius 'b' arrangement, at the pinch-off condition slanted channel in the cylindrical semiconductor, would form Residual Truncated Cone (RTC) shape. So, the external gate-capacitance at pinch-off can be

calculated by subtracting the Virtual Truncated Cone (VTC) capacitance out of an exterior cylindrical capacitor as it follows the superposition principle of capacitances.

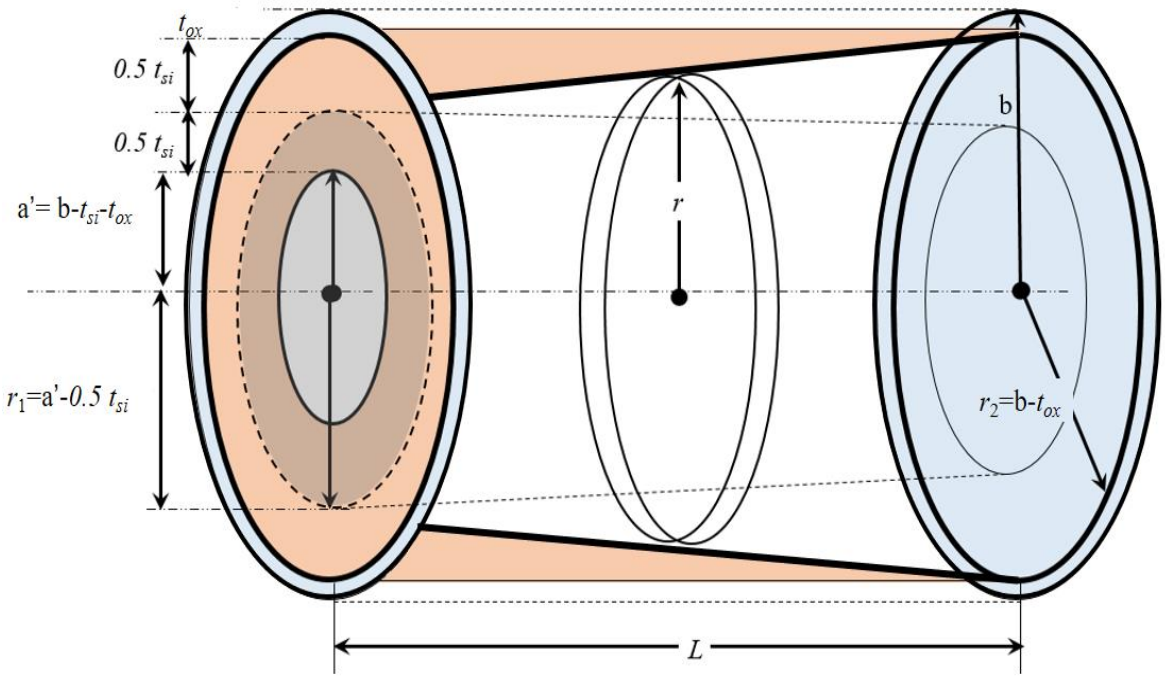


Fig. 3.3. Calculation of external gate-oxide capacitance at pinch-off.

The resultant would display the oxide capacitance for an external gate. If the external cylindrical capacitor has outer and inner electrode radius of b and a + t_{si} + t_{ox}, respectively. The exterior cylindrical capacitance can be given as [21]:

$$C_{exterior} = \frac{2\pi\varepsilon_o L}{\ln\left(\frac{\mathrm{b}}{\mathrm{a}+t_{si}+t_{ox}}\right)} \tag{3.6}$$

The residual truncated cone capacitance would be:

$$C_{ox(\mathrm{ext})} = C_{\mathrm{RTC}} = C_{exterior} - C_{\mathrm{VTC}} \tag{3.7}$$

So, first the virtual truncated cone capacitance (C_{VTC}) is calculated using the same principle as in section 3.3, where dimensions for truncated cone, are shown in Fig. 3.3.

For determining D_2, substituting the value of a', r_1, and r_2 as (b-t_{si}-t_{ox}), (a'+0.5t_{si}), and (b-t_{ox}) in Eq. (4), respectively, in accordance with Fig. 3.3.

$$D_2 = \frac{L}{2\pi\varepsilon_0(\mathrm{b}-t_{si}-t_{ox})(\mathrm{b}-t_{ox}-\mathrm{a}'-0.5t_{si})}\ln\left[\frac{\left(\frac{t_{si}}{2\mathrm{b}-t_{si}-2t_{ox}}\right)}{\left(\frac{0.5t_{si}}{2\mathrm{b}-1.5t_{si}-2t_{ox}}\right)}\right]$$

$$C_{VTC} = \frac{1}{D_1} = \frac{\pi\varepsilon_0(\mathrm{b}-t_{si}-t_{ox})}{L}\times\frac{t_{si}}{\ln\left(\frac{2\mathrm{b}-1.5t_{si}-2t_{ox}}{\mathrm{b}-0.5t_{si}-t_{ox}}\right)}$$

Substituting values of C_{VTC} from Eq. (3.8) and $C_{exterior}$ from Eq. (3.6) into Eq. (3.7) results in external capacitance $C_{ox(\mathrm{ext})}$=C_{RTC} can be given as Eq. (3.9)

$$C_{ox(\mathrm{ext})} = C_{RTC} = \frac{2\pi\varepsilon_o L}{\ln\left(\frac{\mathrm{b}}{\mathrm{a}+\mathrm{t_{si}}}\right)} - \frac{\pi\varepsilon_o(\mathrm{b}-\mathrm{t_{si}}-\mathrm{t_{ox}})}{L}\times\frac{\mathrm{t_{si}}}{\ln\left(\frac{2b-1.5\mathrm{t_{si}}-2\mathrm{t_{ox}}}{b-0.5\mathrm{t_{si}}-\mathrm{t_{ox}}}\right)} \tag{3.9}$$

Overall Oxide capacitance of CSDG MOSFET at a pinch-off condition can be given as:

$$\frac{1}{C_{ox(\mathrm{CSDG})}} = \frac{1}{C_{ox(\mathrm{ext})}} + \frac{1}{C_{ox(\mathrm{int})}}$$

$$C_{ox(\mathrm{CSDG})} = \frac{C_{ox(\mathrm{ext})}C_{ox(\mathrm{int})}}{C_{ox(\mathrm{ext})}+C_{ox(\mathrm{int})}}$$

$$C_{ox(\mathrm{CSDG})} = \frac{\frac{\mathrm{a}\pi\varepsilon_0 t_{si}}{L.\ln\left\{\left(\frac{t_{ox}+0.5t_{si}}{2\mathrm{a}+t_{ox}+0.5t_{si}}\right)\left(1+\frac{2\mathrm{a}}{t_{ox}}\right)\right\}}\left[\frac{2\pi\varepsilon_0 L}{\ln\left(\frac{\mathrm{b}}{\mathrm{a}+t_{si}}\right)} - \frac{\pi\varepsilon_0(\mathrm{b}-t_{si}-t_{ox})t_{si}}{L\ln\left(\frac{2b-1.5t_{si}-2t_{ox}}{b-0.5t_{si}-t_{ox}}\right)}\right]}{\frac{\mathrm{a}\pi\varepsilon_0 t_{si}}{L.\ln\left\{\left(\frac{t_{ox}+0.5t_{si}}{2\mathrm{a}+t_{ox}+0.5t_{si}}\right)\left(1+\frac{2\mathrm{a}}{t_{ox}}\right)\right\}} + \left[\frac{2\pi\varepsilon_0 L}{\ln\left(\frac{\mathrm{b}}{\mathrm{a}+t_{ox}}\right)} - \frac{\pi\varepsilon_0(\mathrm{b}-t_{si}-t_{ox})\mathrm{t_{si}}}{L\ln\left(\frac{2b-1.5t_{si}-2t_{ox}}{b-0.5t_{si}-t_{ox}}\right)}\right]} \tag{3.10}$$

The resulting equation, as expressed in Eq. (3.10), contains the Cylindrical Surrounding Double-Gate MOSFET's internal and external capacitor structure. The capacitance CSDG is a function of structure dimensions (length of the channel (L), internal and external gate radius (a, b) and also depends on the thickness of silicon and oxide (t_{ox} and t_{si}) of the device structure. In the analysis, free-space is assumed for both the capacitor assembly with free space permittivity ε_0. In the real situation of CSDG MOSFET, the type of dielectric material used would affect the overall result.

3.5. Chapter Summary

As detailed in chapter 2, the primary objective of exercising gate material engineering is to lower the threshold voltage and threshold voltage roll-off; therefore, it becomes imperative for closer integration of capacitance (at pinch-off) in smaller device dimensions. Consequently, this chapter presents a mathematical analysis of the oxide capacitance of CSDG MOSFET, which originates at the pinch-off.

The resulting expression reveals that the capacitance at pinch-off is not a direct rationale of cylindrical sizes of the device; instead, it takes a complex algebraic and logarithmic fractional form as resulted in the expression, which is comprised of the external, internal dimensions, thickness, and material properties of the capacitive layer in the CSDG structure.

As CSDG MOSFETs have been reported for high-frequency applications for high speed, data transmission, antenna, sensor networks, and RF circuits, the proposed work could add a more in-depth insight into the analytical understanding of the capacitance formation in a CSDG MOSFET to incorporate in ongoing research. Further, the impact of the resulted capacitance expression and comparison with previously reported literature can be analyzed to discriminate future work's influence.

Chapter-4

ELECTRICAL FIELD ANALYSIS IN CSDG MOSFET

This chapter details the electrical field analysis in Cylindrical Surrounding Double-Gate (CSDG) MOSFET using the physics of surface-potential, threshold voltage, and gate-oxide capacitances. The CSDG structure has been viewed as two individual separate capacitor assembly to calculate each gate's electric field in the analysis. After that, field vector summation results in an expression that concludes the overall electric field due to oxide capacitances.

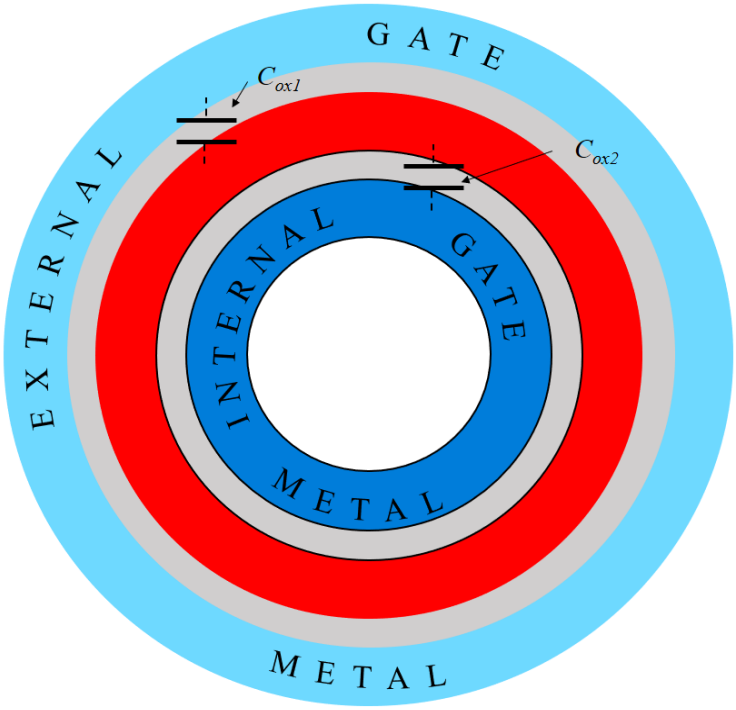
The electric field distribution due to metal junction in the DMG-CSDG structure would be required to interpret the results of the impact on carrier transport efficiency in the presented research work of this thesis. Furthermore, the electric field estimates the channel mobility that describes electrical device parameters [82-84]. Integration of ring analysis has been used for deriving the expression of the overall electric field of the CSDG structure.

The electric field in the semiconductor channel describes the channel's charge carrier mobility, while the mobility is a function of drift velocity. Besides, the electric field at any channel region is the lateral and longitudinal electric field component's vector sum in the current flow direction [85-87]. Therefore, it is worth mentioning that the electric field components can substantially change the mobility, charge carrier velocity, and provide a high drain current. Based on the peak electric field's existence, shifting the rise towards the source/drain side and the field distribution along the channel length for the device structure and dimension can consequently comprehend the device behavior.

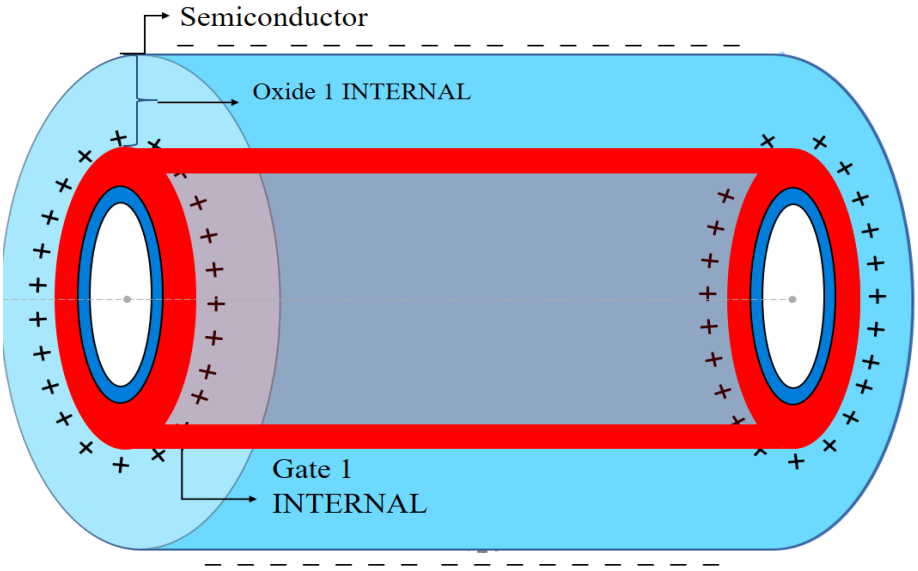
4.1. Electric Field in CSDG Due to Oxide Capacitances

As the name suggests, the Cylindrical Surrounding Double-gate (CSDG) MOSFET is comprised of two gates conceptualized from a basic Double-Gated (DG) MOSFET shaped into a cylindrical structure. The DG MOSFET's top and bottom gates form two metallic cylinders separated by semiconductors channel of radius a and b. Further, each of the external and internal metal cylinders is isolated from the gate insulators. Therefore, a

typical CSDG MOSFET creates two oxide capacitances, namely C_{ox1} and $C_{ox2,}$ between the internal, external gate, and the metal-oxide-semiconductor layers, as indicated in the cross-section of the device shown in Fig. 4.1(a).



(a)



(b)

Fig. 4.1. Illustration of CSDG structure (a) oxide-capacitances and (b) surface and the field charges.

The mathematical analysis of the origin of charges and capacitance of CSDG MOSFET structure has been discussed in the previous chapter. The oxide capacitances develop the charge that creates the electric fields in the structure's surrounding [88], as shown in Fig. 4.1(b). In other words, the capacitors C_{ox1} and C_{ox2} store the electrostatic energy using the storage of electric charge on two cylindrical electrodes (metal/semiconductor) and build up an electric field between the space, i.e., oxide in CSDG MOSFET.

4.2. Theory of Electric Field in CSDG MOSFET

The electric field analysis is based on the capacitive field generated due to the capacitor's charge [89]. The developed electric field causes a net positive charge to collect on the metal and a net negative charge on either side of the gate assembly in the semiconductor of CSDG MOSFET. The electric field of the overall CSDG structure would assume field vector aggregation due to the individual cylindrical capacitors. For ease of analysis, the same gate-oxide materials and thickness (t_{ox}) are considered for both the gates of the CSDG MOSFET. The 2D structure of CSDG MOSFET is similar to those of the DG MOSFET. However, the analysis differs as the cylindrical coordinates system is most suitable for studying the newly designed structure.

The electric field analysis due to oxide capacitance in CSDG MOSFET evolves with its structure that has a combination of two cylindrical capacitors. For reducing the difficulty, each capacitor has been considered separately for deducing electric field expression. Fig. 4.2 Shows the representation of CSDG structure with electric field develops in the cylindrical cores. As the Surface-Potential ϕ_s depends on the applied $V_{GS,}$ charges are produced on the gate metal electrode and semiconductor electrodes. With the positive gate voltage (V_{GS1}) used at the internal gate, positive charges are uniformly spread over the oxide-semiconductor interface's cylindrical surface.

4.3. Derivation of the Electric Field Analysis in CSDG MOSFET

A cylindrical structure can be considered as consisting of infinitesimally small circular rings of uniform charge density ρ_l and radius 'a' as shown in Fig. 4.2. The charges on both the cylinders are equal in magnitude but have opposite polarities surrounding the metallic

cylinders' surface, and the inverted charges are available about the semiconductor cylinder. The two-dimensional Poisson's equation adequately defines the potential distribution in a uniformly doped cylindrical channel before the inception of inversion [90, 91].

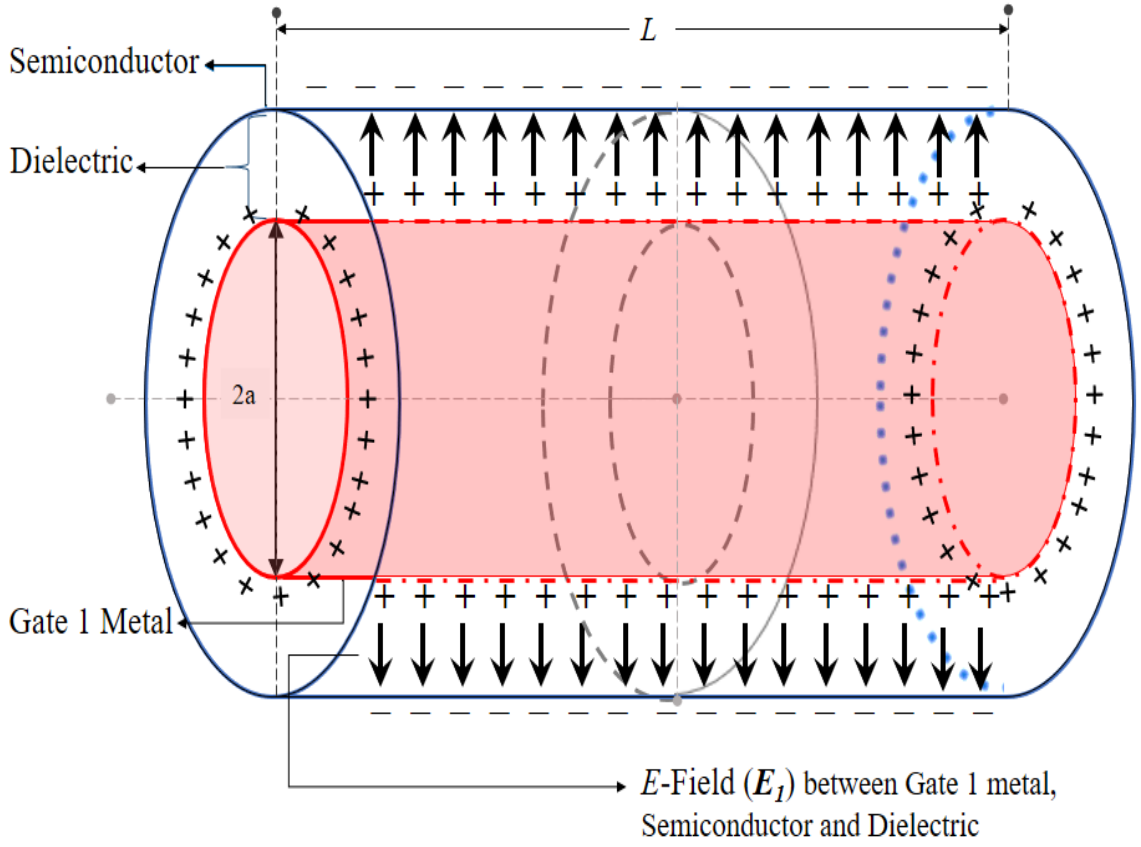


Fig. 4.2. Schematic of cylindrical metal-oxide-semiconductor structure.

In setting up this analysis, it has been assumed that the channel is unaffected by the carrier concentration, charge carriers, and fixed oxide charges. The solution of the Poisson's equation results in a parabolic form of general solution [92]; therefore, the potential profile in the direction perpendicular to the channel could be used for deriving the Surface-Potential as:

$$\phi_s(z) = Ae^{\lambda z} + Be^{-\lambda z} - \frac{\beta}{\lambda^2} \tag{4.1}$$

where, the minima of Surface-Potential occurs at $z = z_{min} = (1/2\lambda)\ln(B/A)$ which results $\phi_{s,min} = 2(AB)^{1/2} - (\beta/\lambda^2)$. Usually, the electrostatic analysis is done in radial direction

only, but it can be applied to the results at $z = z_{max}$ to realize our structure at the specific point (virtual cathode); the mobile charge primarily is controlled by the electric field along the *r*-direction. The virtual cathode's mobile charge sheet density is controlled by the gate electrode [93, 94], and the charge *Q* associated is given in Eq. (4.2).

$$Q = C_{ox}(V_{GS} - \Delta\psi - \phi_s) \tag{4.2}$$

$$\text{where } C_{ox} = 2\varepsilon_{ox} / t_{si} \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right);$$

Moreover, $\Delta\psi$, V_{GS}, and ϕ_s are the work-function difference between the gate electrode and semiconductor, applied gate-source potential, and the device's Surface-Potential.

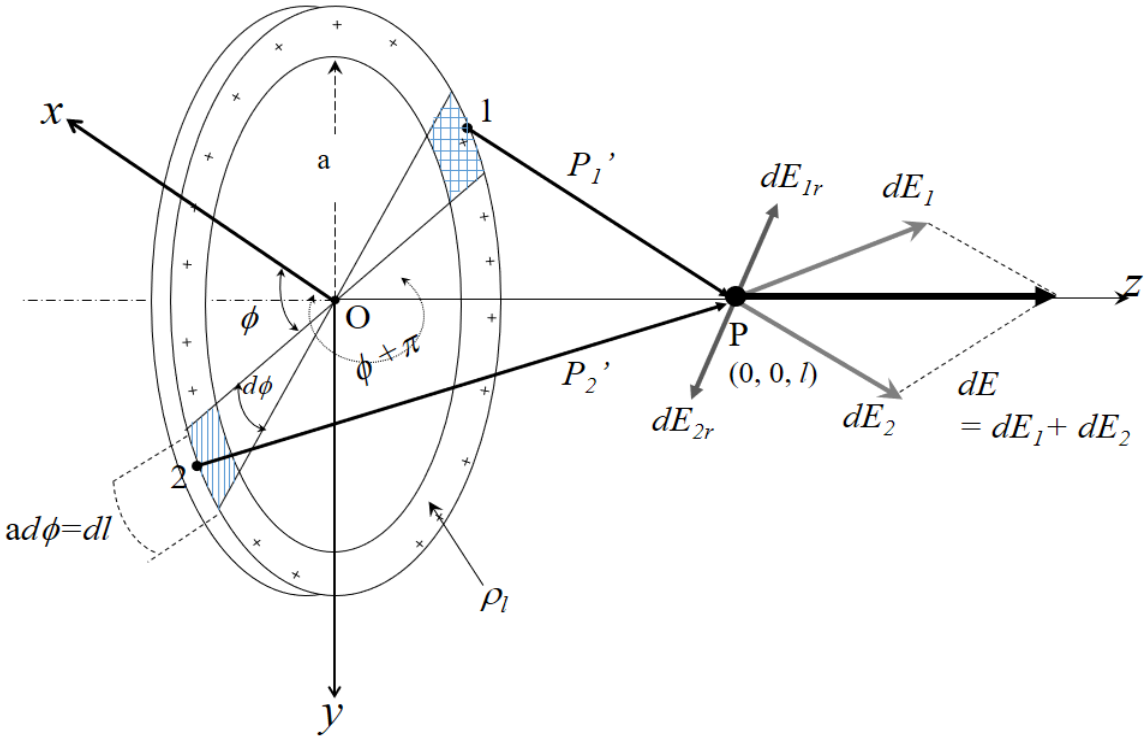


Fig. 4.3. Electric field due to uniformly charged ring for calculating electric field along the length.

The integral of field analysis of a ring along the z-axis at point P (*0, 0, l*) can be an obvious choice for the solution of *E*-Field in a cylindrical geometry of the CSDG. The differential charge segment length $dl = ad\phi$ and the differential charge density is $dQ = \rho_l d\phi$.

At that time, the vector *P'* is pointing from the differential charge towards the field point *P* is given as:

$$P' = -\hat{r}\,\mathrm{a} + \hat{z}\,l$$

$$\left|P'\right| = \sqrt{\mathrm{a}^2 + l^2}$$

$$\hat{\mathrm{P}}' = \frac{\mathrm{P}'}{\left|\mathrm{P}'\right|} = -\frac{\hat{r}\,\mathrm{a} + \hat{z}\,l}{\sqrt{\mathrm{a}^2 + l^2}}$$

where $\hat{\mathrm{P}}'$ is the corresponding unit vector, then:

$$dE = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\rho_l \mathrm{a}\frac{-\hat{r}\,\mathrm{a} + \hat{z}\,l}{(\mathrm{a}^2 + l^2)^{3/2}}d\phi \tag{4.3}$$

The charge ring has been divided into two semicircles, where each of them is defined over the angle $0 \le \phi \le \pi$. The radial ($\hat{r}$) field contributed due to charge segments on the opposite sides of the ring cancel, and the remainder is only the axial components. As the axial field components add constructively [95], thus:

$$E_{1l} = \hat{z}\,2 \times \frac{\rho_l \mathrm{a} l}{4\pi\varepsilon_0\varepsilon_r(\mathrm{a}^2 + l^2)^{3/2}}\int_0^{\pi} d\phi$$

$$= \hat{z}\frac{\rho_l \mathrm{a} l}{2\varepsilon_0\varepsilon_r(\mathrm{a}^2 + l^2)^{3/2}} = \hat{z}\frac{l}{4\pi\varepsilon_0\varepsilon_r(\mathrm{a}^2 + l^2)^{3/2}}Q \tag{4.4}$$

where $Q = 2\pi\mathrm{a} \times \rho_l$, is the total charge on the ring. Now, by dividing the area into such infinitesimally thin rings of thickness *dl*, the effective electric field in the structure at distance *l* (Point P) regions can be determined, as shown in Fig. 4.3.

$$E_1 = \hat{z}\frac{\rho_l \mathrm{a}}{2\varepsilon_0\varepsilon_r}\int_0^{L} \frac{l dl}{4\pi(\mathrm{a}^2 + l^2)^{3/2}} \tag{4.5}$$

The solution of Eq. (4.5) results as given in Eq. (4.6).

$$E_1 = \hat{z}\frac{\rho_l}{2\varepsilon_0\varepsilon_r}\left[1-\frac{\mathrm{a}}{(\mathrm{a}^2+L^2)^{1/2}}\right] \tag{4.6}$$

also for $L > 0$, $E_1 = \hat{z}\dfrac{\rho_l}{2\varepsilon_0\varepsilon_r}\left[1-\dfrac{|L|}{\sqrt{\mathrm{a}^2+L^2}}\right]$

4.4. Results Analysis

To obtain the electric field in terms of the charge Q, Eq. (4.6) is extended by replacing $\rho_l /(2\varepsilon_0\varepsilon_r)$ in $Q/(\pi\varepsilon_0\varepsilon_r\mathrm{a}^2)$ as:

$$E_1 = \hat{z}\frac{Q_1}{4\pi\varepsilon_0\varepsilon_r\mathrm{a}}\left[1-\frac{\mathrm{a}}{(\mathrm{a}^2+L^2)^{1/2}}\right] \tag{4.7}$$

$$= \hat{z}\frac{Q}{2\pi\varepsilon_0\varepsilon_r\mathrm{a}^2}\left[1-\frac{|L|}{\sqrt{\mathrm{a}^2+L^2}}\right], L>0$$

By assuming $L >>$ a, and then using binomial expansion,

$$E_1 = \frac{\hat{z}\,Q_1L^2}{8\pi\varepsilon_0\varepsilon_r\mathrm{a}^3} = \frac{\hat{z}\,L^2}{8\pi\varepsilon_0\varepsilon_r\mathrm{a}^3}\frac{2\varepsilon_{ox}(V_{GS1}-\Delta\psi-\phi_s)}{t_{si}\ln\left(1+\dfrac{2t_{ox}}{t_{si}}\right)} \tag{4.8}$$

As shown in Fig. 4.1(b), the external gate (Gate metal 2) also surrounds the semiconductor and forms cylindrical capacitance C_{ox2} of radius b having charge Q_2 at applied positive outer gate voltage (V_{GS2}).

Similar to Eq. (4.8), the electric field in the external metal-oxide-semiconductor capacitor, E_2 can be given as:

$$E_2 = \frac{\hat{z}\,Q_2L^2}{8\pi\varepsilon_0\varepsilon_r\mathrm{b}^3} = \frac{\hat{z}\,L^2}{8\pi\varepsilon_0\varepsilon_r\mathrm{b}^3}\frac{2\varepsilon_{ox}(V_{GS2}-\Delta\psi-\phi_s)}{t_{si}\ln\left(1+\dfrac{2t_{ox}}{t_{si}}\right)} \tag{4.9}$$

Therefore, the resulting electric field in CSDG structure due to oxide capacitance is a vector summation of E_1 and E_2, i.e., $\boldsymbol{E} = \boldsymbol{E}_1 + \boldsymbol{E}_2$.

The resulting electric field of this analysis can be written as given in Eq. (4.10).

$$E = \frac{2\varepsilon_{ox}}{t_{si}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)} \frac{\hat{z}\,L^2}{8\pi\varepsilon_0\varepsilon_r} \times \left[\left\{\left(\frac{1}{a^3}\right)(V_{GS1} - \Delta\psi - \phi_s)\right\} + \left\{\left(\frac{1}{b^3}\right)(V_{GS2} - \Delta\psi - \phi_s)\right\}\right] \quad (4.10)$$

The obtained relation is a significant correlation for CSDG MOSFET that depends on applied gate voltages, oxide dielectric constant, square of the channel length, gate metal work function, and Surface-Potential. Besides, the physical dimensions of the semiconductor, oxide, metal involve as the component. The resulting expression also relates oxide properties and suggests that high-*k* oxide materials with higher permittivity would result in a high electric field.

4.5. Chapter Summary

The work presented in this chapter derives the insights into the electric field developed due to the oxide capacitances in a uniformly doped Cylindrical Surrounding Double-Gate MOSFET. The analysis has been founded upon considering the internal and external gate assembly individually. The resulting electric field in the double-gate structure due to the oxide capacitance is a vector sum of the field generated due to the internal capacitor part (E_1), and an external capacitor (E_2) has been analyzed.

The analysis assumes the CSDG cylindrical structure consisting of infinitesimally small circular rings of uniform charge density and dimensions corresponding to the internal and external radius. The presented electric field analysis of Cylindrical Surrounding Double-Gate MOSFET and the mathematical formulation established in this work serves as an essential expression that incorporates the structure design.

The research presented in this chapter could be treated as the foundation of a detailed physical and mathematical model for obtaining channel mobility and electrical

characteristics of the device. The analysis results are significant and can improve channel mobility and other device's electrical performance parameters. It is because of the fact that when a MOSFET is conducted through the channel controlled by suitable gate potential, the induced electric field at the gate terminal affects the electrical characteristics [96-98]. Therefore, it becomes more imperative at the nanoscale, where the channel is too short that the maximum electric field increases and injects electrons to the oxide layer. The situation gives rise to hot carrier injection, which unfortunately requires a high threshold voltage to mitigate the short-channel effects.

Chapter-5

ANALYSIS OF DEPLETION WIDTH IN MOSFET

This chapter presents the analysis to understand the effect of variation in depletion-width (under source, drain, and gate regions) due to different oxide materials and thickness to develop Cylindrical Surrounding thickness modeling Double-gate (CSDG) MOSFET. The obtained results are vital in realizing the dependency of depletion width on oxide properties, which could further be used as a parameter for procuring optimal silicon thickness in a CSDG. The analysis provides a significant guide for the device thickness analysis of metal-oxide-semiconductor structures, followed in this thesis's subsequent chapter.

5.1. Introduction

In the era of highly compact electronics, elementary Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have been phenomenally downscaled of the device size by two orders magnitude over the last four decades [99].

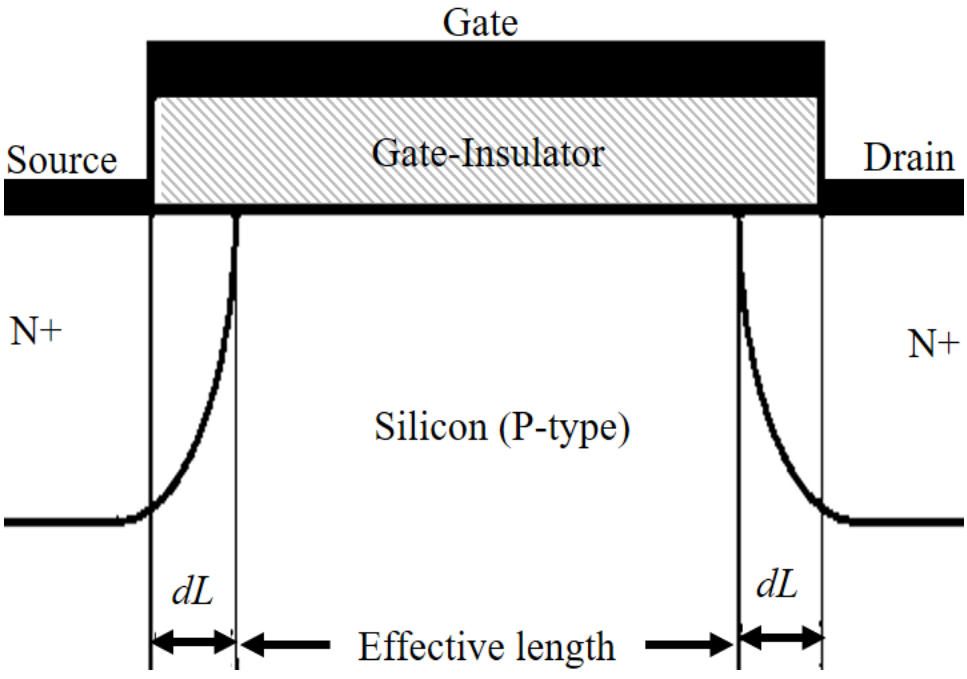


Fig. 5.1. A typical Short channel-MOSFET.

Therefore, it becomes necessary to analyze the parameters which can influence the device scaling and performance at reduced device size. Owing to the scaling, a shorter transistor channel results in an abrupt operation that affects the performance, modeling, and reliability [100].

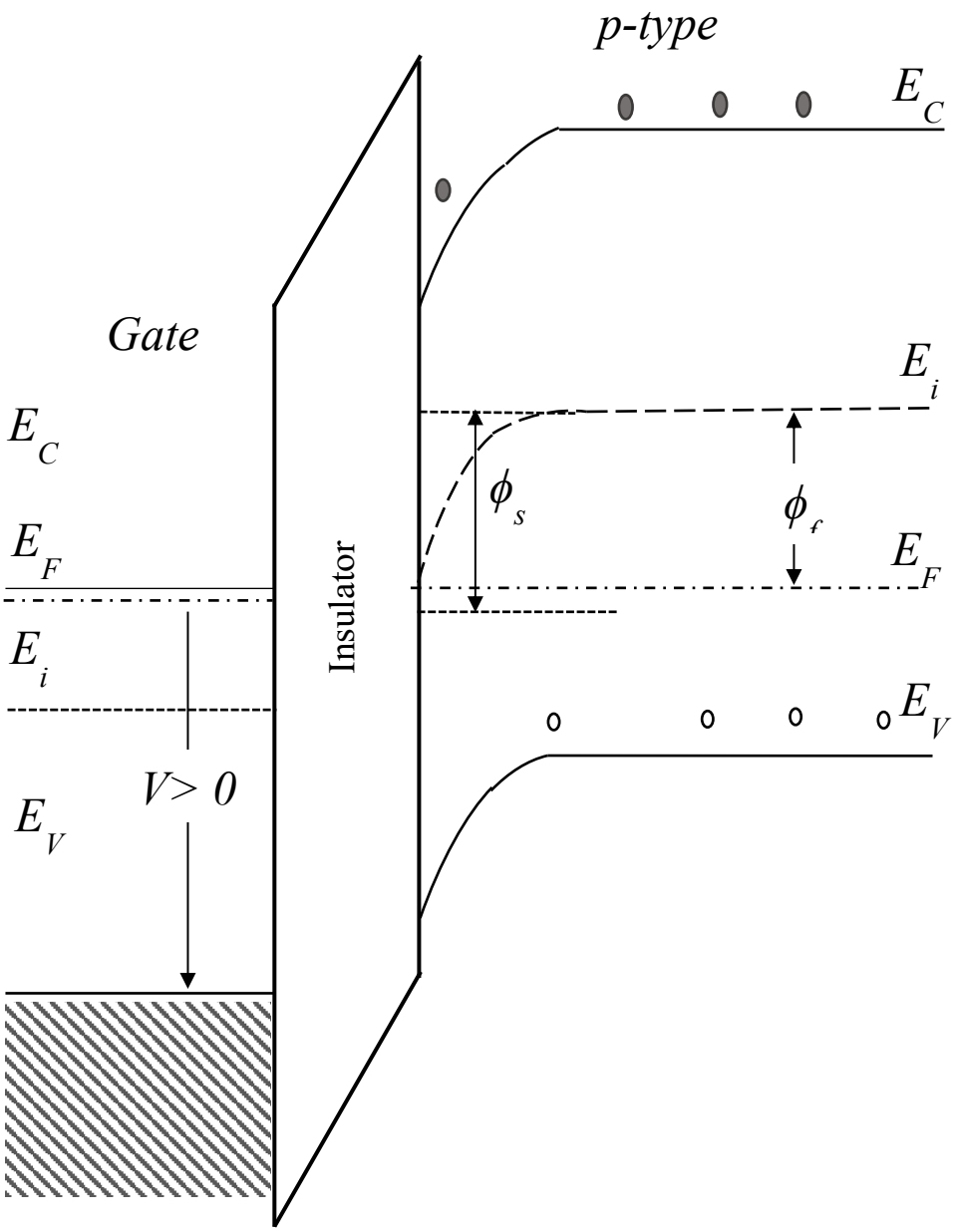


Fig. 5.2. Energy band of MOSFET at depletion.

The CSDG structure has been one among such promising MOSFETs that can withstand even at short-channel up to an extent. Though numerous analysis of CSDG exists, it becomes imperative to analyze the channel to find the improvements from a

typical MOS perspective. Fig. 5.1 shows the schematic representing a short-channel MOSFET wherein the effective channel length ($L_{eff} = L\text{-}2\Delta L$) substitutes the actual channel length [40, 101].

5.2. Depletion width in MOSFET

The junction depletion regions due to diffused source-drain and the depletion region's width are determined from the concentration of substrate doping, Fermi, and Surface-Potentials, as defined by the Dang's model [102, 103].

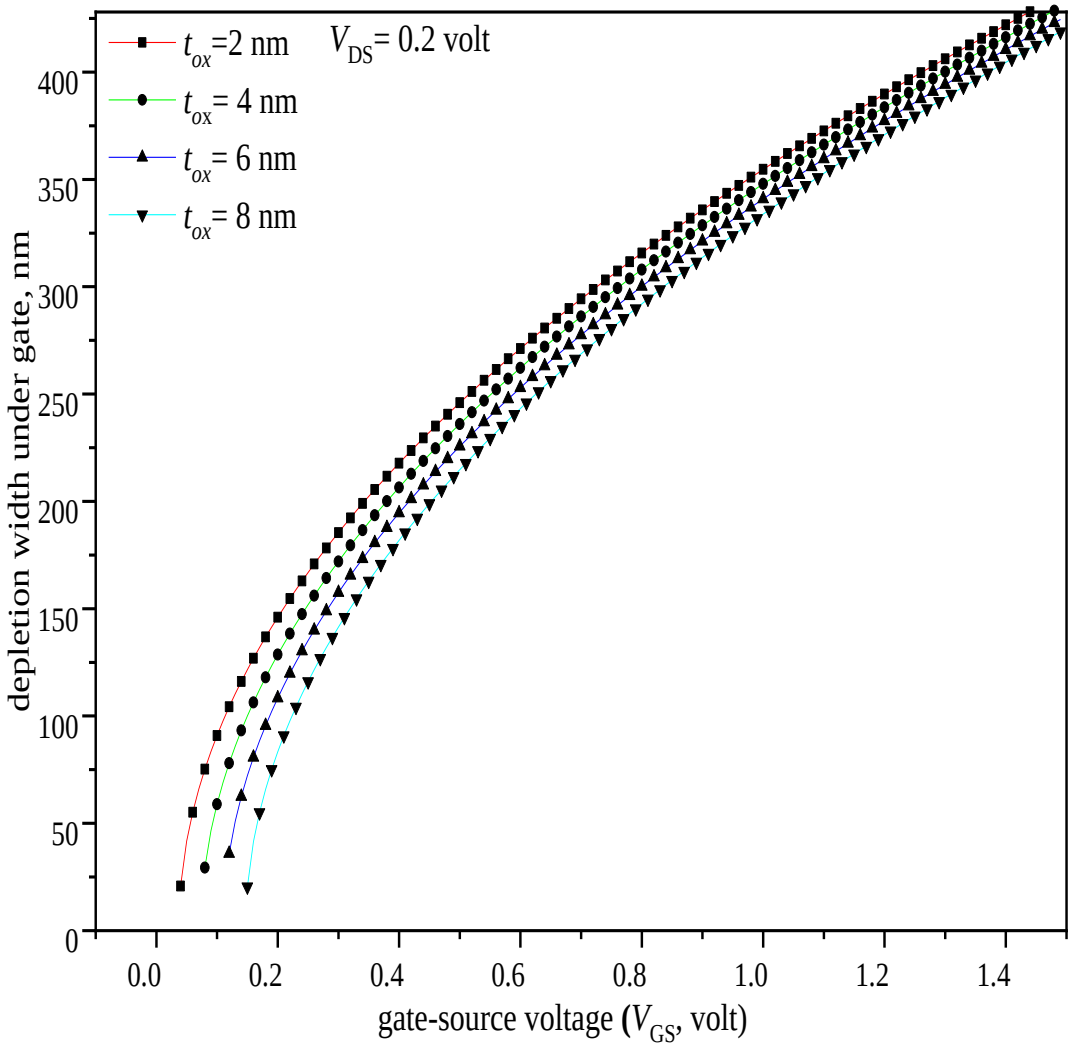


Fig. 5.3. Gate-oxide thickness effect on Depletion width.

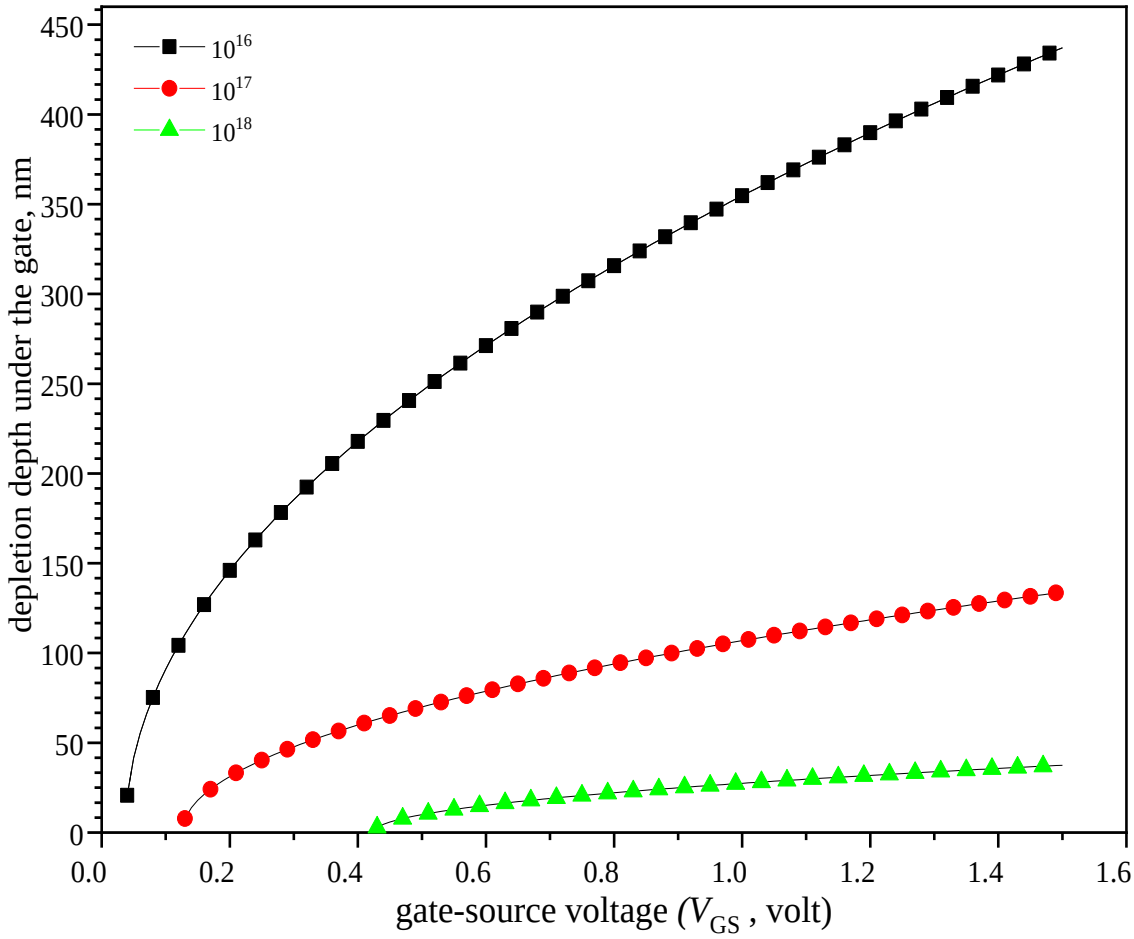


Fig. 5.4. Effect of variation in doping on depletion depth of the device.

The depletion region in a MOSFET structure accounts for the inclusion of the source and drain depletion regions divided primarily into three separate sub-regions as a junction between the diffused source/drain and the substrate, depletion under the channel and by region induced by lateral source and drain diffusions.

The conventional MOSFET band diagram depicting the Fermi energy level at the depletion is shown in Fig. 5.2. Now, the model is built upon the base theory given in the well-known Dang's Model. The optimum or minimum wherein the term is used as the depletion depth, at least, would essentially exist based on the device physics. In the strong inversion of a MOSFET, the depletion depth and charge in the depletion region remain unaffected from $V_{GS.}$

The regions include junction between the diffused source/drain and the substrate, depletion under the channel, and portion induced by lateral source and drain diffusions.

When the device is in operation, the drain and the gate bias initiate inversion and results in bands bending to bring the surface Fermi level closer to the conduction band [104].

5.3. Modeling and Analysis

Once the channel is formed in the device, depletion width under the gate and the drain regions are governed by $\xi(\phi_s - V_{bs}))^{1/2}$ and $\xi(2\phi_s - V_{DS} - V_{bs}))^{1/2}$, respectively, where $\xi = 2\varepsilon_{si}/qN_{sub}$ and ϕ_s, ε_{si}, q, and N_{sub} are the Surface-Potential, permittivity of silicon, electron charge, and the substrate doping concentration, respectively [105-107].

From the two condition device operation, setting up the inversion and gate voltage increase over the threshold cause ϕ_s variation that depends on the gate-oxide thickness and dielectric properties [108]. The variations in the depletion width under the gate region, at the applied gate bias, are represented in Fig. 5.3.

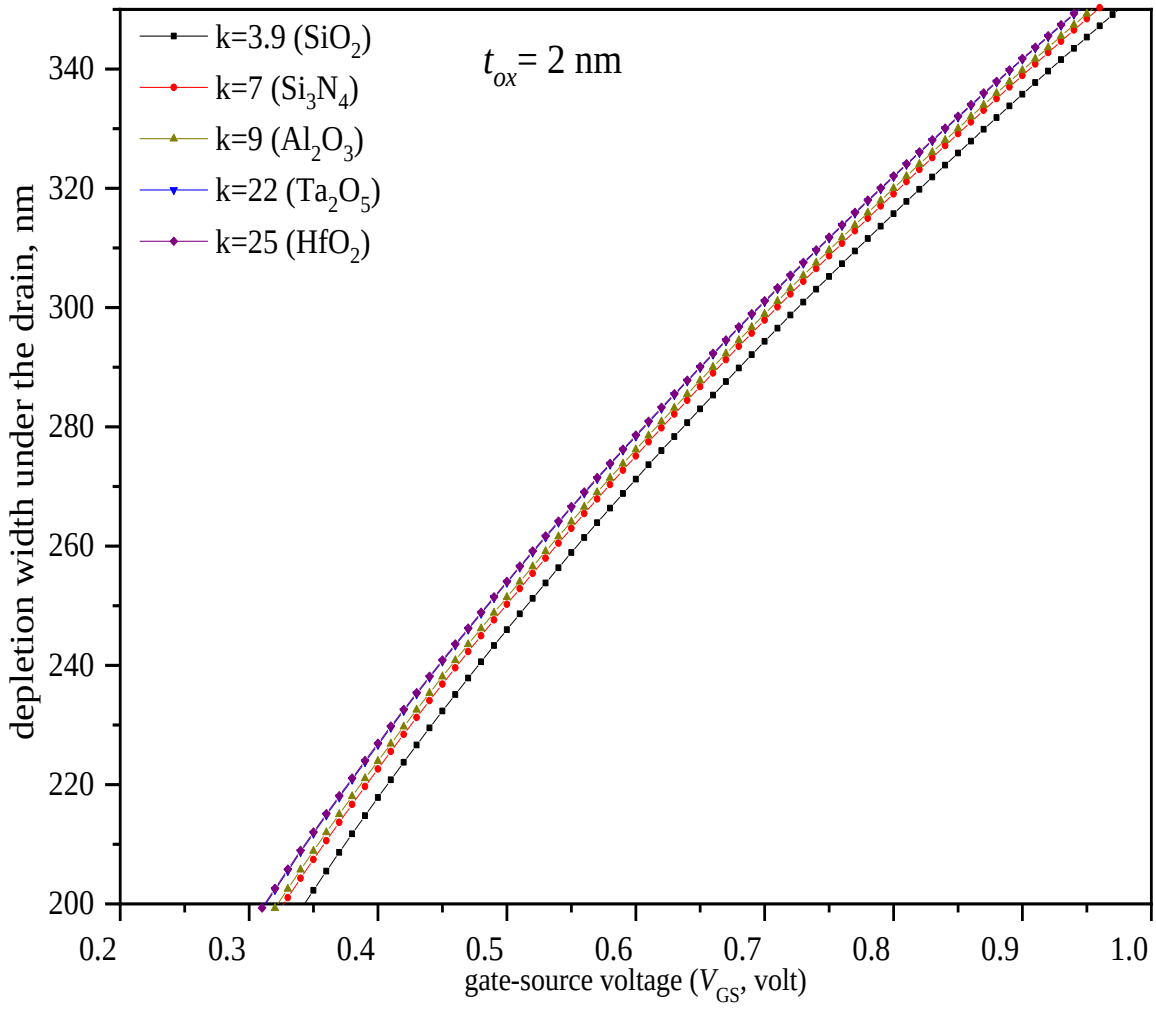


Fig. 5.5. Oxide materials effects on depletion width.

In comparison, the obtained results at gate-oxide thickness 2 *nm*, 4 *nm*, 6 *nm*, and 8 *nm*, respectively, the lowest value of oxide thickness result in relatively larger depletion width. Moreover, the lower thickness also results in high oxide capacitance, which would lower the threshold. Referring to Fig. 5.4, the depletion depth at increasing V_{GS} is minimal compared to large doping concentrations.

Table 5.1 Effect on depletion width due to gate dielectric variation

Gate voltage (volt)	**Depletion width (nm)**				
	k=3.9 (SiO_2)	**k=7 (Si_3N_4)**	**k=9 (Al_2O_3)**	**k=22 (Ta_2O_5)**	**k=25 (HfO_2)**
0.04	20.7616	50.5329	56.0979	66.1379	66.9043
0.12	104.301	114.023	116.596	121.745	122.163
0.2	146.036	153.131	155.056	158.964	159.285
0.28	178.253	184.111	185.715	188.99	189.26
0.36	205.48	210.581	211.986	214.861	215.098
0.44	229.499	234.077	235.341	237.935	238.149
0.52	251.232	255.421	256.58	258.961	259.157
0.6	271.229	275.114	276.19	278.403	278.586
0.68	289.85	293.488	294.497	296.574	296.746
0.76	307.344	310.778	311.731	313.694	313.856
0.84	323.895	327.156	328.061	329.926	330.081
0.92	339.641	342.751	343.616	345.397	345.545
1	354.688	357.668	358.496	360.204	360.345
1.08	369.122	371.986	372.783	374.426	374.562
1.16	383.013	385.774	386.542	388.127	388.258
1.24	396.418	399.086	399.828	401.36	401.487
1.32	409.383	411.967	412.687	414.171	414.294
1.4	421.951	424.458	425.157	426.598	426.717
1.48	434.154	436.592	437.271	438.672	438.788
1.49	435.656	438.085	438.762	440.158	440.274
1.5	437.152	439.573	440.248	441.639	441.755

The effect on depletion width due to gate dielectric variation is tabulated in Table 5.1 which has been shown in Fig. 5.5 for the comparison of performance. The depletion region width at a fixed thickness (t_{ox} = 2 nm) for oxide materials k = 3.9 for silica (SiO_2), k = 7 for Silicon Nitrate (Si_3N_4), k = 9 for Alumina (Al_2O_3) = Alumina, k = 22 for Tantalum Pentoxide (Ta_2O_5), and k =25 for Hafnia (HfO_2) have been exemplified. Primarily, the depletion width under the drain is a significant constituent of required silicon thickness. It is noteworthy that the oxide material with the highest value dielectric constant (HfO_2) results in the broader depletion width under the drain at increasing V_{GS}, whereas the depletion widths are subsequently obtained at low-k dielectric materials.

5.4. Chapter Summary

This chapter deals with the device substrate analysis of depletion width formation using the numerical solution at the different gate-oxide dielectric constant and the thickness. This analysis gives insight into the oxide material's effect on junction depths. The depletion width at increasing ε_{ox} (k) values of the oxide material declines at increasing gate potentials, following the short channel. Furthermore, the depletion width under source and drain decreases with increasing oxide thickness (t_{ox}) for the higher values of k.

The CSDG MOSFET has a cylindrical structure devised from a double-gate planar MOSFET, and therefore, the analyzed insightful notion is used in the analytical model for CSDG for scaling improvements in the next chapter.

Chapter-6

THICKNESS ANALYSIS OF CSDG MOSFET

Due to the shrinking of transistor size, the channel becomes too small and leads to the short-channel effects, which necessitate analysis of the optimum device design, particularly to the operating conditions. Using the notion of depletion region formation at short-channel MOSFET, approximate numerical solution and silicon thickness inducing Cylindrical Surrounding Double-gate (CSDG) MOSFET parameters have been analyzed in this chapter. Further, the results of the depletion depth regions with the optimum silicon thickness have been realized.

This chapter introduces the depletion region of single gate MOSFET operation and further derives the expression for the minimum thickness of CSDG MOSFET. Subsequent, the results of depletion depth and optimum silicon thickness of CSDG MOSFET analyzed at various carrier concentrations and drain bias are explained.

6.1. Introduction

The charge-sheet model that can quickly analyze a long-channel device current in the subthreshold to saturation regime without discontinuity becomes inappropriate at reduced channel size [109-110]. At the device's nano-scaling, since the accumulation layer thickness is comparable to the device, the channel assumes that a thin sheet of charge vanishes [111-112].

Though the depletion layers or zone are the regions of the absentia of charges, the existence affects the device behavior and the channel thickness [113]. Therefore, channel thickness modeling becomes essential at various bias conditions to define the specifics of device operation and the channel dependence of the structural parameters.

An approximation of the silicon thickness and analysis for CSDG MOSFET using a mathematical derivation of depletion depth concerning the concept of strong inversion has been presented in this chapter. Further, the authors analyze the parameters influencing the thickness of CSDG MOSFET using the numerical solution results.

6.2. Depletion Depth in CSDG MOSFET

The analysis of semiconductor thickness in a CSDG MOSFET structure builds upon the formation of the depletion region. The depletion regions induced in a MOSFET are defined by Dang's model [114-115], which can be represented by the schematic in Fig. 6.1 at the device's short-channel length.

The depletion region in a MOSFET structure accounts for the inclusion of the source and drain depletion regions divided primarily into three separate sub-regions as a junction between the diffused source/drain and the substrate, depletion under the channel and by region induced by lateral source and drain diffusions [116-117]. The condition of channel formation, i.e., strong inversion in a MOSFET, considered for this mathematical analysis, is explained in the following subsections.

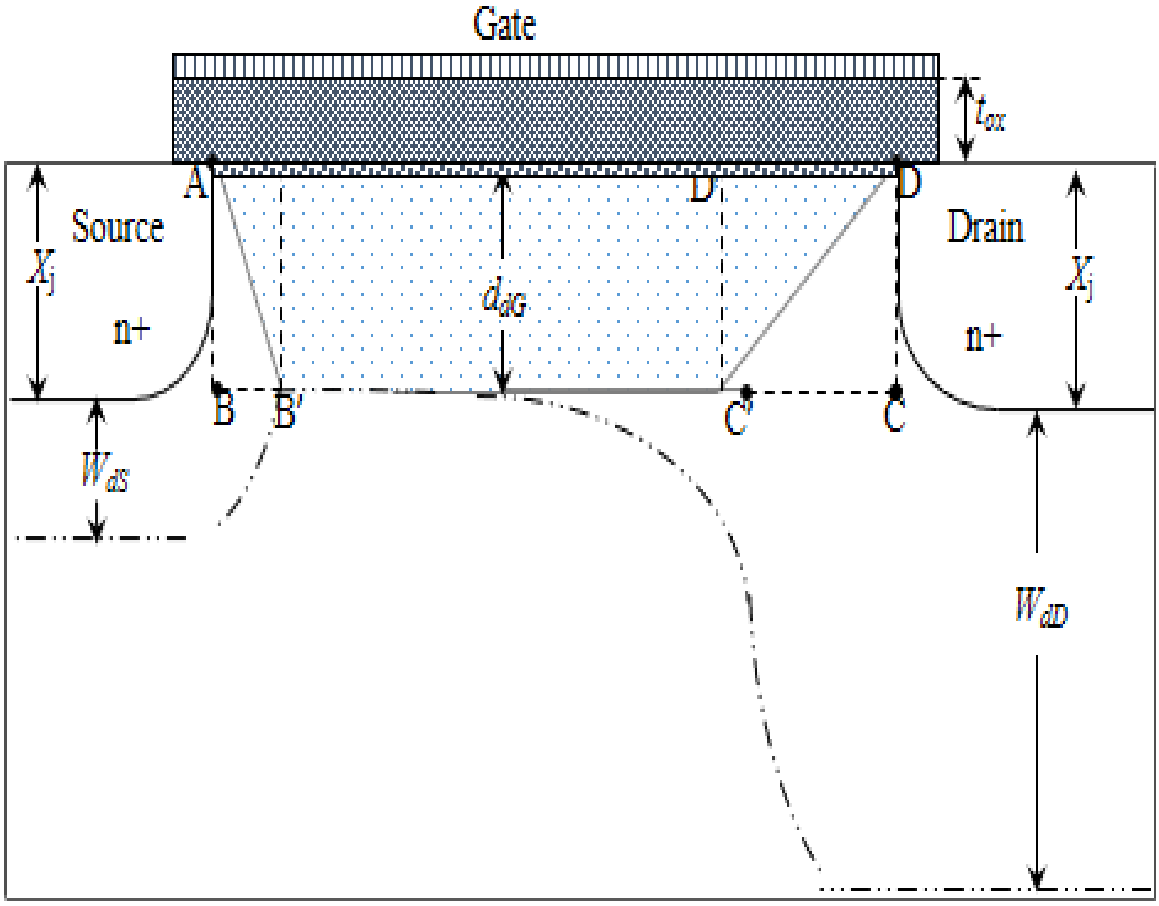


Fig. 6.1. Induced depletion regions in MOSFET.

6.3. Evolution of Depletion depth in MOSFET

The conventional MOSFET band diagram depicting the Fermi energy level at the inversion is shown in Fig. 6.2. When the surface of a MOS structure is inverted, it results in bands bending, and the Fermi level at the surface becomes closer to the conduction band [118, 119].

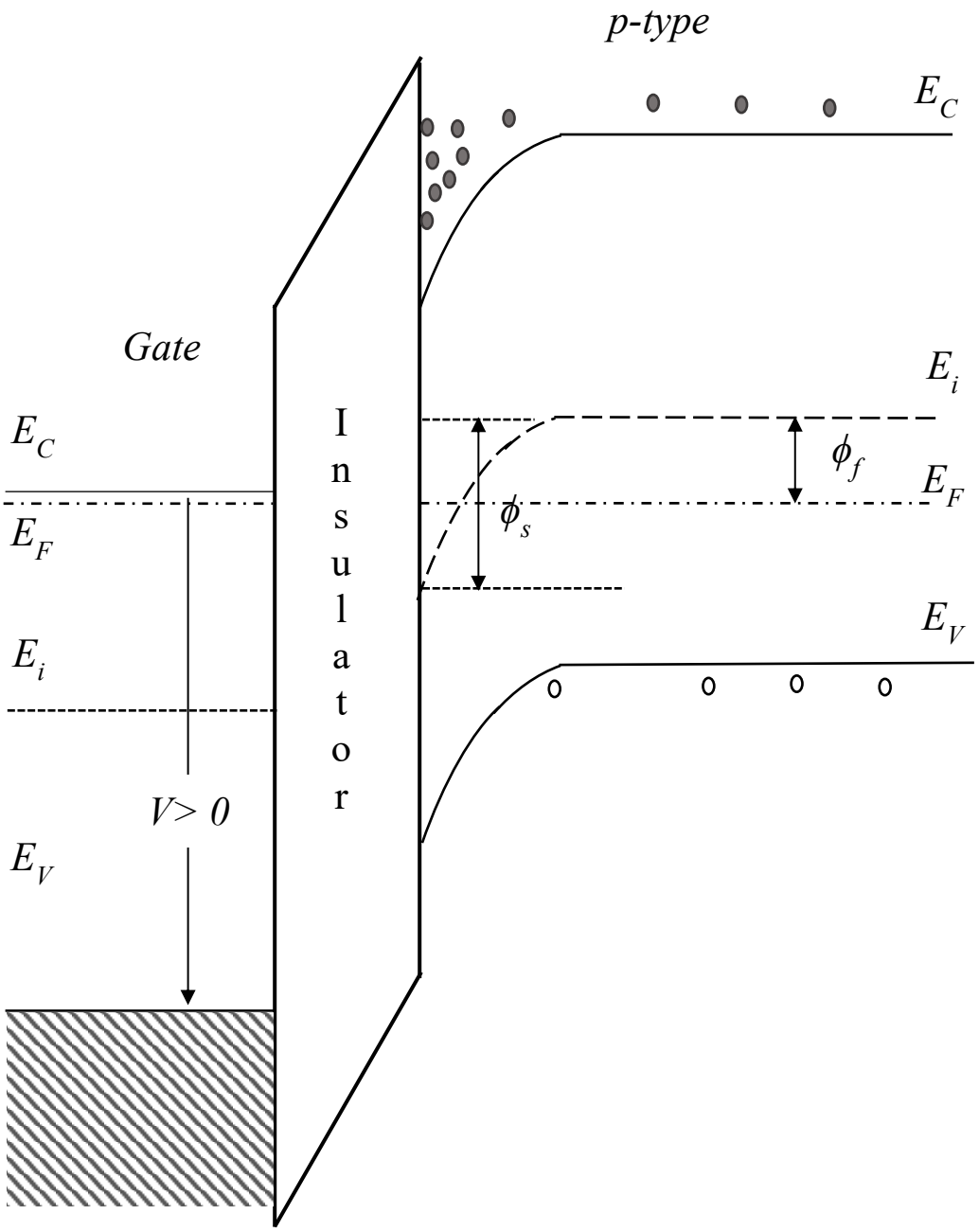


Fig. 6.2. Energy band of MOSFET at inversion [122, 123].

When the electrons concentration at the surface and the acceptor concentration of substrate are equal, a strong inversion occurs [120]. At the strong inversion, the Fermi level at the surface is located much above the intrinsic level, and the Surface-Potential for p-type substrate becomes $\phi_s=2\phi_f=2k\mathrm{Tln}(N_{sub}/n_i)$, where k is the Boltzmann's constant, N_{sub} is the acceptor concentration of substrate, and n_i is the intrinsic carrier concentration of silicon, ϕ_f is Fermi potential for semiconductor.

If the source is grounded and a minor positive gate-to-source bias creates a depletion region near the surface of the semiconductor-oxide interface, as shown in Fig. 6.2.

Here, the model is built upon the base theory given in the well-known Dang's Model. The optimum or minimum wherein the term is used as the depletion depth, at least, would essentially exist based on the device physics.

A strong inversion in a MOSFET, depletion depth, and charge in the depletion region remain unaffected from $V_{GS.}$ The depletion depth under the gate (d_{dG}) and charge density in the depletion region (Q_{dmax}) [121] can be given, as shown in Eq. 6.1) and (6.2).

$$d_{dG}=\left[\frac{2\varepsilon_{si}}{q\mathrm{N}_{sub}}\left(\phi_s-V_{bs}\right)\right]^{\frac{1}{2}} \tag{6.1}$$

$$Q_{dmax}=-q.\mathrm{N}_{sub}.d_{dG}$$

$$=-\left[2\varepsilon_{si}q\mathrm{N}_{sub}\left(\phi_s-V_{bs}\right)\right]^{\frac{1}{2}} \tag{6.2}$$

The depth of the channel (d_c) is maximum at the condition of strong inversion at which $\phi_s=2\phi_f$ relating d_c and d_{dG} [113], can be written as in Eq. (6.3).

$$d_c=d_{dG}\left(\frac{\sqrt{2}-1}{\sqrt{2}}\right) \tag{6.3}$$

and $$W_C=0.0631+0.8W_P-\frac{0.011W_P}{X_j}$$

where W_c represents the depletion width in the curved region which depends upon planar junction depletion width (W_P) and the junction depth (X_j) and follows the relation [124-126].

6.4. Optimum Semiconductor Thickness at Strong Inversion

The planar depth can be determined from the constituting material and doping parameters by $W_P = (2\varepsilon_{si}V_x/q\mathrm{N}_{sub})^{1/2}$. The V_x takes the value of either V_{bi} or $V_{bi} - V_{DS}$ depending upon the source and the drain diffusion. The X_j is given by Eq. (6.4).

$$X_j = 2\sqrt{D_o\tau \times \exp\left(\frac{-E_A}{kT}\right)\left[\ln\left(\frac{\mathrm{N}_s}{\mathrm{N}_{sub}}\right)\right]} \tag{6.4}$$

where D_o, τ, and E_A are the temperature-independent pre-exponent (m^2/sec), diffusion time (sec), and activation energy for diffusion (eV), respectively, and k, T, N_s, and N_{sub} are the Boltzmann constant, absolute temperature, surface concentration, and the substrate doping concentration, respectively. Considering typical metallurgical junction depth for n-type using phosphorus diffusion and assuming the width of the planar junction and curved region are equal, the width of the depletion region under the source and drain diffusion can be approximated as given in Eq. (6.5), adapted from [127]:

$$W_{dD} = \left[\frac{2\varepsilon_{si}}{q\mathrm{N}_{sub}}\left(2\phi_s - V_{DS} - V_{bs}\right)\right]^{\frac{1}{2}} \tag{6.5}$$

As shown in Fig. 6.2 at strong inversion, $\phi_s = 2\phi_f$. The maximum depletion depth from the oxide-semiconductor interface (d_{dG}), which approximates the diffused junction depletion depth, the optimum thickness of semiconductor (t_{smin}) in an operative short-channel single-gate MOSFET can be determined from the equation, as given as:

$$t_{smin} \approx \left[\left(2\phi_f - V_{bs}\right)^{\frac{1}{2}} + \left(2\phi_f - V_{DS} - V_{bs}\right)^{\frac{1}{2}}\right] \times \left(\frac{2\varepsilon_{si}}{q\mathrm{N}_{sub}}\right)^{\frac{1}{2}} \tag{6.6}$$

The CSDG MOSFET has a radius of internal gate metal ‘a’ and outer gate metal ‘b’ [128-129]. Therefore, the CSDG total thickness (t_{CSDG}), including silicon thickness (T_{si} = $4t_{smin}$) at the onset of strong inversion, is shown in Fig. 6.3 and given by Eq. (6.7).

$$t_{CSDG} = 2\left[\left(\frac{2\varepsilon_{si}}{q\mathrm{N}_{sub}}\right)^{\frac{1}{2}}\left\{\left(2\phi_{f} - V_{BS}\right)^{\frac{1}{2}} + \left(V_{bi} - V_{DS} - V_{bs}\right)^{\frac{1}{2}}\right\}\right] + 2t_{ox} + 2a + 2t_{m} \tag{6.7}$$

where t_m and t_{ox} are the gate-metal and oxide thicknesses of the CSDG structure, respectively. The governing Eq. (6.7) is comprised of the device and regional material size parameters.

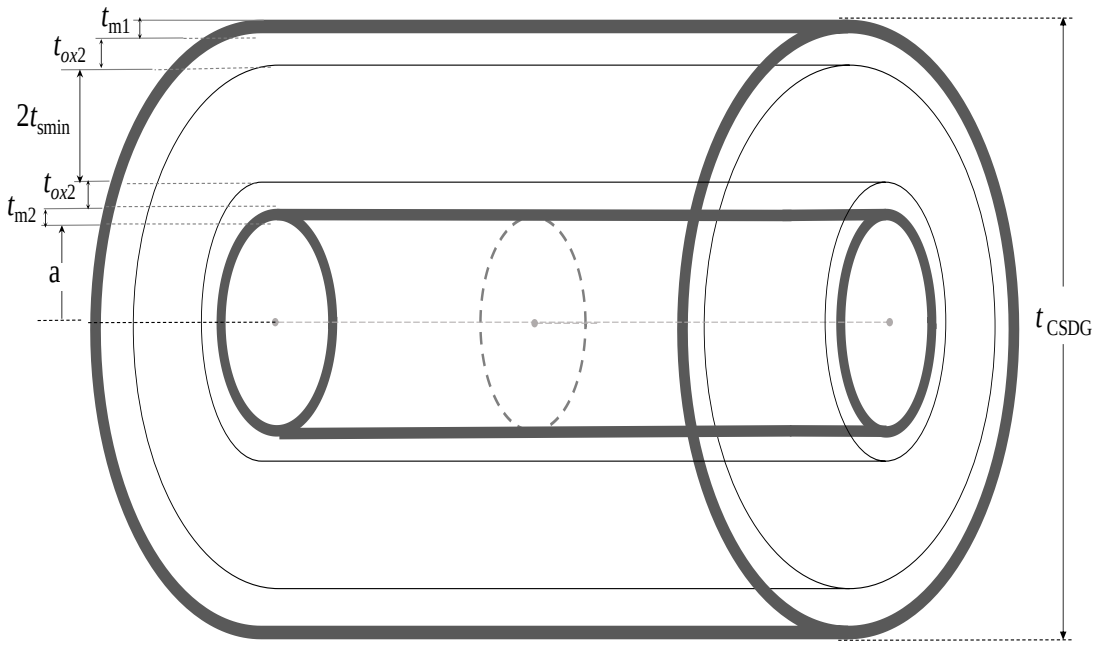


Fig. 6.3. Schematic representation of thickness at strong inversion in CSDG MOSFET structure.

6.5. Optimum Semiconductor Thickness at $V_{GS} > V_{TH}$

When gate bias voltage V_{GS} increases (than the threshold voltage), the depletion layer thickness under the source (W'_{dS}) and the drain (W'_{dD}) is given by Eq. (6.8) [130-131].

$$W_{dS}^{'} = \left[\frac{2\varepsilon_{si}}{q\mathrm{N}_{sub}} \left(\phi_{\mathrm{s}} - V_{\mathrm{bs}} \right) \right]^{\frac{1}{2}} \tag{6.8a}$$

$$W_{dD}^{'} = \left[\frac{2\varepsilon_{si}}{q\mathrm{N}_{sub}} \left(\phi_{S} - V_{\mathrm{DS}} - V_{\mathrm{BS}} \right) \right]^{\frac{1}{2}} \tag{6.8b}$$

Moreover, the depletion thickness under the gate terminal d'$_{dG}$ is given by:

$$d_{\mathrm{dG}}^{'} = \left[\frac{2\varepsilon_{si}\varepsilon_{o}}{q\mathrm{N}_{sub}} \left(\phi_{s} - V_{\mathrm{bs}} \right) \right]^{\frac{1}{2}} \text{ at } V_{\mathrm{GS}} > V_{\mathrm{TH}} \tag{6.9}$$

Moreover, ϕ_{s} can be conveyed as $\phi_{\mathrm{s}} = V_{\mathrm{GS}} - V_{ox,}$ where V_{ox} is the gate-oxide voltage. Considering a negligible value of flat-band voltage, Eq. (6.10) reflects the thickness of the depletion layer under the gate as a function of the bias voltage V_{GS}. Besides, the depletion layer thickness is related to the other parameters.

The relationship between the d'_{dG} versus V_{GS} has been analyzed where the charge on the gate terminal results from conservation property of charge [132-134] at strong inversion as the sum of ionized acceptors charge (coulomb/m^2) at drain terminal and channel charges near the semiconductor surface. The charge developed at the gate region can be given as:

$$Q_{\mathrm{G}} = q\mathrm{N}_{sub} d_{\mathrm{c}} + \sqrt{2q\mathrm{N}_{sub}\varepsilon_{si}\varepsilon_{o}\phi_{\mathrm{s}}} \tag{6.10}$$

Therefore, the gate-oxide voltage for a CSDG structure yields as:

$$V_{ox} = q\mathrm{N}_{sub} d_{\mathrm{c}} + \sqrt{2q\mathrm{N}_{sub}\varepsilon_{si}\varepsilon_{o}\phi_{\mathrm{s}}} \Big/ C_{ox} \tag{6.11}$$

where d_c is the thickness of the channel, and C_{ox} is the oxide capacitance of the structure. For CSDG, the cylindrical oxide capacitance would be applicable instead of a planar configuration.

The calculated values for the analyzed CSDG oxide capacitance from our work, as discussed in the previous chapter, can be replaced in Eq. (6.11) [135] since the structure takes truncated conical capacitor shape at saturation, as given below:

$$C_{ox(CSDG)} = \frac{\dfrac{a\pi\varepsilon_{ox}t_{si}}{L.\ln\left\{\left(\dfrac{t_{ox}+0.5t_{si}}{2a+t_{ox}+0.5t_{si}}\right)\left(1+\dfrac{2a}{t_{ox}}\right)\right\}}\left[\dfrac{2\pi\varepsilon_{ox}L}{\ln\left(\dfrac{b}{a+t_{si}}\right)}-\dfrac{\pi\varepsilon_{ox}(b-t_{si}-t_{ox})t_{si}}{L\ln\left(\dfrac{2b-1.5t_{si}-2t_{ox}}{b-0.5t_{si}-t_{ox}}\right)}\right]}{\dfrac{a\pi\varepsilon_{ox}t_{si}}{L.\ln\left\{\left(\dfrac{t_{ox}+0.5t_{si}}{2a+t_{ox}+0.5t_{si}}\right)\left(1+\dfrac{2a}{t_{ox}}\right)\right\}}+\left[\dfrac{2\pi\varepsilon_{ox}L}{\ln\left(\dfrac{b}{a+t_{ox}}\right)}-\dfrac{\pi\varepsilon_{ox}(b-t_{si}-t_{ox})t_{si}}{L\ln\left(\dfrac{2b-1.5t_{si}-2t_{ox}}{b-0.5t_{si}-t_{ox}}\right)}\right]} \tag{6.12}$$

Therefore, by replacing oxide capacitance C_{ox} of Eq. (6.11) with CSDG oxide capacitance $C_{ox(CSDG)}$, the gate-oxide voltage for a CSDG MOSFET of channel Length (L), can be determined.

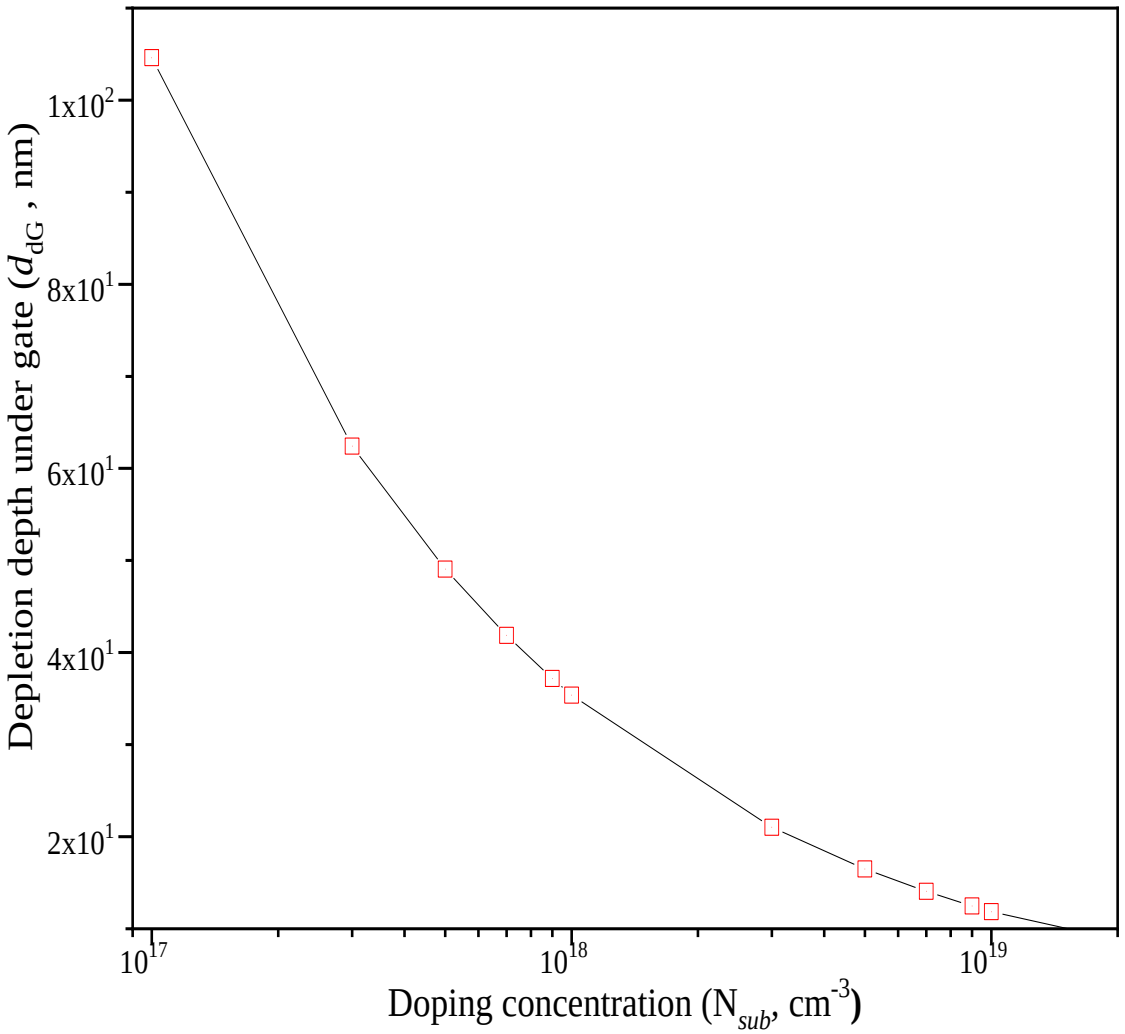


Fig. 6.4. Depletion depth under the gate versus doping concentration at the onset of strong inversion ($\phi_s=2\phi_f$) planar MOSFET.

For a short channeled CSDG MOSFET structure, the threshold voltage expression of an ultra-thin MOS structure given in [136] is appropriately relevant. Consequently, the threshold voltage of the CSDG device, which accounts for the oxide capacitance of a CSDG structure, would result as:

$$V_{\mathrm{TH}} = 2\phi_f + \frac{q\mathrm{N}_{\mathrm{sub}}\left(2\varepsilon_{si}\varepsilon_o\left(2\phi_f\right)^{1/2}+1\right)}{C_{ox(\mathrm{CSDG})}} + \left(\phi_m - (\chi + \frac{E_{\mathrm{g}}}{2q} + \phi_f)\right) \tag{6.13}$$

where ϕ_m, χ, E_g, and ϕ_f are the metal work function, electron affinity for semiconductor, bandgap, and the Fermi-potential.

The relation extracts an agreement with the depletion region, wherein the considerable current results at thin depletion widths. At inversion accumulates from weaker to strong, the surface charge for the CSDG device increases, which enlarges the depletion region. At unchanged gate bias, both the surface charges and the inversion charges attain the least values to conquer low subthreshold current. This modeled expression of the CSDG MOSFET is useful in resembling the device material thickness and entails a significant correlation with the entire device dimensions.

6.6. Result and Analysis

The mathematical relations developed in the previous section have been solved using an electronic simulator for the numerical analysis. This section presents the computed results of device thickness and depending parameters for a planar MOSFET and leading to the CSDG MOSFET.

To consider the effect of doping on the depletion elements and the thickness, the analysis has been initiated with the Surface-Potential's statistic dependence on the carrier concentration. The Surface-Potential is related to the depletion depth that inhabits maximum value at the condition of strong inversion.

The effect on depth under the gate at different doping concentrations (N_{sub}) are shown in Fig. 6.4. The analysis in graph Fig. 6.4 involves doping dependence of d_{dG} (as labeled in Fig. 6.1) of single MOSFET using Dang's Model. Moreover, as the CSDG MOSFET is

a cylindrical orientation of a double-gate structure, the correlation for a twice of double-gate measurements is the input for final calculation in CSDG MOSFET. The doping variation effect on maximum depletion width under the gate at strong inversion is listed in Table 6.1.

Table 6.1. Doping variation effect on maximum depletion width under the gate at strong inversion.

V_{DS} (V)	Doping Concentration(cm^{-3})	Depletion width under the drain (nm)
0.2	1×10^{17}	104.6223
0.2	3×10^{17}	62.42835
0.2	5×10^{17}	49.06893
0.2	7×10^{17}	41.86253
0.2	9×10^{17}	37.17521
0.2	1×10^{18}	35.3688
0.2	3×10^{18}	21.0203
0.2	5×10^{18}	16.49393
0.2	7×10^{18}	14.05651
0.2	9×10^{18}	12.47293
0.2	1×10^{19}	11.86305
0.2	3×10^{19}	7.02834
0.2	5×10^{19}	5.50748
0.2	7×10^{19}	4.68961
0.2	9×10^{19}	4.15871
0.2	1×10^{20}	3.95435

Referring to Eq. (6.5), the depletion depth under the diffused drain (W_{dD}) depends on the doping concentration and the drain bias. Fig. 6.5 illustrates the dependence of W_{dD} with doping concentration at increasing drain-source voltages (V_{DS}) at 0.*2* V, *0.4* V, *0.6* V, and *0.8* V, respectively. It has been noted that the depletion depth under the drain region decays exponentially with increasing doping concentration.

Table 6.2. Effect of variation of doping on maximum depletion width under the gate at strong inversion

Substrate doping(cm^{-3})	**Depletion width under the drain (nm)**			
	at V_{DS} 0.8V	**at V_{DS} 0.6V**	**at V_{DS} 0.4V**	**at V_{DS} 0.2V**
1×10^{17}	91.26956	75.6266	55.75511	22.31329
3×10^{17}	55.00262	46.42239	35.84395	20.36022
5×10^{17}	43.41108	36.91033	28.98659	17.83458
7×10^{17}	37.13106	31.71358	25.15525	16.11901
9×10^{17}	33.03466	28.30557	22.60801	14.86737
1×10^{18}	31.45332	26.98586	21.61392	14.35572
3×10^{18}	18.83158	16.35858	13.43794	9.67229
5×10^{18}	14.82268	12.94206	10.73694	7.94147
7×10^{18}	12.65701	11.08618	9.25241	6.95058
9×10^{18}	11.24701	9.87355	8.27518	6.28254
1×10^{19}	10.70332	9.40497	7.89595	6.01984
3×10^{19}	6.37752	5.65423	4.82367	3.81645
5×10^{19}	5.00971	4.45821	3.82807	3.07126
7×10^{19}	4.27233	3.81093	3.28535	2.6578
9×10^{19}	3.79291	3.389	2.92993	2.38405
1×10^{20}	3.6082	3.22619	2.79242	2.27746
3×10^{20}	2.14203	1.92822	1.68753	1.40624

At the larger densities, shallower depletion depth under the gate is obtained. The depletion depth at the decrease of decade order doping from 10^{19}, 10^{18}, and 10^{17} cm^3 results in reduced depths of *104.62* nm, *35.36* nm, and *11.86* nm.

The higher the value of V_{DS}, the thicker is the W_{dD} for any particular amount of $N_{sub.}$ The values of W_{dD} and d_{dG} both are maximum at strong inversion, and it constitutes a substantial portion of semiconductor thickness as displayed in Fig. 6.5; therefore, at such conditions, the thickness of silicon remains optimum.

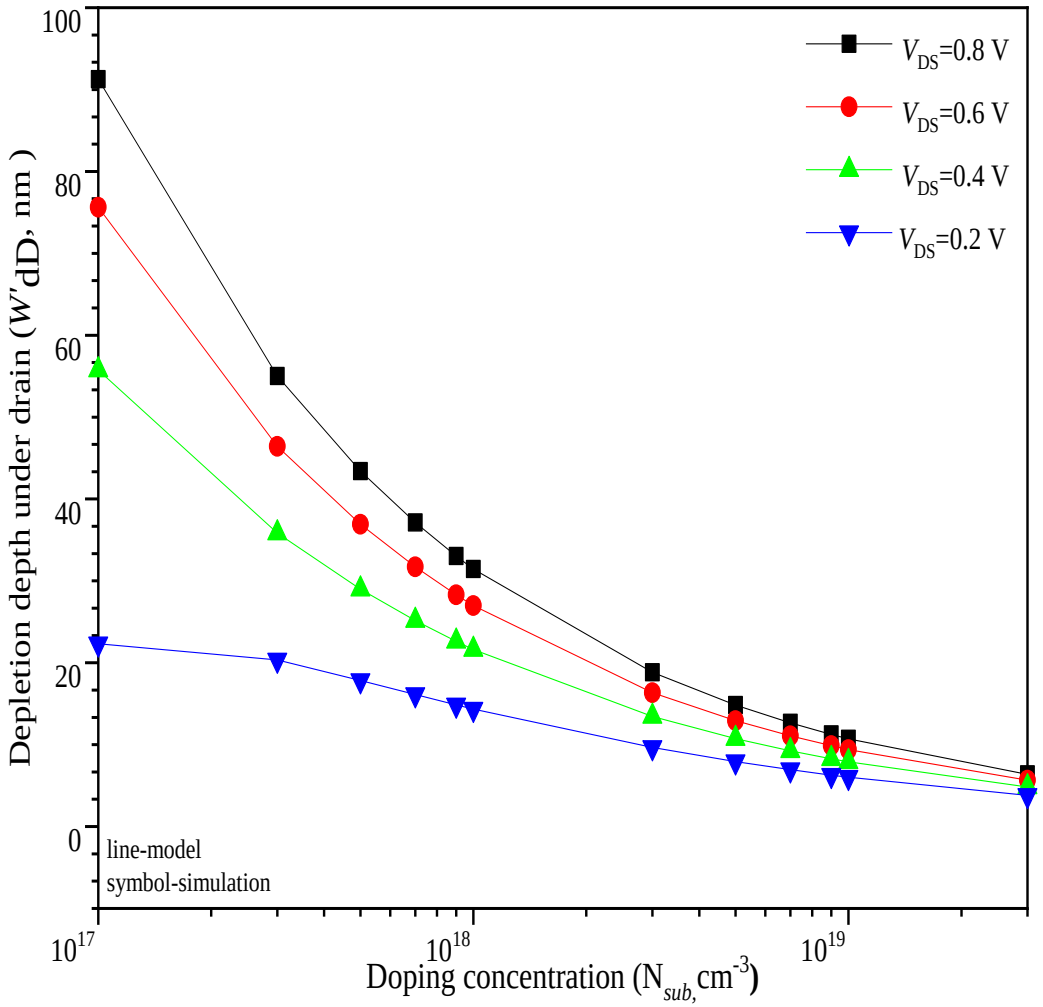


Fig. 6.5. Depletion width under the drain versus doping concentration at various V_{DS}.

Fig. 6.6 shows the minimum silicon thickness parameter as a variant of doping concentration along with the drain potential. With an increase of the same order of the carrier densities (from 10^{17} cm^{-3} to 10^{18} cm^{-3}) for V_{DS} = *0.2* V to *0.8* V, the CSDG device's thickness reduces intensely. The results of the technique for a CSDG device depicting the comparison with a planar MOSFET at the varying simultaneous gate and drain potentials are shown in Fig. 6.7.

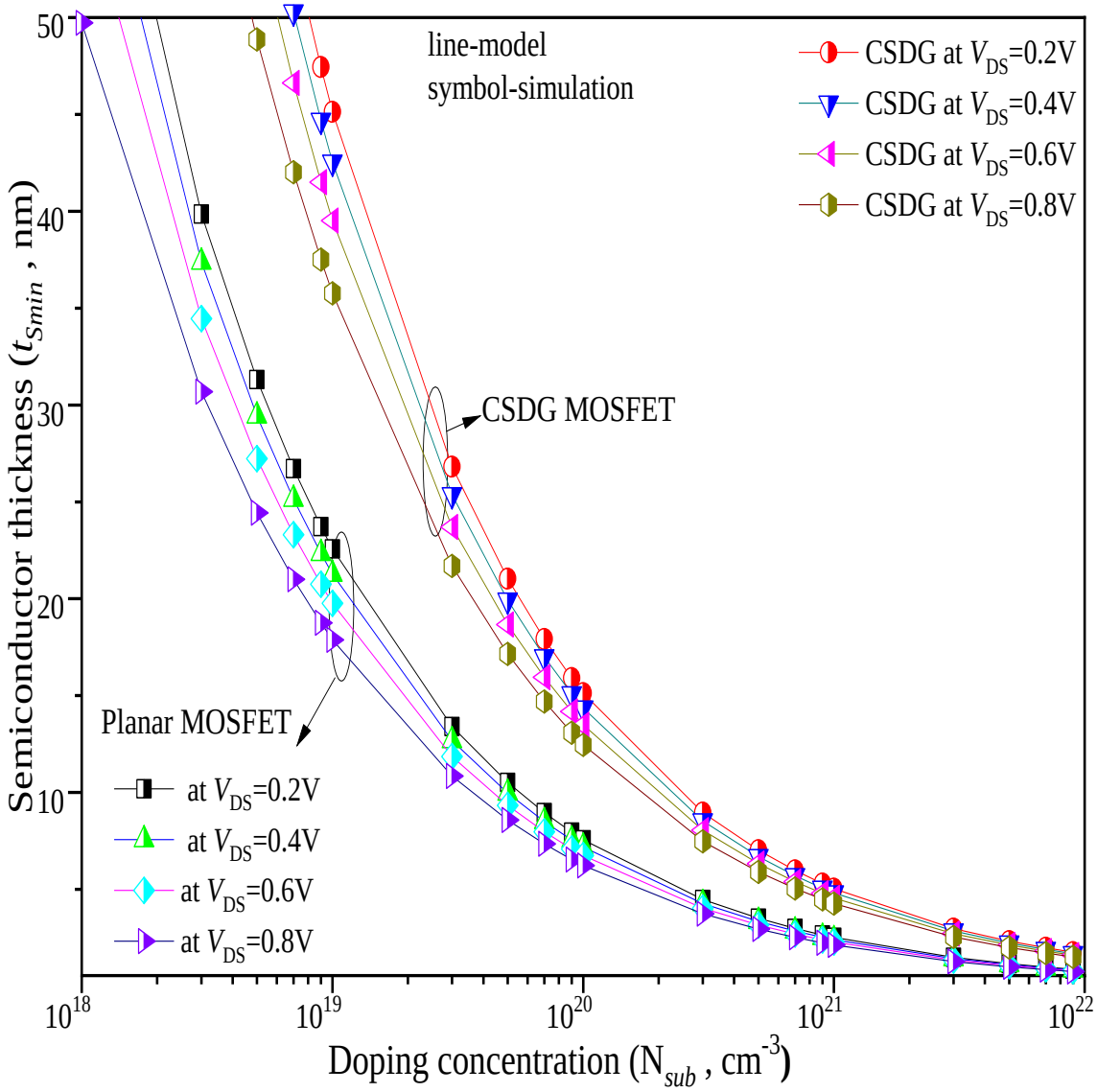


Fig. 6.6. Comparison of semiconductor thickness versus doping concentration in planar and CSDG structures at various V_{DS}.

Another significant probing from the derived model is to find the effect of device gate voltage (V_{GS}) and drain voltage (V_{DS}) on the thickness of the semiconductor. Therefore, the impact of V_{GS} on CSDG silicon thickness at a constant V_{DS} and N_{sub} at individual instants have been computed using the numerical methods

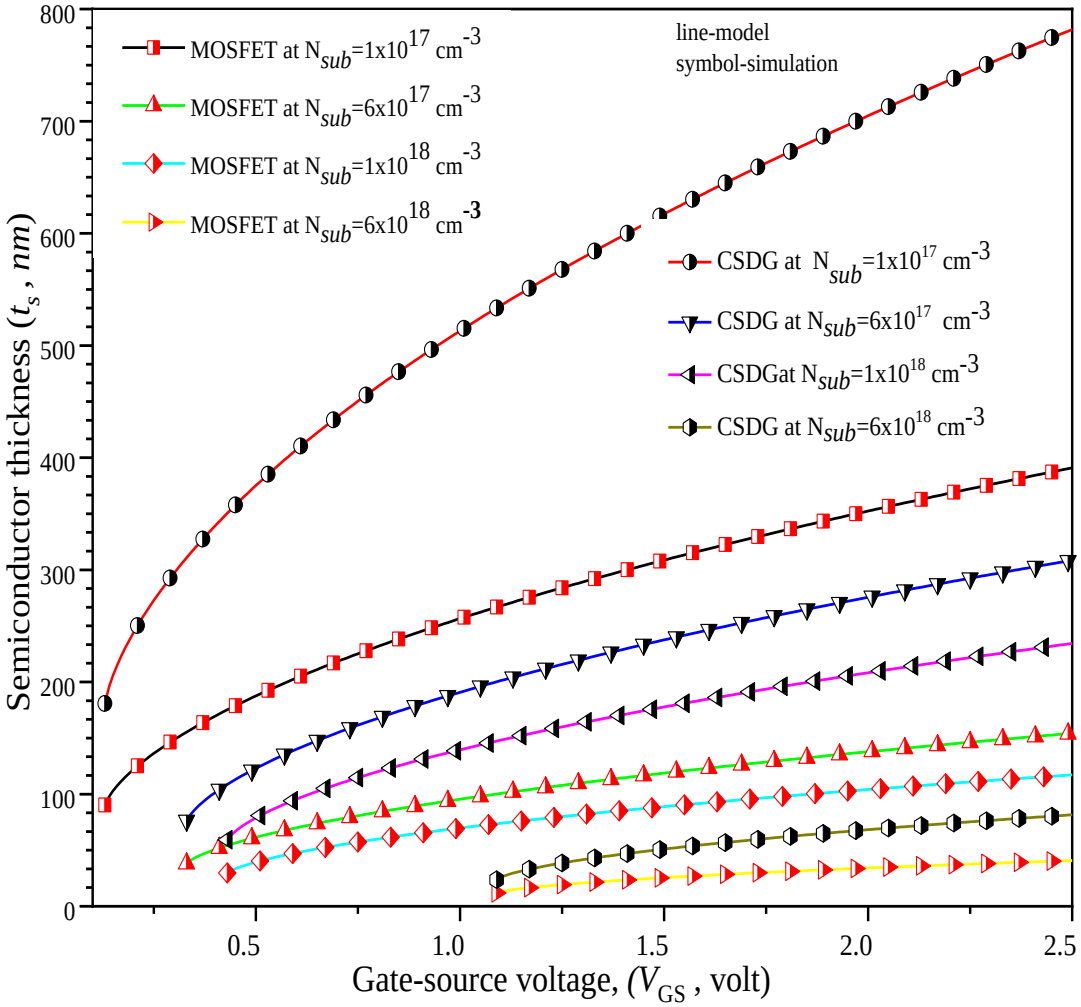


Fig. 6.7. CSDG Silicon thickness variation with applied Gate voltage at various N_{sub} and V_{DS}=0.2 volt.

6.7. Chapter Summary

This chapter provides the mathematical analysis of silicon thickness in Cylindrical Surrounding Double-Gate (CSDG) MOSFET has been derived from the depletion model of a conventional MOSFET. At the device's nano-scaling, since the accumulation layer thickness is comparable to the device, the channel's postulation as a thin sheet of charge vanishes. Though the depletion layers or zone are the regions of the absentia of charges, the existence affects the device behavior and the channel thickness. Therefore, channel thickness modeling becomes essential at various bias conditions to define the specifics of device operation and the channel dependence of the structural parameters. The chapter

presents an analytical model, and numerical analysis of the Cylindrical Surrounding Double-Gate (CSDG) MOSFET has been exemplified, including the thickness derived based on depletion depth formation analyzes the device performance at reducing dimensions. The analysis is built upon the device's physical and electrical parameters such as capacitance, electric field, thickness, threshold voltage, adequate channel dimensions, drain current is considered in this research. The depletion region in a MOSFET structure accounts for the inclusion of the source and drain depletion regions divided primarily into three separate sub-regions as a junction between the diffused source/drain and the substrate, depletion under the channel and by region induced by lateral source and drain diffusion.

The condition of a planar MOSFET in channel formation, i.e., for strong inversion, and when $V_{GS} > V_{TH}$ has been considered for this mathematical analysis. The computed results of device thickness and depending parameters for a planar MOSFET and the CSDG MOSFET have been compared. Based on this analysis, the typical CSDG MOSFET calculated silicon thickness is *180 nm*, *281 nm*, and *327* nm at V_{DS} *0.2* V, *0.8* V, and *1.2* V, respectively. The thickness modeling results proposed in this chapter show that nanoscale CSDG MOSFET can be deployed for improvements in the device performance and novel design modifications. The analysis presented in this work significantly contributes to interpreting the dependence of channel thickness in SMG and DMG structures of CSDG MOSFET and serves as a guide for the device scaling density developments.

Chapter-7

DUAL-METAL GATE STRUCTURE IN CSDG MOSFET

The metallic gate plays a significant role that improves the characteristics by controlling the carrier in the device channel. The metallic substance has a specific value of work-function due to inherited characteristics [137-139]. The work-function is a fundamental physical property that defines the least energy required to release one electron from the material surface. In the other sense, it is the minimum energy needed for an electron to move up from its Fermi level [140, 141]. Accordingly, the work-function is a prominent electronic property of any bare or coated metal. In the situation the traditional MOSFETs fail to attain, alternative device structures for further scaling have been invented. By an appropriate pursuit to the gate-metal work-function, the internal gate's threshold voltage could be transformed to a lower than the external gate with correspondingly lower internal gate-metal work-function [142].

Moreover, the potential profile along the channel results in depleting the broader channel region under the internal gate with drain potential variations to help simultaneously in mitigation to SCEs. This chapter details the analytical modeling of such CSDG MOSFET with a novel stacked-Dual-Metal Gate (DMG) structure using the solution of 2D Poisson's equations in the geometrical boundary conditions of the device. Moreover, a Cylindrical Surrounding Double-Gate (CSDG) MOSFET in an unstacked Dual-Metal Gate (DMG) design has also been simulated to study gate metal's ability to variate the channel field formation.

7.1. Conception of CSDG MOSFET with Dual-Metal Gate

The past research has revealed that the device characteristics such as on-current improvement and the negative effect of SCE can effectively be minimized if the gate material is appropriately engineered [143-145]. However, gate metal engineering also tends to increase the undesired off-current; nevertheless, I_{on}/I_{off} ratio remains unaltered due to the relative increase of the on-current.

Furthermore, the metal with low work-function on the drain side drops the drain bias across the region. It tends to decay in the direction of the drain end, which leads to a decline of Drain-Induced-Barrier-Lowering (DIBL) and channel length modulation effects in the device performance [146-148].

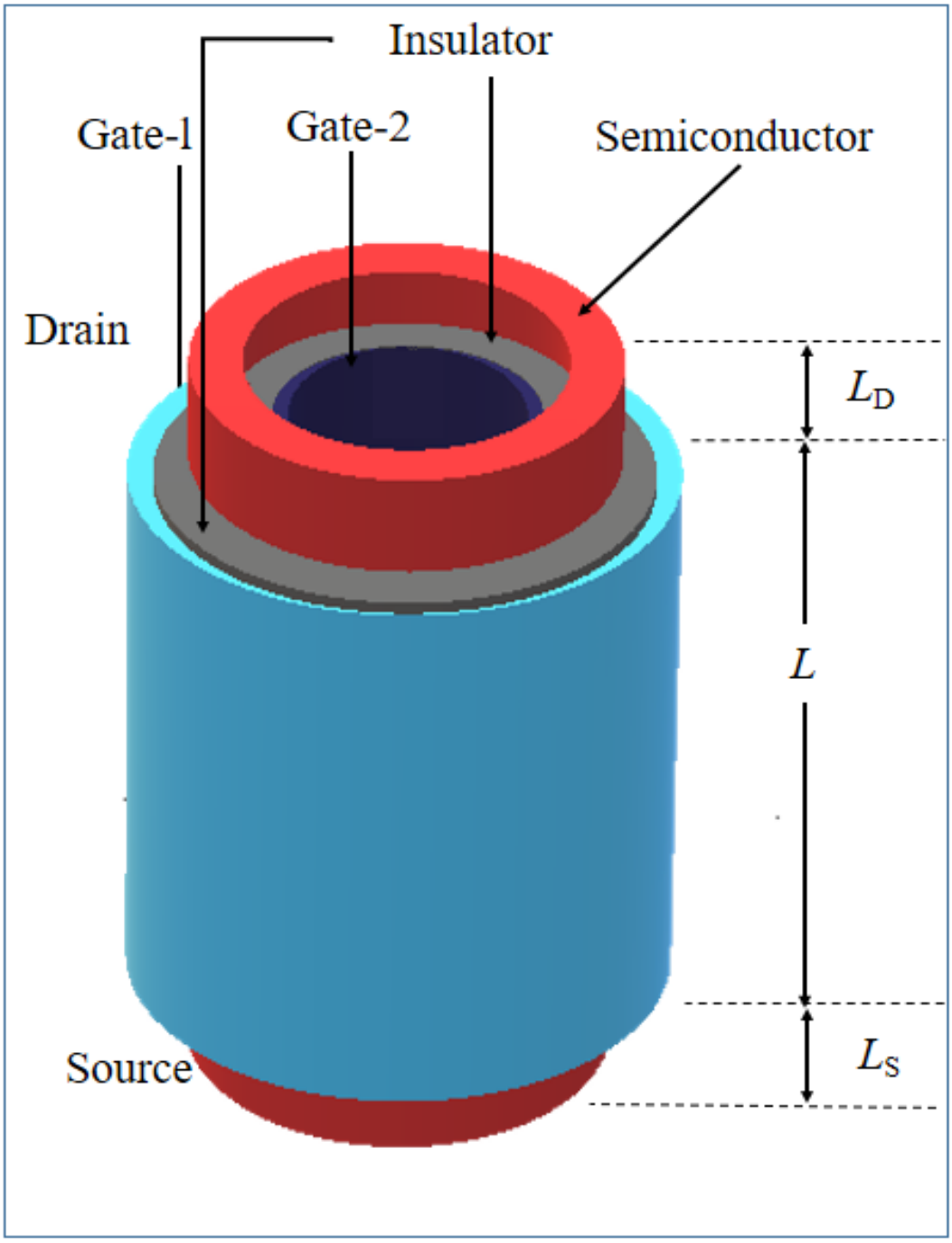


Fig. 7.1. Proposed schematic of cylindrical DMG architecture of CSDG MOSFET.

Further, the internal gate's threshold voltage (V_{TH1}) could be reduced compared to the external gate (V_{TH2}) by arranging the gate metal work-function in Double-Gate devices. Therefore, a device design of CSDG MOSFET has first been conceptualized, as shown in Fig. 7.1. In this configuration of DMG, the dual-metal gate structure contains dissimilar metals for both gates with the same channel length (L). The cross-sectional schematic of the cylindrical DMG is shown in Fig. 7.2.

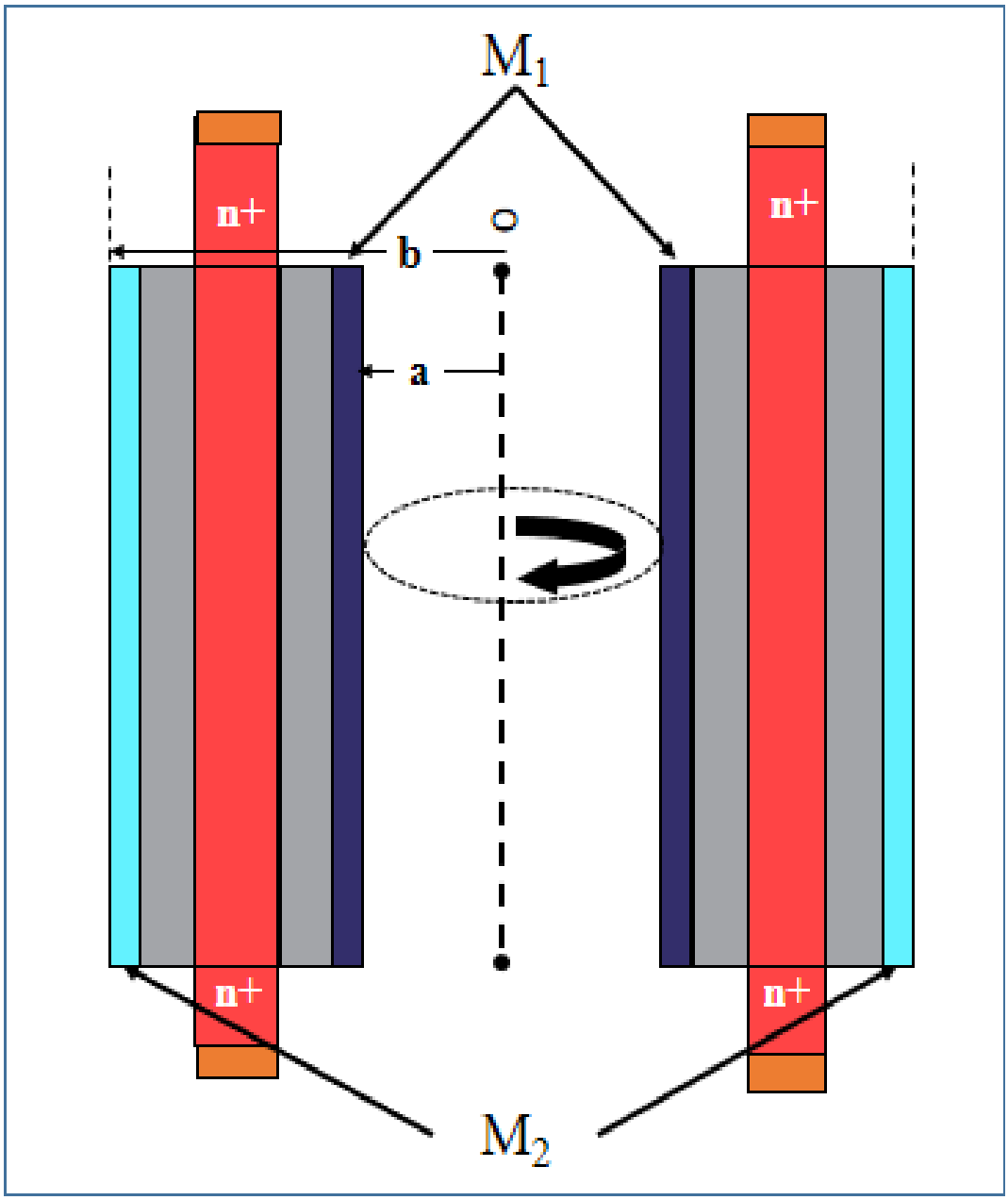
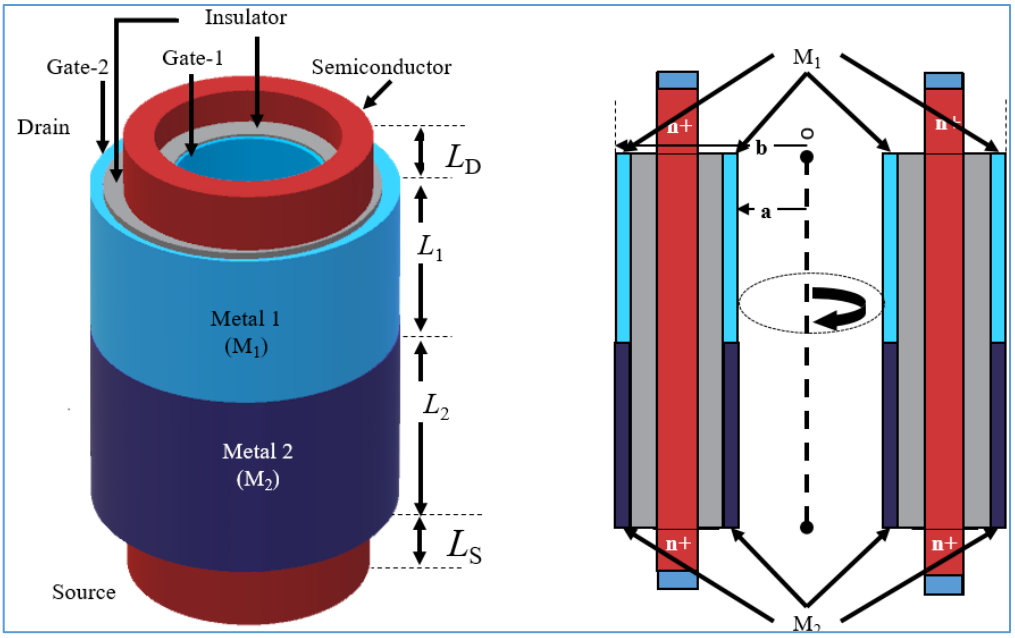
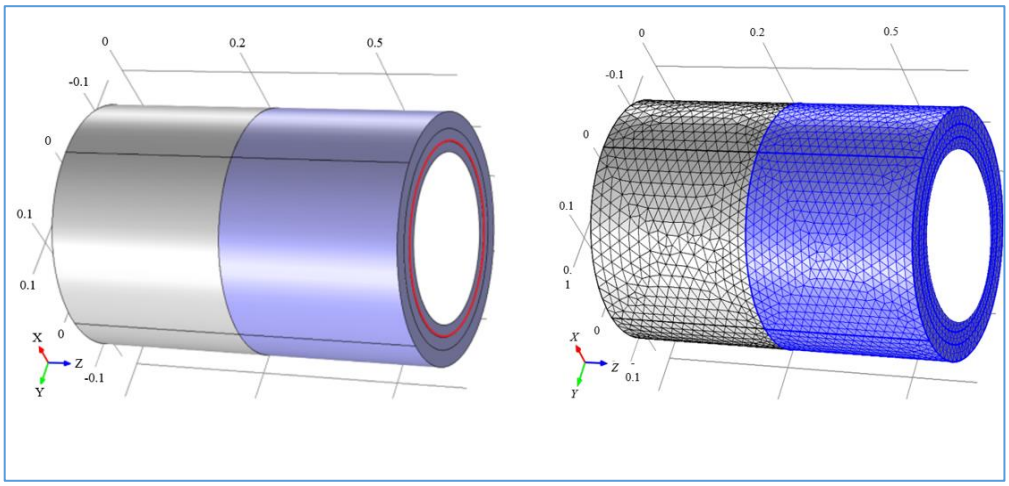


Fig. 7.2. Cylindrical DMG architecture of two-dimension cross-sectional view.

The internal and external assembly of CSDG MOSFET differs in terms of the metal work-function of Gate-1 and Gate-2, while the dielectric material serving as gate insulators is the same. It is noteworthy that at smaller dimensions with shorter channel lengths, the device is also influenced by the confinement of energy, and the quantum-mechanical effects govern the device operation. The channel scaling has been considered such that the quantum effects are omitted in this work [149-151].



(a)



(b)

Fig. 7.3. A stacked-dual-metal gate based CSDG MOSFET device (a) schematic and a cross-sectional view, (b) simulation and meshing structure.

The schematic of the CSDG MOSFET with Dual-Metal Gate (DMG) architecture and its simulation structure is shown in Fig. 7.3. Both of the gates contain similar metal up to the length L_1 and L_2 individually. The device follows an internal gate radius 'a' and an external gate radius of 'b' from the center. The material considered for the gate insulator in the stacked-DMG structure is the same in terms of dielectric permittivity and thickness.

The gradual decrease of metal work-function towards the drain also improves the Drain-Induced-Barrier-Lowering (DIBL) and subthreshold characteristics [152-154]. The physics-based analysis of gate stack CSDG MOSFET that operates in saturation involving the analogy of cylindrical dual-metal gates has been considered to evaluate the performance improvements.

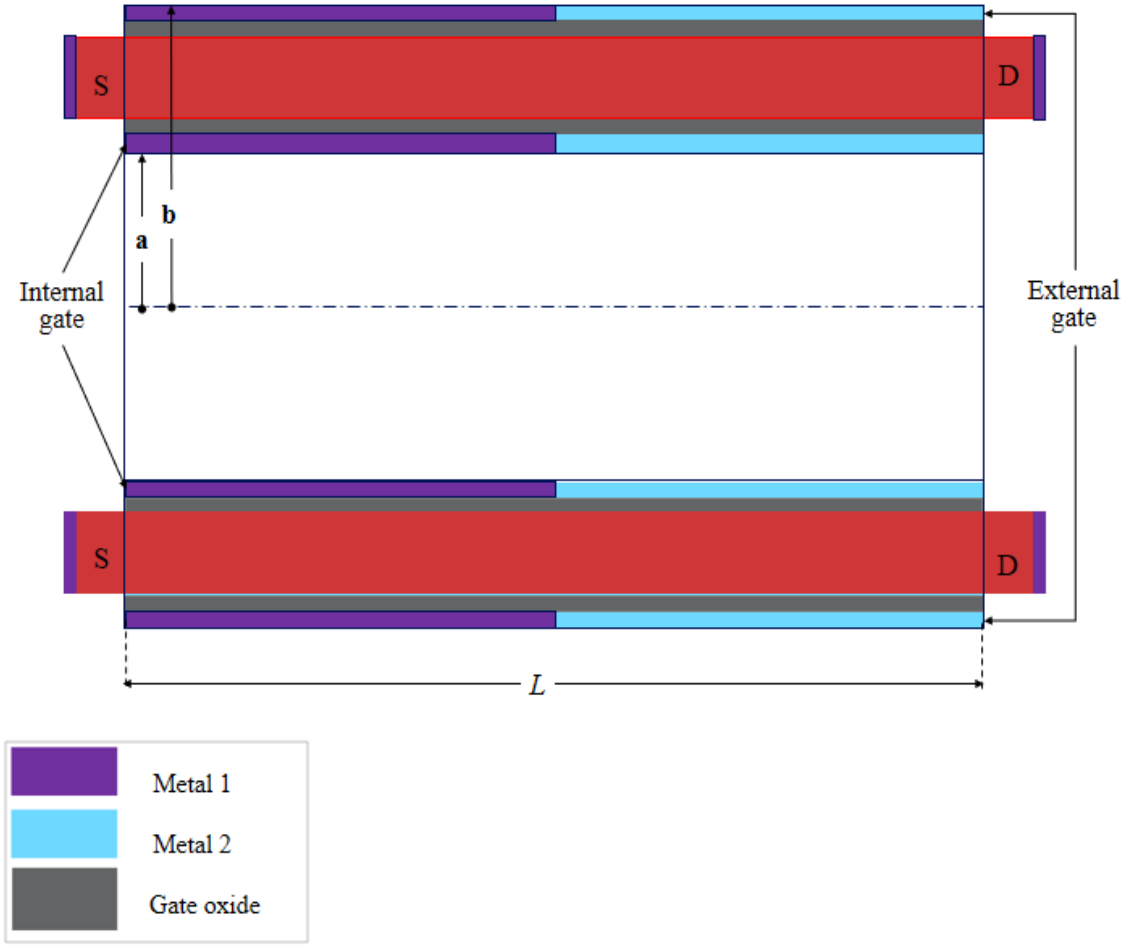


Fig. 7.4. Two-dimensional cross-section of the DM-CSDG MOSFET structure.

The 2-dimensional cross-section of the device is shown in Fig. 7.4. The derivation of the surface-potential, gate charge, threshold voltage model for the proposed DMG structure of the CSDG device has been explained in the subsequent sections.

7.2.1. Two-Dimensional Model for Surface-Potential

In general, the cylindrical coordinate system consists of directions in the radial and axial component, i.e., *r* and *z*, respectively, and the angular θ component in the radial direction plane. Due to the structure's symmetry, the electric field's potential has no variation in the θ direction. Therefore, the analysis can be adequately defined using a two-dimensional model.

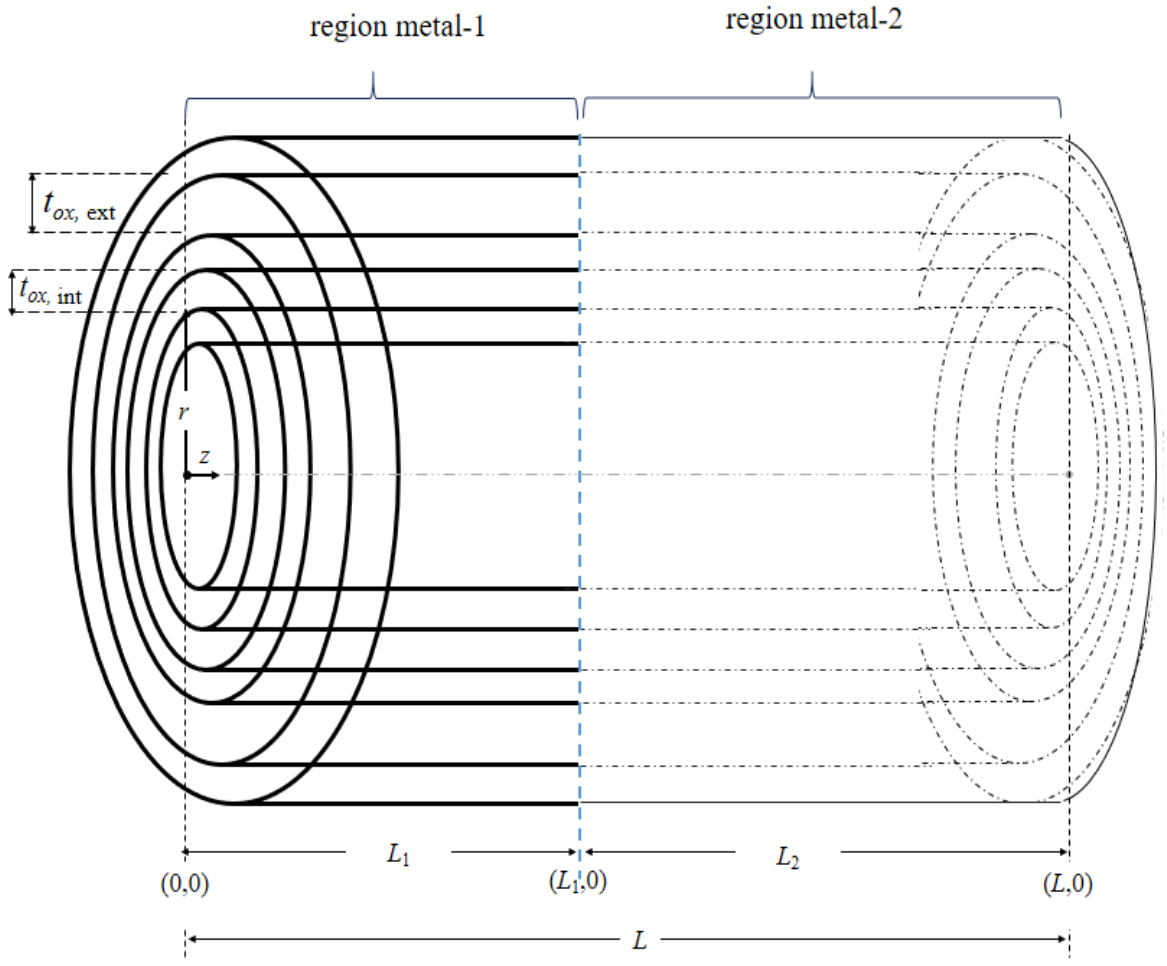


Fig. 7.5. DM-CSDG MOSFET structure outlining the two metal regions.

Fig. 7.5 shows the sketch of the proposed structure outlining the regions of the device. The solid-line part belongs to the device's portion with high metal work-function, and the dashed area has low metal work-function, comparatively. The relationship between surface-potential, charge, and the electric field in the semiconductor channel is appropriately defined by the solution of Poisson's equation [155, 156].

Assuming the charge carriers' negligible contribution and fixed charges in channel electrostatics, the channel's potential distribution at the onset of strong inversion can be defined by the 2-D Poisson's equation.

Furthermore, to obtain electric potential and drain current can be obtained using the right boundary conditions applied in the cylindrical coordinates system. Therefore, the potential distribution along the semiconductor involving both the CSDG MOSFET gates can be expressed using [157-159], as given Eq. (7.1).

$$\begin{aligned} V_{fb} &= \phi_{\mathrm{m}_i} - \phi_{\mathrm{si}} \Big| i = 1, 2, ..\mathrm{n} \\ \phi_{\mathrm{f}} &= \frac{k\mathrm{T}}{\mathrm{q}} \ln\left(\frac{\mathrm{N}_{sub}}{n_i}\right) \\ \phi_{\mathrm{si}} &= \chi_{\mathrm{s}} + \frac{E_{\mathrm{g}}}{2q} \ln + \phi_{\mathrm{f}} \end{aligned} \tag{7.1}$$

where $\phi(r, z)$ is the potential distribution in semiconductors, and $\mathrm{N_{sub}}$, q, ε_{si} are the substrate doping concentration, charge of the electron, and silicon permittivity. The potential profile in the perpendicular direction, which is the z dependence of the potential distribution, can be approximated using the parabolic function, applying which the individual potential distribution of the device for the internal and external gate assembly can be written as:

$$\phi_{s,\mathrm{int}}(r,z) = \mathrm{c}_1(z) + \mathrm{c}_2(z)r + \mathrm{c}_3(z)r^2 \tag{7.2a}$$

$$\phi_{s,\mathrm{ext}}(r,z) = \mathrm{c}_1^{'}(z) + \mathrm{c}_2^{'}(z)r + \mathrm{c}_3^{'}(z)r^2 \tag{7.2b}$$

where $\mathrm{c}_1(z)$, $\mathrm{c}_2(z)$, $\mathrm{c}_3(z)$ and $\mathrm{c}'_1(z)$, $\mathrm{c}'_2(z)$, and $\mathrm{c}'_3(z)$ are the function of z that can be determined by applying boundary conditions for the internal and the external gate assembly, respectively. Ensuing Gauss' Law, the electric field at the center of the

semiconductor is zero. Therefore, the potential at the surface of internal and external gate after complying the structure boundary condition, i.e., $\phi(r{=}\mathrm{a}, z) = \phi(\mathrm{a}) = \phi_{\mathrm{int}}(0)$ and $\phi(r{=}\mathrm{b}, z) = \phi(\mathrm{b}) = \phi_{\mathrm{ext}}(0)$, can be given as:

$$\left.\frac{d\phi(\mathrm{r},\mathrm{z})}{d\,\mathrm{r}}\right|_{r=0,\mathrm{r=a}} = 0; \qquad \text{and} \quad \left.\frac{d\phi(\mathrm{r},\mathrm{z})}{d\,\mathrm{r}}\right|_{r=0,\mathrm{r=b}} = 0 \tag{7.3}$$

Similarly, the electric field for the internal and external gate assembly at the interface of semiconductor and insulator can be written as:

$$\begin{aligned} \varepsilon_{si}\left.\frac{d\phi(r,z)}{dr}\right|_{\mathrm{r}=a} &= C_{ox,\mathrm{int}}(V_{\mathrm{GS,int}} - V_{fb,\mathrm{int}} - \phi_{\mathrm{s,int}}(r{=}\mathrm{a}, z)); \\ \varepsilon_{si}\left.\frac{d\phi(r,z)}{dr}\right|_{\mathrm{r}=b} &= C_{ox,\mathrm{ext}}(V_{\mathrm{GS,ext}} - V_{fb,\mathrm{ext}} - \phi_{\mathrm{s,ext}}(r{=}\mathrm{b}, z)) \end{aligned} \tag{7.4}$$

where $C_{ox,\mathrm{int}}$ and $C_{ox,\mathrm{ext}}$ are the gate-capacitances of the device's internal and external assembly, excluding the confinement phenomenon [160-163].

$$\begin{aligned} C_{ox,\mathrm{int}} &= \varepsilon_{ox} \Big/ \mathrm{a}\ln\left(1+\frac{t_{ox}}{\mathrm{a}}\right) \\ C_{ox,\mathrm{ext}} &= \varepsilon_{ox} \Big/ \mathrm{b}\ln\left(1+\frac{t_{ox}}{\mathrm{b}}\right) \end{aligned} \tag{7.5}$$

Further, $V_{\mathrm{GS,int}}$, $V_{\mathrm{GS,ext}}$ and $V_{fb,\mathrm{int}}$, $V_{fb,\mathrm{ext}}$ are the applied gate-source and the channel flat band voltages of the internal and external gate. Considering, equal channel flat band voltage for the internal and external gate of the device, i.e., $V_{fb,\mathrm{int}} = V_{fb,\mathrm{ext}} = V_{fb} = \phi_m - \phi_s$. The ϕ_m and ϕ_s are the gate-metal and Silicon work-function, respectively.

The proposed structure is comprised of dual-metal for its gate, so the flat band voltage for channel length $0 < z < L_1$ turn into $V_{fb1,\mathrm{int}}$ and $V_{fb1,\mathrm{ext}}$ while $L_1 < z < L$ becomes $\mathrm{V}_{fb2,\mathrm{int}}$ and $\mathrm{V}_{fb2,\mathrm{ext}}$ for the internal and external gate assembly respectively. It can be determined by the following given equations [164, 165]:

$$V_{fb1} = V_{\mathrm{b1}} - \phi_{si} = V_{\mathrm{b1}} - \left(\chi + \frac{E_{\mathrm{g}}}{2} + \frac{kT}{q}\ln\frac{\mathrm{N}_{sub}}{n_i}\right) \qquad \text{for length } L_1 \tag{7.6a}$$

$$V_{fb2} = V_{b2} - \phi_{si} = V_{b2} - \left(\chi + \frac{E_g}{2} + \frac{kT}{q}\ln\frac{\mathrm{N}_{sub}}{n_i}\right) \qquad \text{for length } L_2 \tag{7.6b}$$

where χ, $E_{g,}$ and N_{sub} are the electron affinity, bandgap, and the substrate doping of the semiconductor, respectively. In this analysis, identical gate metal is assumed for both the regions up to length $0 < z < L_1$ and $L_1 < z < L$, therefore, the flat band voltage of the internal and external gates can be equalized as $V_{fb1,\text{int}} = V_{fb1,\text{ext}}$ and $V_{fb2,\text{int}} = V_{fb2,\text{ext}}$.

The potential at the source and drain side can be expressed as:

$$\begin{aligned}\phi(r, z=0) &= V_{\text{bi}} - \phi(r) \\ \phi(r, z=L) &= V_{\text{bi}} + V_{\text{DS}} - \phi(r)\end{aligned} \tag{7.7}$$

The constants $c_1(z)$, $c_2(z)$, $c_3(z)$ and $c'_1(z)$, $c'_2(z)$, $c'_3(z)$ have been determined using the boundary equations given in Eq. (7.3) to Eq. (7.7) and that results as:

$$c_1(z) = \phi_{s,\text{int}}(z)\left[1 + \frac{C_{ox,\text{int}}\,a}{2\varepsilon_{si}}\right] - \frac{C_{ox,\text{int}}\,a}{2\varepsilon_{si}}\left[V_{\text{GS}_1} - V_{fb}\right] \tag{7.8a}$$

$$c_2(z) = 0 \tag{7.8b}$$

$$c_3(z) = \frac{C_{ox,\text{int}}}{2a\varepsilon_{si}}\left[V_{\text{GS}} - \phi_{s,\text{int}} - V_{fb}\right] \tag{7.8c}$$

$$c'_1(z) = \phi_{s,\text{ext}}(z)\left[1 + \frac{C_{ox,\text{ext}}\,b}{2\varepsilon_{si}}\right] - \frac{C_{ox,\text{ext}}\,b}{2\varepsilon_{si}}\left[V_{\text{GS2}} - V_{fb}\right] \tag{7.9a}$$

$$c'_2(z) = 0 \tag{7.9b}$$

$$c'_3(z) = \frac{C_{ox,\text{ext}}}{2b\varepsilon_{si}}\left[V_{\text{GS2}} - \phi_{s,\text{ext}} - V_{fb}\right] \tag{7.9c}$$

By substituting the values of $c_1(z)$, $c_2(z)$, $c_3(z)$ in Eq. (7.2a), the potential distribution of internal gate assembly has been obtained, as given by:

$$\phi_{s,\text{int}}(r,z) = \phi_{s,\text{int}}(z)\left[1 + \frac{C_{ox,\text{int}}}{2\varepsilon_{si}}\right] - \frac{C_{ox,\text{int}}\,a}{2\varepsilon_{si}}\left[V_{\text{GS}_1} - V_{fb}\right] + \frac{C_{ox,\text{int}}}{2a\varepsilon_{si}}[V_{\text{GS}_1} - \phi_{s,\text{int}}(z) - V_{fb}]r^2 \tag{7.10}$$

By substituting the values of Eq. (7.10), the Eq. (7.1) can be rewritten in the form of a differential equation as [166]:

$$\frac{d^2\phi_{s,int}(z)}{dz^2} - \lambda_{int}^2\phi_{s,int}(z) = \beta \tag{7.11}$$

Consequently, the derived value of surface-potential for the internal gate can be obtained from the solution of differential equation as $\phi_{s,int}(z) = A\, e^{z\lambda int} + B\, e^{-z\,\lambda int} - (\beta/\lambda^2_{int})$.

Similarly, by substituting the values of $c'_1(z)$, $c'_2(z)$, $c'_3(z)$ in Eq. (7.2a), potential distribution for external gate assembly can be determined as:

$$\phi_{s,ext}(r,z) = \phi_{s,ext}(z)\left[1+\frac{C_{ox,ext}}{2\varepsilon_{si}}\right] - \frac{C_{ox,ext}b}{2\varepsilon_{si}}\left[V_{GS_2} - V_{fb}\right] + \frac{C_{ox,ext}}{2b\varepsilon_{si}}[V_{GS_2} - \phi_{s,ext}(z) - V_{fb}]r^2 \tag{7.12}$$

Moreover, the differential equation signifying the potential distribution of external gate assembly can be obtained by substitution of the surface-potential from Eq. (7.12) into the Eq. (7.1), can be given as:

$$\frac{d^2\phi_{s,ext}(z)}{dz^2} - \lambda_{ext}^2\phi_{s,ext}(z) = \beta' \tag{7.13}$$

The solution of Eq. (7.13) results in the surface-potential for the external gate of the device; as $\phi_{s,ext}(z) = A' e^{z\lambda ext} + B' e^{-z\,\lambda ext} - (\beta'/\lambda^2_{ext})$. Owing to the two dissimilar metals utilized in the proposed device [167, 168], the surface-potential along the channel also becomes divergent, being a channel length function.

Subsequently, for $0 < z < L_1$, the surface-potential can be written for the higher metal work-function (V_{b1}) region as:

$$\phi_{s,L_1,int}(z) = A_1 e^{\lambda z} + B_1 e^{-\lambda z} - \frac{\beta_1}{\lambda_{int}^2} \tag{7.14a}$$

and the region of low metal work-function (V_{b2}), i.e., $L_1 < z < L_2$, the surface-potential would be:

$$\phi_{s,L_2,int}(z) = C_1 e^{\lambda z} + D_1 e^{-\lambda z} - \frac{\beta_2}{\lambda_{int}^2} \tag{7.14b}$$

where, the parameters λ, β_1, and β_2 can be given as:

$$\lambda_{\text{int}}^2 = 2\frac{C_{ox,\text{int}}}{\varepsilon_{si}\text{a}}$$

$$\beta_1 = \frac{q\text{N}_{sub}}{\varepsilon_{si}} - \lambda_1^2\left(V_{\text{GS}} - V_{fb1}\right) \qquad \text{for } 0 < z < L_1$$

$$\beta_1 = \frac{q\text{N}_{sub}}{\varepsilon_{si}} - \lambda_1^2\left(V_{\text{GS}} - V_{fb1}\right) \qquad \text{for } L_1 < z < L_2$$

$$\phi_{\text{s},L_1,\text{ext}}(z) = \text{A}_1^{'}e^{\lambda_{\text{ext}}z} + \text{B}_1^{'}e^{-\lambda_{ext}z} - \frac{\beta_1}{\lambda_{\text{ext}}^2} \text{ for } 0 < z < L_1 \tag{7.15a}$$

$$\phi_{\text{s},L_2,\text{ext}}(z) = \text{C}_1^{'}e^{\lambda_{\text{ext}}z} + \text{D}_1^{'}e^{-\lambda_{\text{ext}}z} - \frac{\beta_2}{\lambda_{\text{ext}}^2} \text{ for } \ L_1 < z < L_2 \tag{7.15b}$$

The constant A_1, B_1, C_1, D_1, and A'_1, B'_1, C'_1, and D'_1 can be derived from the boundary condition given in Eq. (7.3) to Eq. (7.7), whose computed values are shown in the Appendix.

Further, the electric field along *z*-direction across the channel can be obtained from the surface-potential derivative. Therefore, for the internal gate assembly of the DM-CSDG structure, the electric field along *z*-direction would result as in Eq. (7.16).

$$E_{z_1,\text{int}} = \frac{d\phi_{\text{s}_1,\text{int}}(z)}{dz} = \text{A}_1e^{\lambda_{\text{int}}z} - \text{B}_1e^{-\lambda_{\text{int}}z} \ \text{ for } \ 0 < z \le L_1 \tag{7.16a}$$

$$E_{z_2,\text{int}} = \frac{d\phi_{\text{s}_2,\text{int}}(z)}{dz} = \text{C}_1e^{\lambda_{\text{int}}z} - \text{D}_1e^{-\lambda_{\text{int}}z} \text{for } L_1 < z \le L \tag{7.16b}$$

Moreover, at the junction ($z = L_1$), $E_{z1,\text{int}}$, and $E_{z2,\text{int}}$ can be equated the same as:

$$\left.\frac{d\phi_{\text{s}_1,\text{int}}(z)}{dz}\right|_{z=L_1} = \left.\frac{d\phi_{\text{s}_2,\text{int}}(z)}{dz}\right|_{z=L_1}$$

The electric field significantly determines the variation of the drain-side electric field due to the proposed DM-CSDG structure.

7.2.2. Gate Charge and Threshold Voltage Model

The total mobile charges in the channel for the regions, distinctly for internal and external assembly, can be written as:

$$Q_{\text{int}} = Q_{L_1,\text{int}} + Q_{L_2,\text{int}} = C_{ox,\text{int}} \left\lfloor \left(V_{\text{GS}_2} - V_{fb1} - \phi_{\text{s}_1,\text{int}} \right) + \left(V_{\text{GS}_1} - V_{fb2} - \phi_{\text{s}_2,\text{int}} \right) \right\rfloor$$

$$Q_{\text{ext}} = Q_{L_1,\text{ext}} + Q_{L_2,\text{ext}} = C_{ox,\text{ext}} \left\lfloor \left(V_{\text{GS}_2} - V_{fb1} - \phi_{\text{s1,ext}} \right) + \left(V_{\text{GS}_1} - V_{fb2} - \phi_{\text{s}_2,\text{ext}} \right) \right\rfloor$$

As the gate charge is an integral function, the mobile charge density from Source to drain in both the region and therefore, the internal and external gate charge can essentially be written as follows:

$$Q_{\text{G,int}} = -\left(2\pi \text{a}\right) \left[\int_0^{L_1} Q_{L_1,\text{int}} dz + \int_{L_1}^{L} Q_{L_2,\text{int}} dz \right] \tag{7.17a}$$

$$Q_{\text{G,ext}} = -\left(2\pi \text{b}\right) \left[\int_0^{L_1} Q_{L_1,\text{ext}} dz + \int_{L_1}^{L} Q_{L_2,\text{ext}} dz \right] \tag{7.17b}$$

The gate-capacitance due to the internal and external gate can be determined as follows:

$$C_{\text{GS,int}} = \left. \frac{dQ_{\text{G,int}}}{dV_{\text{GS}}} \right|_{V_{\text{DS}}=\text{constant}} \text{; and } C_{\text{GD,int}} = \left. \frac{dQ_{\text{G,int}}}{dV_{\text{DS}}} \right|_{V_{\text{GS}}=\text{constant}} \tag{7.18a}$$

$$C_{\text{GS,ext}} = \left. \frac{dQ_{\text{G,ext}}}{dV_{\text{GS}}} \right|_{V_{\text{DS}}=\text{constant}} \text{; and } C_{\text{GD,ext}} = \left. \frac{dQ_{\text{G,ext}}}{dV_{\text{DS}}} \right|_{V_{\text{GS}}=\text{constant}} \tag{7.18b}$$

Total external gate-capacitance can be written as: $C_{\text{G,ext}} = C_{\text{GS,ext}} + C_{\text{GD,ext}}$, therefore, the total internal gate-capacitance (by neglecting inversion capacitance) can be given as:

$$C_{\text{G,int}} = C_{\text{GS,int}} + C_{\text{GD,int}} \tag{7.19}$$

The minimum value of V_{GS} at which the surface-potential is equal to the double of the fermi-potential results in the threshold voltage that can be as [169]:

$$\phi_{\text{s,int}_{\text{min}}} = \left(2\sqrt{\text{A}_1\text{B}_1}\right) - \beta_1/\lambda_{\text{int}}^2 \text{ at } x_{\text{min}} = \left(2\lambda_{\text{int}}\right)^{-1} \ln\left(\text{B}_1/\text{A}_1\right) \tag{7.20a}$$

$$\phi_{s,\text{ext}_{\min}} = \left(2\sqrt{A_1^{'}B_1^{'}}\right) - \beta_1/\lambda_{\text{ext}}^2 \text{ at } x_{\min} = \left(2\lambda_{\text{ext}}\right)^{-1} \ln\left(B_1^{'}/A_1^{'}\right) \tag{7.20b}$$

and at this point, the value of threshold voltage can be determined as [170]:

$$V_{\text{TH,int}} = -V_{\phi_{L_1,\text{int}}} + \sqrt{V_{\phi_{L_1,\text{int}}}^2 - 4V_{\phi_{L_1,\text{int}}}\xi}\Big/2\xi \tag{7.21a}$$

$$V_{\text{TH,ext}} = -V_{\phi_{L_1,\text{ext}}} + \sqrt{V_{\phi_{L_1,\text{ext}}}^2 - 4V_{\phi_{L_1,\text{ext}}}\xi}\Big/2\xi \tag{7.21b}$$

The threshold voltage of DMG-CSDG MOSFET will be the minimum threshold of both of the assemblies. The short-channel threshold voltage shift ΔV_{TH} of the DM CSDG MOSFET can be written as:

$$\Delta V_{\text{TH,int}} = 2\sqrt{\eta_s \eta_{L_1} e^{-M}} \tag{7.22}$$

where η_s, η_{L_1}, M, and γ are the parameters as follows:

$$\eta_s = V_{\text{bi}} - V_{\text{GS,L}_1\text{int}}^{'} + \left[\Delta V_{fb,\text{int}} \Big/ 2\left(1 + \frac{t_{si}}{2\gamma t_{ox}}\right)\right];$$

$$\eta_{L_1} = \frac{\left(V_{bi} + V_{DS} - V_{gs,L_2\,\text{int}}^{'}\right)\sinh L_1/\lambda_{\text{int}} + \eta_s \sinh L_2/\lambda_{\text{int}}}{\cosh L_1/\lambda_{\text{int}} \sinh L_2/\lambda_{\text{int}} + \sinh L_1/\lambda \cosh L_2/\lambda_{\text{int}}}, \text{ and}$$

$$\gamma = \varepsilon_{si}/\varepsilon_{ox}; M = L_1/\sqrt{2\gamma t_{si} t_{ox}}$$

Further, using the charge sheet approximation method [171], the subthreshold current for the device's portion has been determined at inversion accumulating from weak to strong results in an increased surface charge for the CSDG device, extending the depletion region.

7.3. Model Framework of Device Simulation

The Poisson's equation's numerical solution in two dimensions using Leibmann's iterative method defines the surface-potential for an instantaneously stationary value of

gate-drain voltage [172, 173]. The obtained solution from previous steps is needed to apply to the two-dimensional Schrödinger equation.

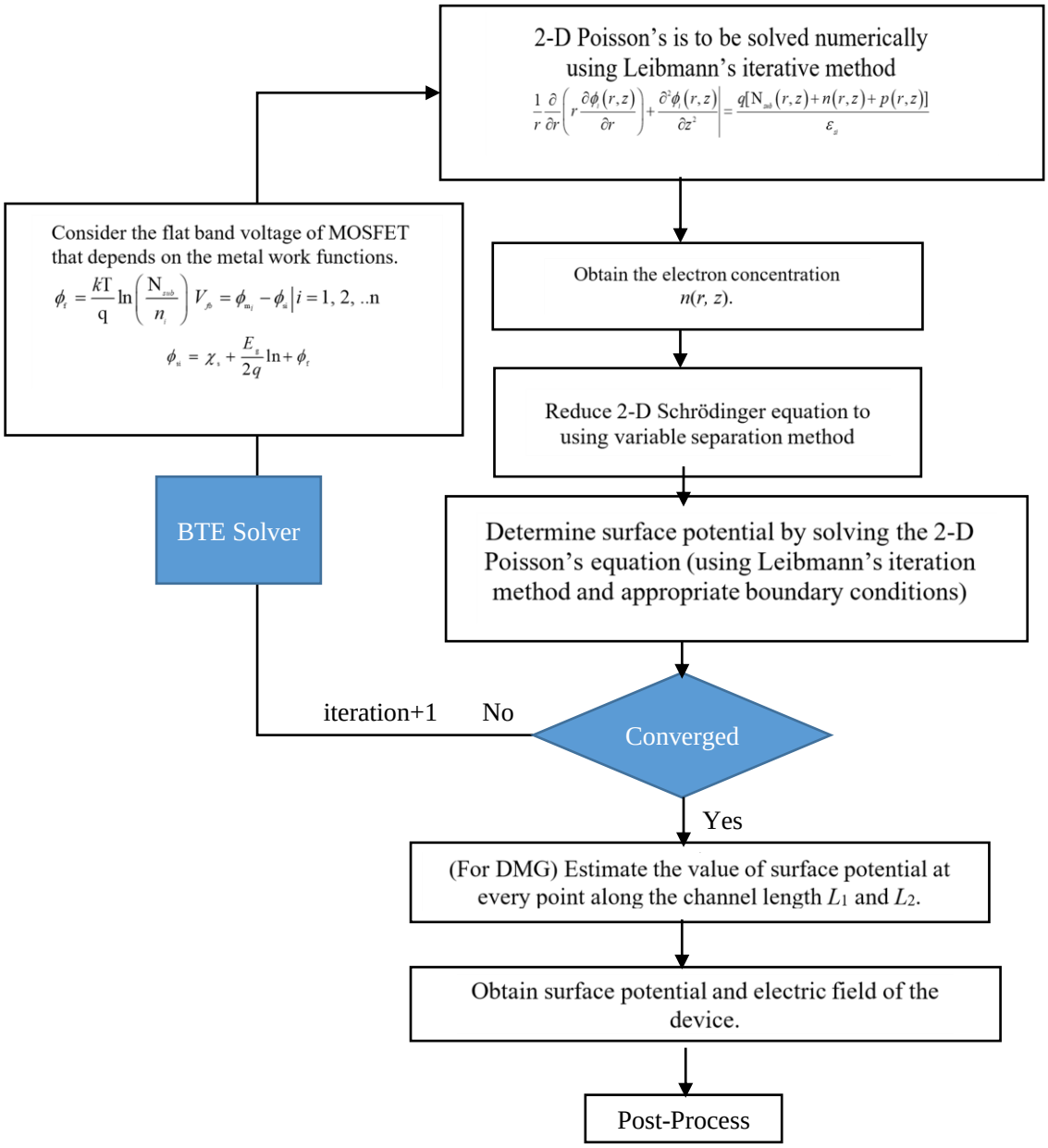


Fig. 7.6. Model framework for the estimation of surface-potential.

The two-dimensional equation can be transformed into a 1-D Schrodinger equation using the separable variation method [174, 175]. As the MOSFET's flat band voltage depends on the metal work-functions keeping metal work-function difference for L_1 and L_2 channel length considering each time, obtain the electron concentration.

The next step is to calculate a new function in the *r*, *z* cylindrical coordinates to obtain the wavefunctions and their corresponding Eigen energies, which leads to a new surface-potential value in each iteration of *i* (*i* =1, 2, 3 to *n*.) Further, computation of the relative error between the original values and those used in the old surface-potential iteration has been done. After repetition until the optimized convergence is achieved, by increasing the number of iterations of boundary condition.

Table 7.1. List of device parameters

Parameter (Unit)	**Symbol**	**SMG**	**DMG**	**stacked-DMG**
Channel Length (nm)	L	20	20	20
Substrate Doping(cm^{-3})	N_{sub}	1×10^{17}	1×10^{17}	1×10^{17}
Source and Drain Doping	N_D	1.6×10^{20}	1.6×10^{20}	1.6×10^{20}
Gate-Insulator Thickness (nm)	t_{ox1}, t_{ox2}	1.5	1.5	1.5
Gate Metal Work-function (eV)	$\phi_{m,int}$, $\phi_{m,ext}$	4.4	4.4, 4.8	4.4, 4.8
Internal Gate Radius (nm)	a	5	5	5
External Gate Radius	b	12	12	12

Table 7.1 lists the dimensional parameters of the CSDG device in the Single Material Gate (SMG), Dual-material Gate (DMG), and the stacked- Single Material Gate (stacked-DMG) structure, as comprehended in Section 7.1.

The potential at subsequent points along the channel length towards the drain end of the device is projected statistically to estimate the characteristics. The work-function of metals M_1 and M_2 of the device's DMG structure are typically chosen 4.8 eV and 4.4 eV, respectively, whereas, in a conventional form as SMG, 4.8 eV has been deliberated as the

gate metal work-function. Excepting the gate metal, other design parameters of both the SMG, DMG, and stacked-DMG are comparable.

7.4. Results and Discussion

The proposed model has been verified using the comparison of the mathematical solution and the simulation for surface-potential distribution along the channel length and the electric field in the device.

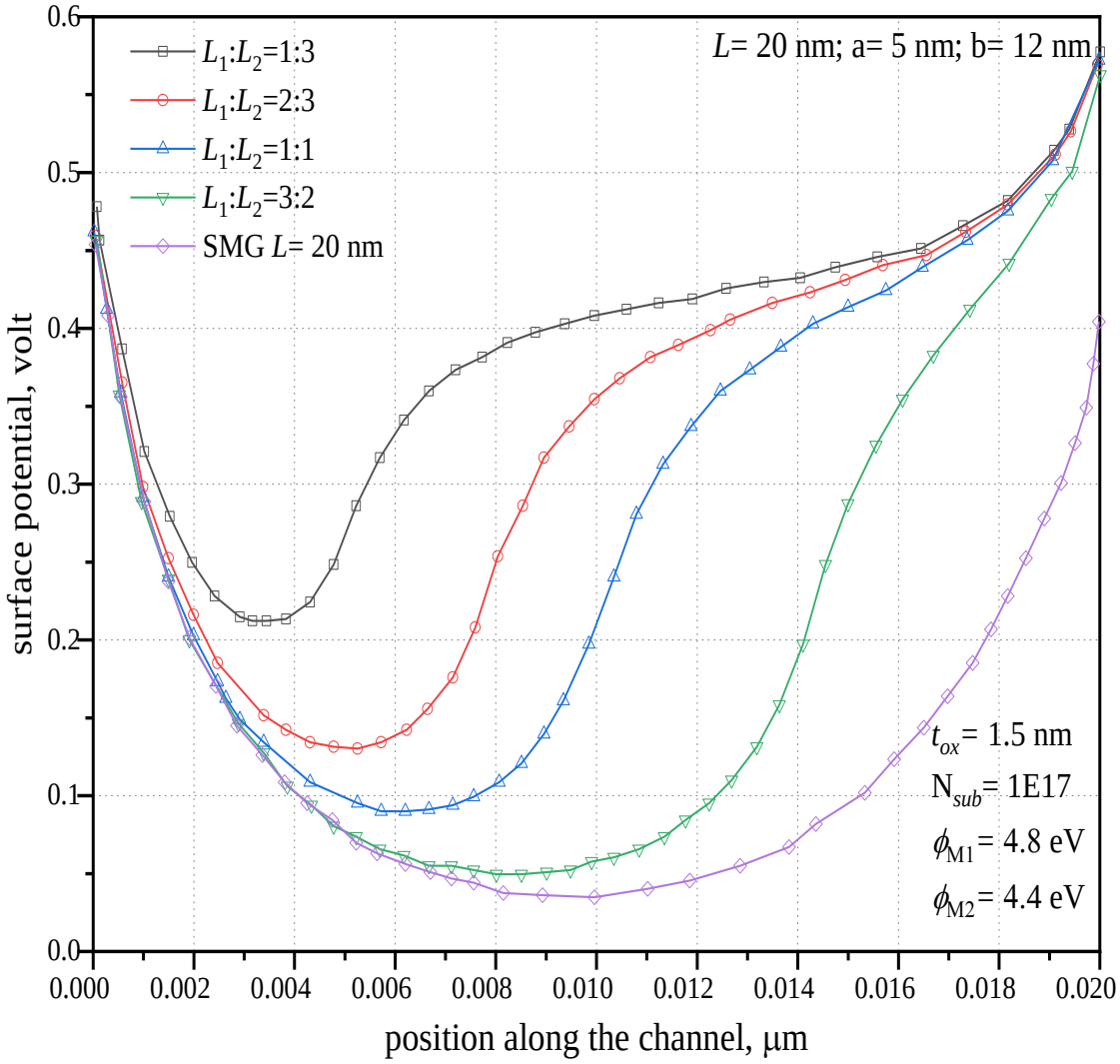


Fig. 7.7. Surface-potential profile versus position along the channel in stacked DMG-CSDG device at varied region lengths.

In the simulation structure, carrier statistics Fermi-Dirac along with the Drift-Diffusion model for carrier transport, have been used to model the simplified nanoscale device. As derived from the modeled expression, the surface-potential distribution against the normalized position along the channel is illustrated in Fig. 7.7 at different region length ratios of L_1 and L_2.

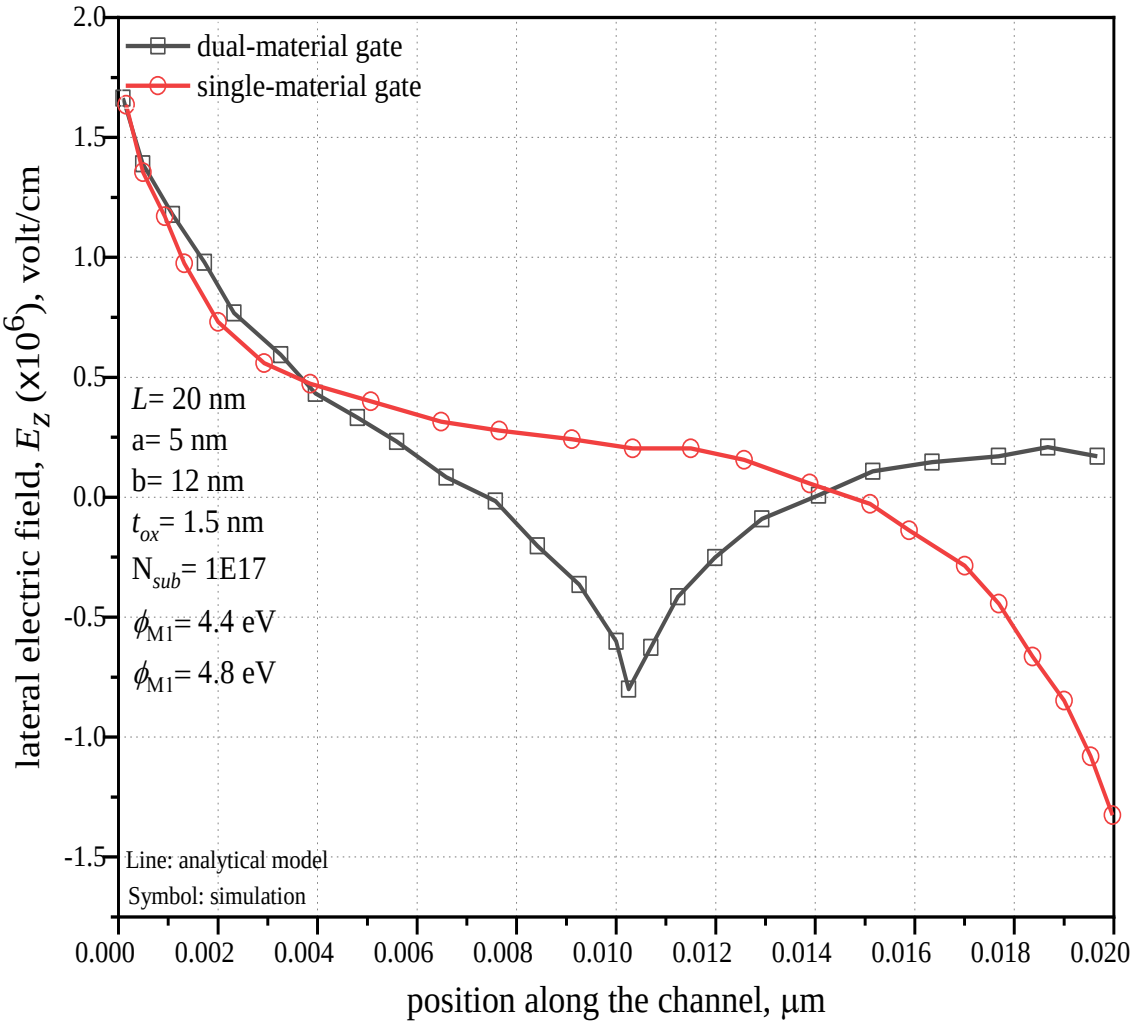


Fig. 7.8. Comparison of electric field profile in dual-metal and single metal gate structures of CSDG MOSFET at L=20 nm, a=5 nm, b=12 nm.

The work-function of metals M_1 and M_2 of the device's DMG structure is typically chosen 4.8 eV and 4.4 eV, respectively, while the conventional design, 4.8 eV, has been deliberated the gate metal work-function. The close agreement between the derived model

has been obtained to validate the model. Excepting the gate metal, other design parameters of both the stacked-DMG and SMG are comparable and indicated in the figure captions. The DMG-CSDG utilizes two different metals, i.e., dissimilar work-function exists; therefore, a stride deviation in the potential near the metal interface exists.

This step-change in the surface-potential in DMG structure leads to the growth in the carrier velocity, which further increases the carrier transport efficiency and that all, in turn, increases the drain current of the device.

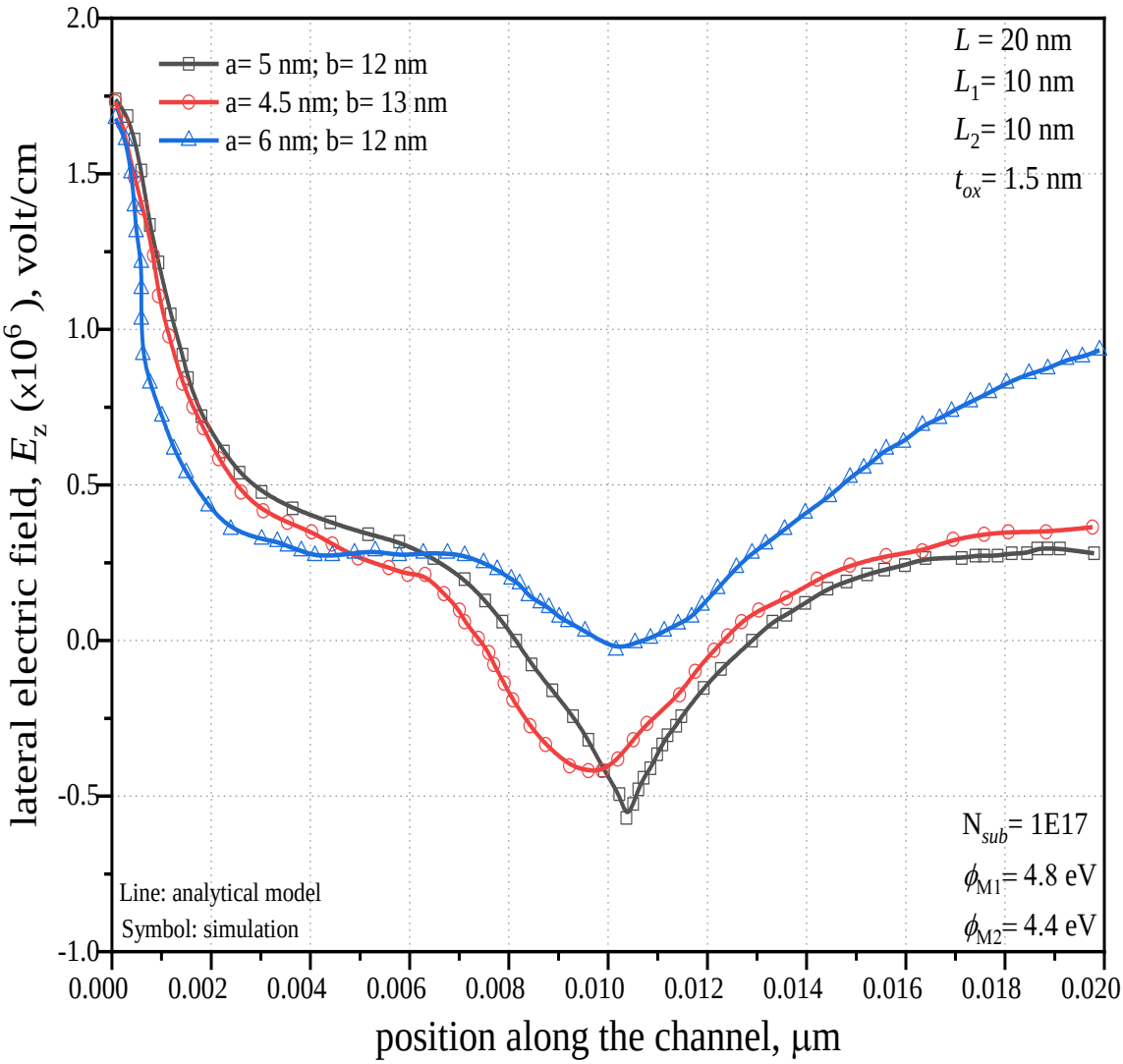


Fig. 7.9. Variation in electric field profile at L_1=L_2 for the different internal and external radius of stacked-DMG-CSDG MOSFET.

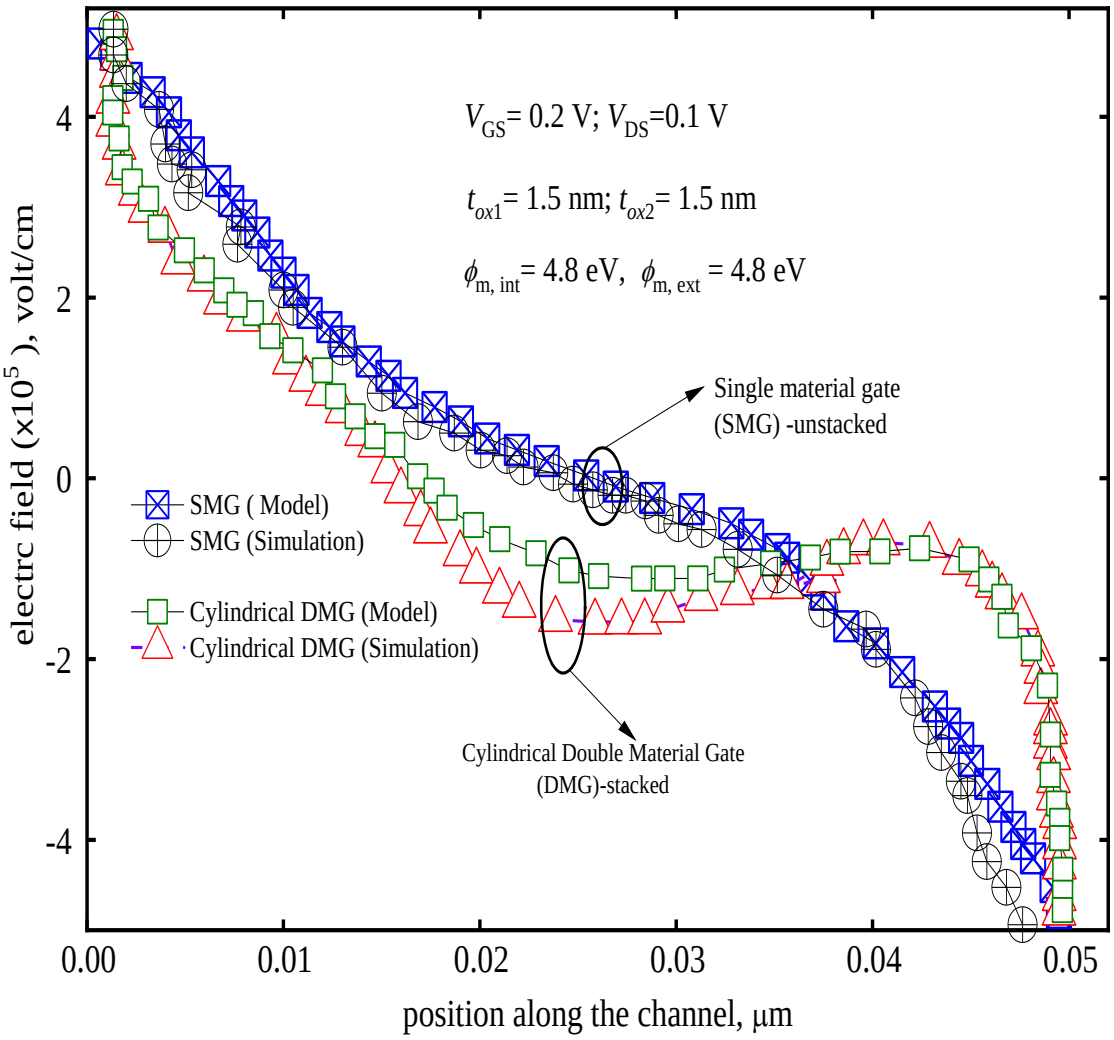


Fig. 7.10. Comparison of lateral electric field distribution in DMG and stacked DMG (at L_1=L_2) device structure L=20 nm, a=5 nm, b=12 nm.

Furthermore, it can be observed that the minima of surface-potential ($\phi_{s_{min}}$), which lies underneath the region-1 of high work-function metal, shifts towards the source side. It reasons the peak electric field to relocate further closer to the source region, and the uniformity of the electric field in the channel enhances. Moreover, the channel potential minima at the different positions of metal interfaces are not the same. It is because of the high work-function of the metal headed to the source side of the channel.

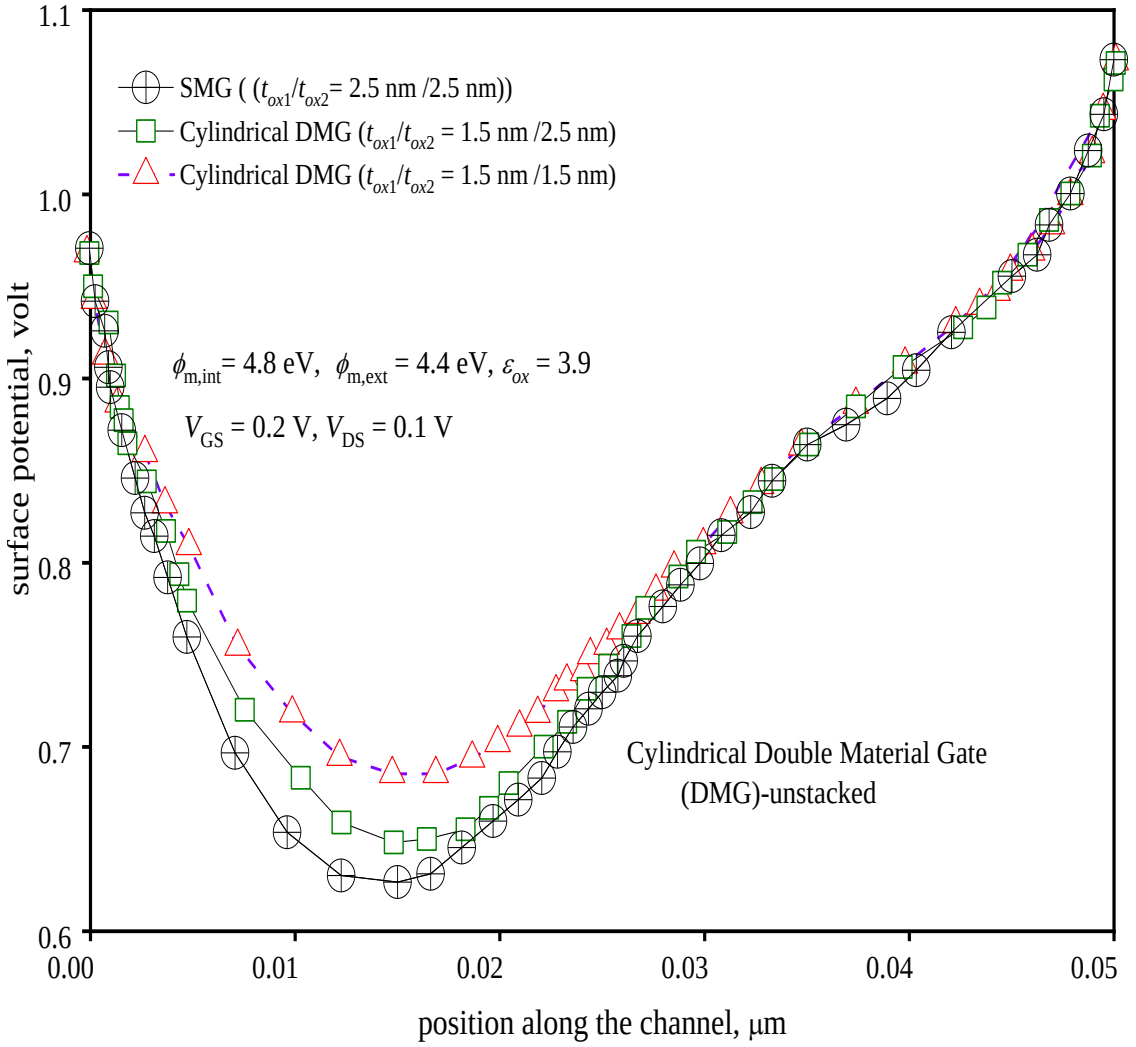
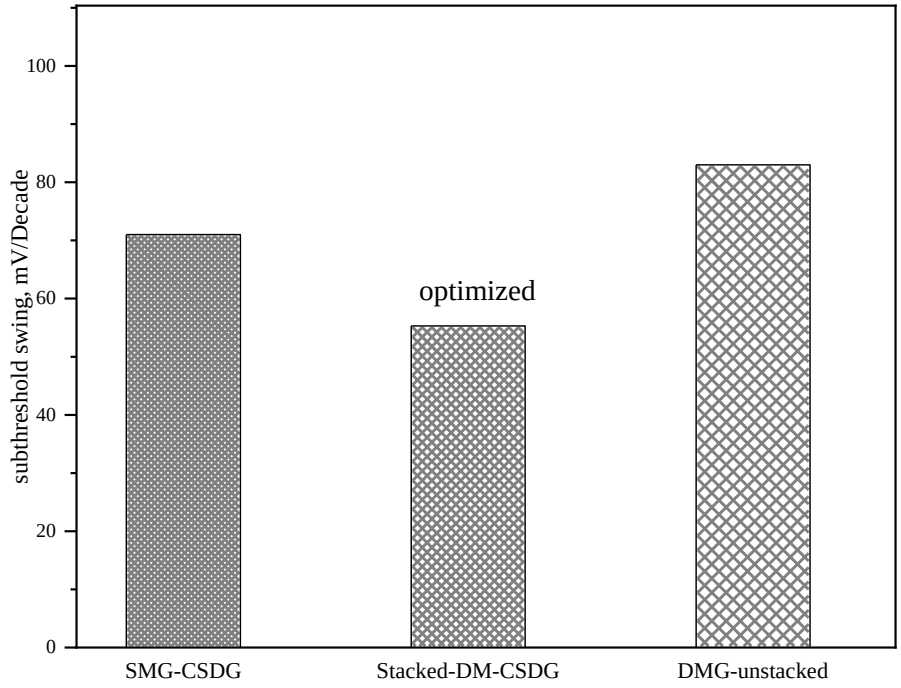
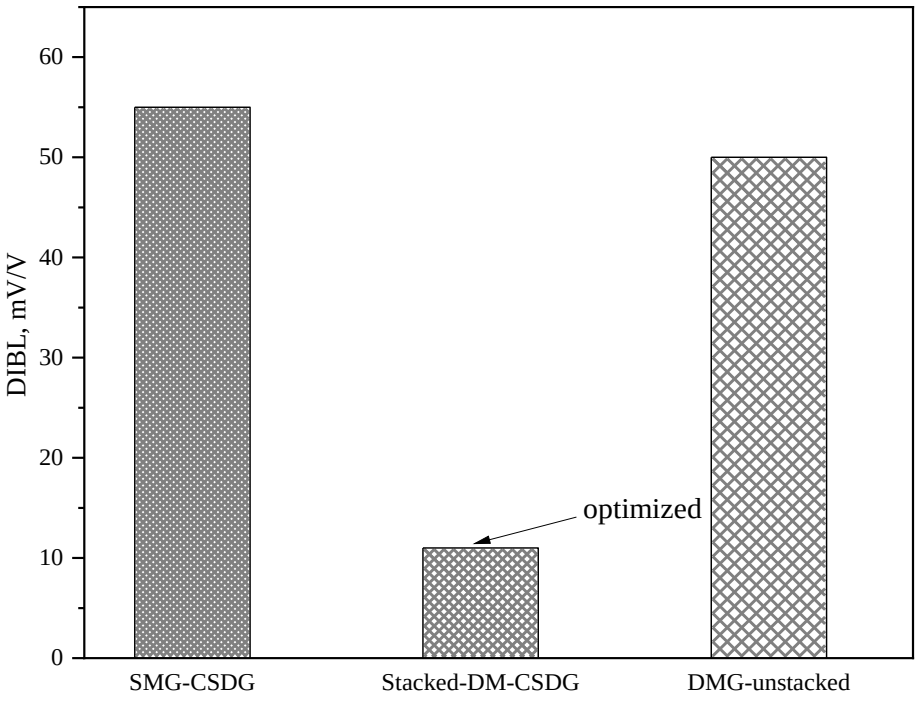


Fig. 7.11. Surface-potential profile as a function of the position along the channel for stacked-DMG-CSDG MOSFET at different gate-oxide thickness.

In DMG, the dependence of minimum surface-potential in the channel can be more effectively reduced by decreasing metal length ratios. Fig. 7.8 shows the result of lateral electric field distribution in dual-metal and single metal gate structures of CSDG MOSFET. The electric field tends to increase near the metal junction (L = 10 nm) in the DMG-CSDG structure, and eventually, that results in increased carrier transport efficiency. The device dimension with a larger internal radius can be comprehended that with a decreasing semiconductor thickness (i.e., b-a), the channel's peak electric field decreases consequently and shifts to the source side.



(a)



(b)

Fig. 7.12. Comparison of the different CSDG MOSFET SMG, DMG, and stacked-DMG structures (a) Subthreshold Swing and (b) DIBL.

As a result, the greater band-bending and increased gate-control are obtainable due to reduced DIBL and threshold voltage roll-off. The distribution of lateral electric field profile with stacked-dual-metal gate structures of CSDG MOSFET obtained by variation of the various internal and external radius is shown in Fig. 7.9. The comparative result of lateral electric field distribution in dual-metal and single metal gate structures of CSDG MOSFET are shown in Fig. 7.10. It is apparent from the figure that the electric field increases near the metal junction (L = 10 nm) in the DMG-CSDG structure, which ensures the ultimate boost in the device's carrier transport efficiency.

Fig. 7.11 shows the surface-potential as a function of position along the channel for stacked DMG-CSDG MOSFET, at V_{DS}=0.1 V and 0.2 V at different oxide thickness of internal and external gates. Furthermore, it can be observed that the minima of surface-potential that lies underneath the region-1 of high work-function metal shifts towards the source side (refer to the valley variation in results). The minimum point of surface potential for an SMG structure is *0.626* V in the position along the channel at 0.015 μm. The DMG structure with an equally thick oxide layer of t_{ox1}/t_{ox2} (i.e., 1.5 nm/1.5 nm) is *0.685* V., but it is interesting to see that when external gate thickness (t_{ox2}) is increased to 2.5 nm, the surface potential fall down to *0.648* V. The obtained value in comparison can be interpreted as a decline of surface potential by the increasing gate oxide thickness of external gate. Because the lower gate metal function interfaces the external side, rather SMG remains unaffected by oxide thickness. The surface potential variation reasons in relocating the peak electric field further close to the source side, and the uniformity of the electric field in the channel enhances. Fig. 7.12 shows the subthreshold and DIBL comparison of simulated device structures. The gate-stack arrangement well recognizes the improvement compared to the SMG and DMG structure of the CSDG device. The comparison of device simulation shown optimized electric field and surface-potential profile.

7.4. Chapter Summary

This chapter presents the analytical modeling of CSDG MOSFET in a DMG structure. The obtained solution from the proposed structure's model expressions has been compared with a single metal gate structure using numerical simulation, and that exhibits an excellent

match with the analytical model. The DMG-CSDG MOSFET structure improves carrier velocity and carrier transport efficiency due to deviation in the surface-potential profile caused by dissimilar gate metal work-function.

The performance comparison of CSDG MOSFET design in a stacked and unstacked arrangement of dual-metal gate structure has been successfully obtained to investigate the surface-potential and electric field distribution with the gate material engineering. It could be established that the gate work-function is responsible for forming a potential channel profile. The surface-potential minima in the DMG-CSDG structure shift the peak electric field, which can be effectually engineered by metal length variation to overcome threshold voltage roll-off. The potential profile along the channel length results in depleting the broader channel region under the internal gate with drain potential variations to help simultaneously in mitigation to SCEs.

Moreover, the channel potential minima at the different positions of metal interfaces are not the same. It is because of the high work-function of the metal headed to the source side of the channel. In stacked-DMG, the dependence of minimum surface-potential in the channel can be more effectively reduced by decreasing metal length ratios and oxide thickness ratios. In conclusion, the DMG device structure results in superior device characteristics that reduce the threshold voltage roll-off and suppression of Hot-Carrier Effects (HCEs) and Short-Channel Effects (SCEs).

Chapter-8

CONCLUSIONS AND FUTURE RECOMMENDATIONS

8.1. Conclusions

This section provides the chapter-wise conclusions drawn from the research work presented in this thesis and outlines the recommended future research work.

In Chapter 3, pinch-off capacitance analysis has been presented for a uniformly doped Cylindrical Surrounding Double-Gate MOSFET. The mathematical analysis reveals that it would be more apt to reconsider the oxide capacitance, unlike a conventional operation being a direct rationale for the device's cylindrical sizes. Instead, the derived expression at the pinch-off operation is a complex algebraic and logarithmic fraction form, involving the external, internal dimensions, thickness, and material properties of the parallel-plate cylindrical capacitive structure of the device. The calculation of pinch-off capacitance can lead to an improvement in the switching characteristics of the overall device.

In Chapter 4, the electric field analysis results show that the electric field in the double-gate structure due to the oxide capacitance is the vector sum of the field generated due to the internal capacitor part (E_1) and an external capacitor (E_2). The CSDG cylindrical structure consisting of infinitesimally small circular rings of uniform charge density and dimensions corresponding to the internal and external assembly radius of the CSDG MOSFET. The mathematical formulation established in this work serves as an essential expression that incorporates the structure design. The analysis could be treated as the foundation of a detailed physical and mathematical model for obtaining channel mobility and electrical characteristics of the device.

In Chapter 5, an analysis to insight into the effect of high-k oxide materials on the development of junction depths has been presented. The depletion width at increasing ε_{ox} (k) values of the oxide material declines at increasing gate potentials, following the short channel. Furthermore, the depletion width under source and drain decreases with increasing oxide thickness (t_{ox}) for the higher values of k.

In Chapter 6, an analysis of results obtained using the derived model of expression for semiconductor thickness dependence based on the simplified device physics has been explored at strong inversion using the perception of depletion depth. The results indicate that low depletion depth under the gate can be attained with high substrate doping and reduces functional silicon thickness. However, the inversion channel formation requires strong surface-potential if the substrate doping increases by double its concentration. Although high doping concentration provides the reduced depth of depletion (d_{dG}), the corresponding channel depth (d_c) is also reduced.

The analysis presented in this chapter significantly contributes to understanding the dependence of semiconductor thickness in CSDG MOSFET. The investigation at strong inversion is significant for deriving the device's comprehensive analytical model, wherein these outcomes could be applied further to determine gate voltage and threshold voltage device model. The condition of a planar MOSFET in channel formation, i.e., for strong inversion, and when $V_{GS} > V_{TH}$ has been considered for this mathematical analysis. The computed results of device thickness and depending parameters for a planar MOSFET and the CSDG MOSFET have been compared. Based on this analysis, the typical CSDG MOSFET calculated silicon thickness is *180 nm*, *281 nm*, and *327* nm at V_{DS} *0.2* V, *0.8* V, and *1.2* V, respectively.

In Chapter 7, a novel model for the analysis of gate-metal engineered CSDG MOSFET structure design has been explored, and a comparison with a single metal gate structure has been presented in terms of gain in the surface-potential and electric field profile of the device. Finally, it has been analyzed that the proposed model exhibits an excellent match with the analytical model. The obtained DMG device structure advances the carrier velocity and transport efficiency, resulting in the surface-potential profile caused by dissimilar gate metal work-function.

In conclusion, the work presented in this thesis contributes as the analytical insights of a novel stacked Dual-Metal Gate (DMG) structure and performance comparison with unstacked DMG structure of CSDG MOSFET in terms of surface potential and electrical field profile. The analytical modeling of CSDG MOSFET in a stacked-Dual-Metal Gate (DMG) structure using the solution of 2D Poisson's equations in their geometrical boundary conditions of the device exhibits an excellent match with the analytical model.

Moreover, the potential profile and channel result in depleting the broader channel region under the internal gate with drain possible variations to help simultaneously in mitigation to SCEs.

The analysis investigates the ability of gate metal variation in channel field formation. It can be concluded from the results that the electric field increases near the metal junction (*L= 10* nm) in the DMG-CSDG structure, which ultimately increases the device's carrier transport efficiency. It has also been apparent from the results at different oxide thickness of internal and external gates of stacked DMG-CSDG MOSFET (at V_{DS}=0.1 V and 0.2 V) that the minima of surface-potential that lies underneath the high work-function metal region-1 shifts towards the source side. The electric field results in the drain side region's displacement closer to the source, enhancing the channel's electric field's uniformity.

The gate-stack arrangement distinguishes the improvement compared to the SMG and DMG structure of the CSDG device. The comparison of device simulation shows a well-optimized electric field and surface-potential profile. It results in a promising improvement in carrier velocity and carrier transport efficiency due to deviation in the surface-potential profile dissimilar gate metal work-function.

8.2. Future Recommendations

As CSDG MOSFETs have been reported for high-frequency applications for high speed, data transmission, antenna, sensor networks, and RF circuits, the proposed work could be an analytical understanding of the capacitance formation in a CSDG MOSFET to incorporate in future work.

The physics-based capacitance analysis presented in this chapter 3 is recommended to apply in scaled DMG and gate-stack DMG structure of CSDG MOSFET. Further recommended to compare and analyze the impact of pinch-off capacitance to distinguish the device performances.

The thickness modeling results proposed in this thesis show that nanoscale CSDG MOSFET can be deployed for improvements in the device performance and novel design modifications. The analysis presented in this work significantly contributes to

understanding the dependence of Semiconductor thickness in CSDG MOSFET and serves as a guide for future device compactness developments.

The gate material engineering has demonstrated the enormous capability of improvements in the device's electrical characteristics. Therefore, the obtained comprehensions of the research design presented in this thesis would undoubtedly guide future efforts, and this specific field would remain fertile for a long time. After the insightful analysis reached in this research work of dual-metal gate design, it is highly recommended to extend the proposed design model of CSDG MOSFET for enumerating the influence on the parameters for velocity saturation and other short-channel effects. Based on the understanding by the device physics presented in this thesis, a small signal model can be derived. The work could be extended in future to see the device operation at high frequencies. Further, the device experimental fabrication can be compared with the obtained characteristics and the numerical results. The presented work opens up the research scope for the DMG CSDG device for circuits and applications in device and circuit simulators.

Moreover, it opens up a path for in the triple-material unstacked and/or stacked implementation to incorporate other gate-material engineering aspects such as the impact of high dielectric material, discrete gate-metal work function, source-drain overlap, and underlap analysis, involving different gate and/or oxide material for the improvement of gate control.

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APPENDIX

The formulation of constants A_1, B_1, C_1, & D_1, and A'_1, B'_1, C'_1, & D'_1 to calculate internal and external surface potential in the device boundary condition, used in Chapter 7 are as follows:

$$A_1 = G_1 \cosh(\lambda_{int} L_2) + E_1 - F_1 e^{-\lambda_{int} L} / 2\sinh(\lambda_{int} L);$$

$$B_1 = G_1 \cosh(\lambda_{int} L_2) - E_1 + F_1 e^{-\lambda_{int} L}$$

$$C_1 = (G_1/2) + 2A_1 e^{\lambda_{int} L};$$

$$D_1 = (G_1/2) + 2B_1 e^{\lambda_{int} L};$$

$$G_1 = (\beta_1/\lambda_{int}^2) - (\beta_2/\lambda_{int}^2);$$

$$E = V_{bi} + V_{DS} - (\beta_2/\lambda_{int}^2);$$

$$F = V_{bi} + (\beta_2/\lambda_{int}^2);$$

The constant A_1, B_1, C_1, and D_1 derived for the boundary condition are:

$$A_1^{'} = G_1^{'} \cosh(\lambda_{ext} L_2) + E_1^{'} - F_1^{'} e^{-\lambda_{ext} L} / 2\sinh(\lambda_{ext} L);$$

$$B_1^{'} = G_1^{'} \cosh(\lambda_{ext} L_2) - E_1^{'} + F_1^{'} e^{-\lambda_{ext} L};$$

$$C_1^{'} = (G_1^{'}/2) + 2A_1^{'} e^{\lambda_{ext} L};$$

$$D_1^{'} = (G_1^{'}/2) + 2B_1^{'} e^{\lambda_{ext} L};$$

$$G_1^{'} = (\beta_1/\lambda_{ext}^2) - (\beta_2/\lambda_{ext}^2);$$

$$E_1^{'} = V_{bi} + V_{ds} - (\beta_2/\lambda_{ext}^2);$$

$$F_1^{'} = V_{bi} + (\beta_2/\lambda_{ext}^2).$$

$$\xi = -(\lambda_{int} - \lambda_{int}^{-1})^2 - 8 - 4(\lambda_{int} + \lambda_{int}^{-1});$$

$$V_{\phi_{L_2,\text{int}}} = -\mathrm{S}_1^2 + \mathrm{S}_2^2;$$

$$V_{\phi_{L1,\text{int}}} = 2\mathrm{S}_1\left(\lambda_{\text{int}} - \lambda_{\text{int}}^{-1}\right) + \mathrm{U}_1(8 - 4\lambda_{\text{int}} - 4\lambda_{\text{int}}^{-1}) + \mathrm{U}_3(8 - 4\lambda_{\text{int}} - 4\lambda_{\text{int}}^{-1}) + \mathrm{U}_2(4 - 2\lambda_{\text{int}} - 2\lambda_{\text{int}}^{-1});$$

$$\mathrm{S}_2 = 4\mathrm{U}_1\mathrm{U}_3(\lambda_{\text{int}} + \lambda_{\text{int}}^{-1}) + 2\mathrm{U}_1\mathrm{U}_2(\lambda_{\text{int}} + \lambda_{\text{int}}^{-1}) - 4\mathrm{U}_2\mathrm{U}_3 - \mathrm{U}_2^2 - 4\mathrm{U}_1^2 - 4\mathrm{U}_3^2;$$

$$\mathrm{S}_1 = \left(\lambda_{\text{int}} - \lambda_{\text{int}}^{-1}\right)\left(2\phi_f + V_{fb_{L_1},\text{int}} + \frac{q\mathrm{N}sub}{k^2\varepsilon_{si}}\right);$$

$$\mathrm{U}_1 = 2\phi_f + V_{fb_{L_1},\text{int}} + V_{bi} + \frac{q\mathrm{N}sub}{k^2\varepsilon_{si}};$$

$$\mathrm{U}_2 = \left(V_{fb_{L_1},\text{int}} - V_{fb_{L_2},\text{int}}\right)k^2\left(\lambda_{L_2,\text{int}}\lambda_{L_1,\text{int}}^{-1} + \lambda_{L_2,\text{int}}^{-1}\lambda_{L_1,\text{int}}\right);$$

$$\mathrm{U}_3 = 2\phi_f + V_{fb_{L_2},\text{int}} + V_{bi} + V_{\text{DS}} + \frac{q\mathrm{N}sub}{k^2\varepsilon_{si}}$$

NOTES