Impact of different pulse width modulation (PWM) techniques on the performance of a three phase Z-Source inverter (ZSI)

By

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ABSTRACT

Traditional voltage source inverters (VSIs) have recently advanced to Z-source inverters (ZSIs). A Z-source inverter is a recent topology of DC-AC inverters that was proposed in 2002 by Prof. F. Z. Peng and has taken over from its predecessors; a voltage-source inverter and a current-source inverter [1], [2], [3]. There were two key modifications applied to VSIs to transform them into ZSIs, viz. the inclusion of a link Z-impedance network between a dc-source and the actual inverter stage (topological amendment); as well the inclusion of the ninth operational state, as opposed to only eight zero and active permissible operating states on VSIs, called the shoot-through state (Control scheme amendment) [2].

In this dissertation, a detailed design of the ZSI is presented. LCL filter is a choice in this design because it gives superb attenuation of -60 Db/decade to switching frequency opposed to LC and L filters whose attenuation is -40 Db/decade and -20 Db/decade respectively [5]. LCL filters are also light in weight, smaller in size and cheaper than LC and L filters for the same rating. Three pulse width modulation (PWM) techniques viz. simple boost control (SBC), constant boost control (CBC) as well as the maximum boost control (MBC); are developed and applied to a ZSI after-which they are compared with each other for critical performance parameters; traditional sine pulse with modulation (SPWM) is only featured as a reference for the other three PWM control techniques sine it does not boost voltage. The boost factor (B), DC-link voltage ($V_{dc\text{-}link}$) and percentage of total harmonics distortion (%THD) are exclusively dependent on the modulation index (m) for all three control techniques. MBC has the highest boost factor and hence the highest DC-link voltage, followed by CBC and SBC coming last; for the same modulation index. MBC has the highest %THD followed by CBC and SBC coming last, for the same modulation index. SBC poses the highest stress on the IGBTs/MOSFETs followed by MBC and CBC coming last; for the same gain [4] [5].

Addition of two parallel capacitors C_{p1} and C_{p2} across inductors L_1 and L_2 respectively, to form a different topology called a Capacitor-Boosted-Z-Source Inverter (CB-ZSI) has proven to improve the response of this topology relative to a classical ZSI. The boost factor of CB-ZSI is increased by more than 56% at SBC technique, more than 25% at CBC technique and more than 14% at MBC technique on average. Since the gain factor is a linear function of a boost factor with the proportionality constant being the modulation index, the percentage of improvement of gain factors from ZSI to CB-ZSI remains the same as that of boost factors across SBC, CBC and MBC techniques. The voltage stress ratio across the switching devices of a CB-ZSI is reduced by more than 40% at MBC technique, more than 5% at CBC control and increased by 1.7% for MBC PWM control technique on average. %THD for CB-ZSI is reduced by more than 112% for SBC technique, more than 16.8% for CBC and increased by more than 24% for MBC technique on average

In general, CB-ZSI topology shows improve response and hence improved power quality compared to a classical ZSI topology and also proves to be more economical. The rating of switching devices is reduced due to reduced voltage stress posed by a CB-ZSI compared to a ZSI. The ratings of the passive components forming an impedance network are also reduced because a CB-ZSI achieves a large boost factor at a shorter shoot-through time intervals and hence higher modulation index compared to a ZSI.

DECLARATION

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I Mbulelo Siyabonga Perfect Ngongoma declare that

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

VSI	Voltage-Source Inverter
CSI	Current-Source Inverter
ZSI	Z-Source Inverter
CB-ZSI	Capacitor Boosted-Z-Source Inverter
PWM	Pulse Width Modulation
SBC	Simple Boost Control
CBC	Control Boost Control
MBC	Maximum Boost Control
SPWM	Sine Pulse Width Modulation
UPS	Uninterruptible Power Supply
DVR	Dynamic Voltage Restorer
PV	Photo-Voltaic
VSD	Variable Speed Drive
MPPT	Maximum Power Point Tracking
EMI	Electro-Magnetic Interference
K-map	Kanaurgh-Map
POS	Product Of Sums
SOP	Sum Of Products
SANS	South African National Standards
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor

1. INTRODUCTION

1.1. Introduction of the research work undertaken

This research study investigates a DC-AC converter called a Z-source inverter (ZSI). A ZSI is a novel topology of a DC-AC converter that was proposed in 2002 by Professor F.Z. Peng and has proven to overcome most of the performance issues faced with the traditional topologies which are the voltage-source inverters (VSI) and current-source inverters (CSI). This has led to ZSIs and ZSI related projects appearing more frequently in literature and finding applications in industries [1], [2], [3].

Therefore, this particular study focuses on the capability of ZSI at different operating input conditions and different PWM control techniques and hence proposes a different topology of an inverter aimed to improve performance capacity relative to that of a classical inverter.

1.2. Motivation

ZSIs have numerous renewable energy and industrial applications. Renewable energy applications include photo-voltaic (PV) power and wind power while industrial applications include uninterruptible power supplies (UPS), voltage sag mitigation (DVR), etc.

Solar power or more specifically photovoltaic power is one of the most promising sources of electrical power for the future. This is due to the capability of distributed PV (photovoltaic) generators to be synchronized to the national utility grid. Apart from augmenting the capacity of distribution systems, PV systems have various other benefits such as deferring capital investments on distribution and transmission systems, improving power quality and improving system reliability [4], [5]. A maximum power point tracking algorithm (MPPT) has been proposed to maximize the yield of PV power systems which is also one of the reasons behind PV grid-tie systems' success [5]. Figure 1.1 below shows a photovoltaic cell connected to a ZSI for the above-stated application.

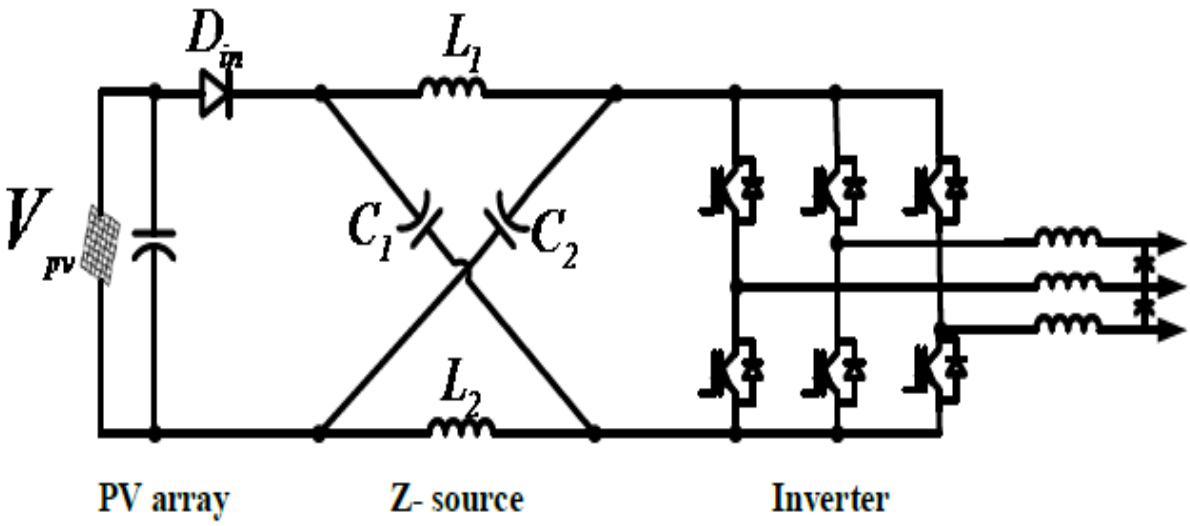


Figure 1.1: PV-cell connected to a ZSI [4]

It is approximated that 100 Giga-Watts can be harvested from off-shore winds across the globe [6]. However; off-shore wind farms are usually far away from areas where power is required which calls for lengthy transmission systems. These transmission systems are associated with transmission losses and transmission voltage drops and hence high gain transformers are normally required part of a transmission system thus implying more costs to transmission systems. Incorporation of a ZSI in a transmission system renders a high gain transformer redundant because a ZSI can boost up to infinity (theoretically) and when used with a properly designed filter they eliminate a large amount of harmonics distortion [2], [6]. Figure 1.2 below shows a wind turbine connected to a ZSI through a full bridge rectifier for the above-stated application.

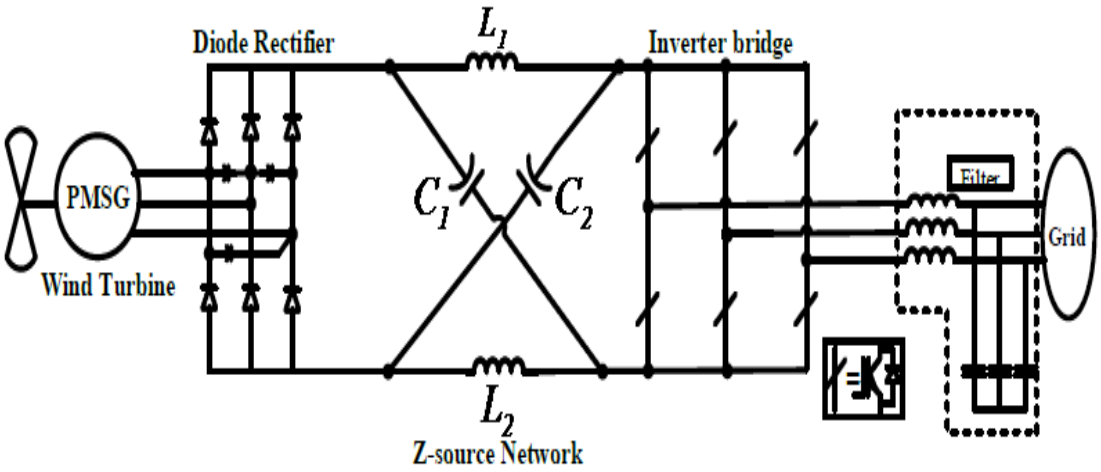


Figure 1.2: Wind turbine connected to a ZSI [6]

Uninterruptible power supplies are devices that provide power to critical loads when the main power fails. Transformers or DC-DC convertors (boost converters) can be used to step-up the voltage in a UPS, however; using a ZSI for this purpose results in much better performance of a UPS. ZSIs give UPSs a capacity of higher peak-to-peak output voltage as compared to when a

transformer or a boost converter is used for the same purpose. ZSIs together with filters reduce the percentage of total harmonics distortion caused by linear or unbalanced loads connected to a UPS [7]. Figure 1.3 below shows a circuit diagram of a ZSI based UPS system.

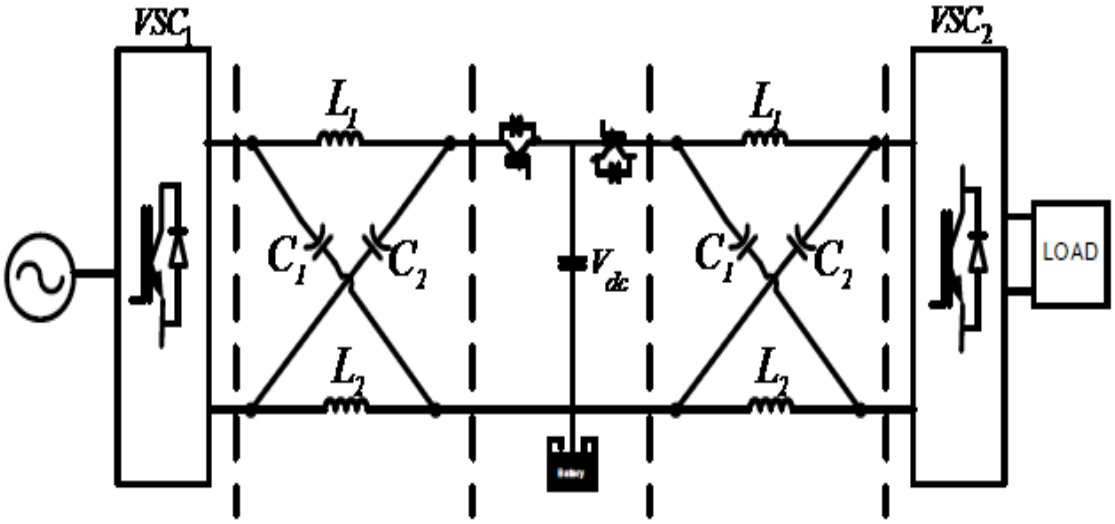


Figure 1.3: ZSI based UPS system [7]

It is approximated that 92% of electrical power systems disturbances is due to voltage sags [8]. Therefore, voltage sags incur serious economic losses to industry and as a result, sensitive equipment should be protected against them. Voltage sag is a sudden reduction in amplitude of a voltage signal by between 0.1 to 0.9 pu (per unit) [8], [9]. Voltage sags are usually mitigated via dynamic voltage restorers (DVR). These devices inject an appropriate amount of voltage, depending on the amount of sag, in series with the supply terminals to compensate for the voltage drop it sees.

Classical DVRs contain voltage source (VSI) inverters however with voltage limitations since VSIs have output voltages of equal or less than its input voltage. Nowadays DVRs are increasingly being based on ZSIs since they overcome most issues (boost factor, reliability, %THD, ETC) faced with VSIs based DVRs [8], [9]. Figure 1.4 below shows a ZSI base DVR connected in series between a source and a load.

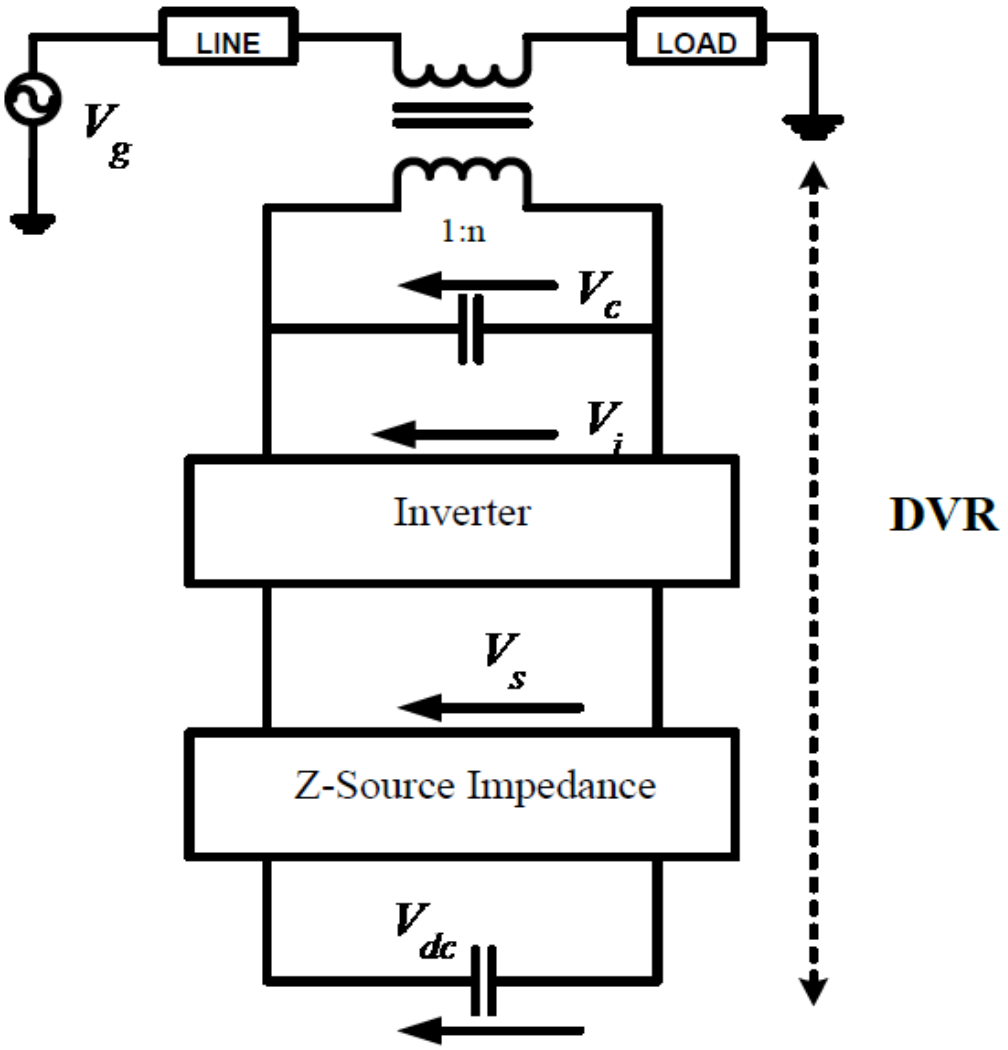


Figure 1.4: ZSI based DVR system [9]

Other applications of ZSIs include variable speed drives (VSD), vehicular drives, grid-tie systems, etc. Literature shows that there are numerous uses of ZSIs which render the study of this dissertation relevant since ZSIs are a focus of researchers and have a significant role in the recent technology of convertors.

1.3. Research question

The problem statement for this research study is to investigate the performance impact of different pulse width modulation (PWM) techniques on a three-phase Z-source inverter. The knowledge gain from the aforementioned study is used to propose a different inverter topology whose performance should show improvement from that of a classical Z-source inverter.

1.4. Background

From the date when ZSIs were proposed, a substantial amount of have been published under the name of these inverters [10], [11]. Miao Zhu et al. proposed a switched inductor Z-source inverter (SL-SZI). Figure 1.5 below shows a circuit diagram of an SL-ZSI. This inverter has a DC-power source in series with an input diode D_{in}, an SL-impedance network and a three-phase universal bridge. An SL-impedance network is a distinction of an SL-ZSI from a ZSI. SL-impedance network has two additional inductors L_3 and L_4 as well as 6 diodes D_1 to D_6 on top of two capacitors and two inductors (L_1, L_2 and C_1, C_2) that a traditional Z-impedance network has.

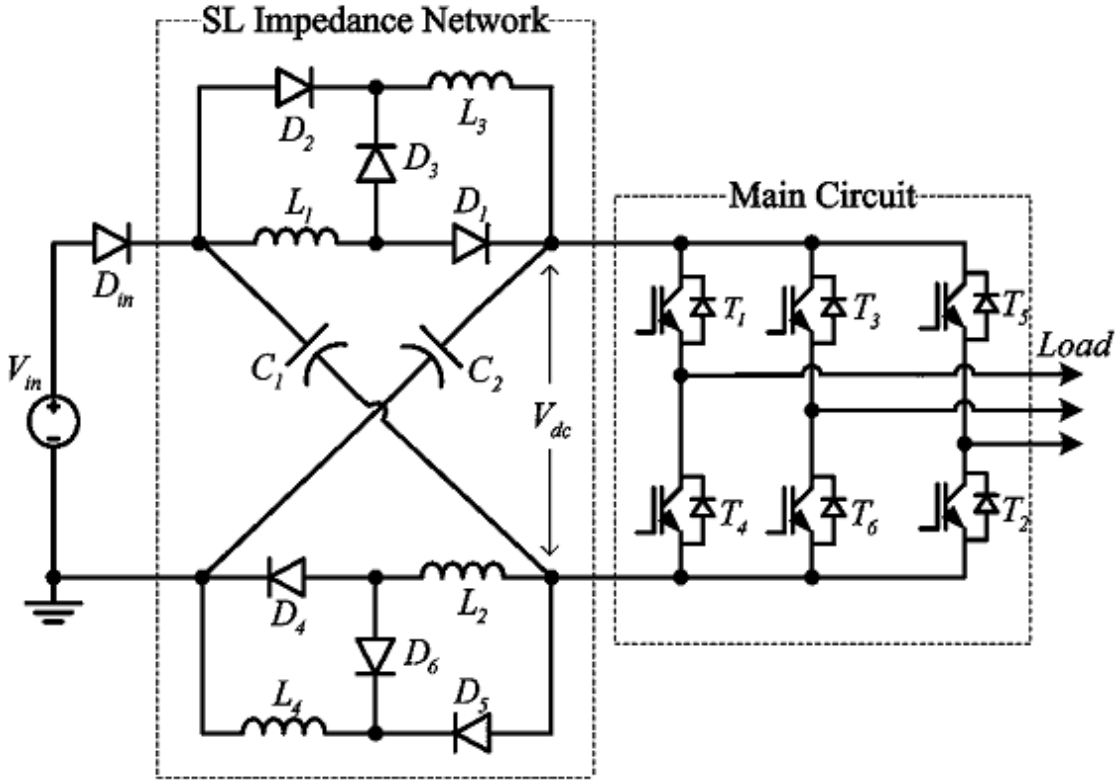


Figure 1.5: A switched inductor Z-source inverter [10]

This topology proved to improve voltage adjustability. The voltage boost is greatly improved. This occurs because, for an SL-ZSI, a very short shoot-through time interval T_0 is required to obtain large voltage gain that would otherwise require a much longer shoot-through interval in a classical ZSI. This has a good overall impact on the quality of output waveforms of an SL-ZSI by reducing the percentage of total harmonic distortion (%THD). SL-ZSIs also offer voltage buck ability that needs low AC voltage and the concept of SL-ZSIs can find application in AC-AC, DC-DC, and AC-DC apart from DC-AC converters. PWM control techniques known to literature such as SBC, CBC, MBC, etc. apply to SL-ZSIs [10], [11].

M. Adamowicz and S. Diva et al. proposed trans-Z-source inverters. In their work, they proposed an Inductor-Capacitor-Capacitor-Transformer-Z-source inverter (LCCT-ZSI) and an inductor-capacitor-capacitor-transformer-quazi-Z-source inverter (LCCT-qZSI). Figures 1.6 and 1.7 below show an LCCT-ZSI and an LCCT-qZSI respectively [9].

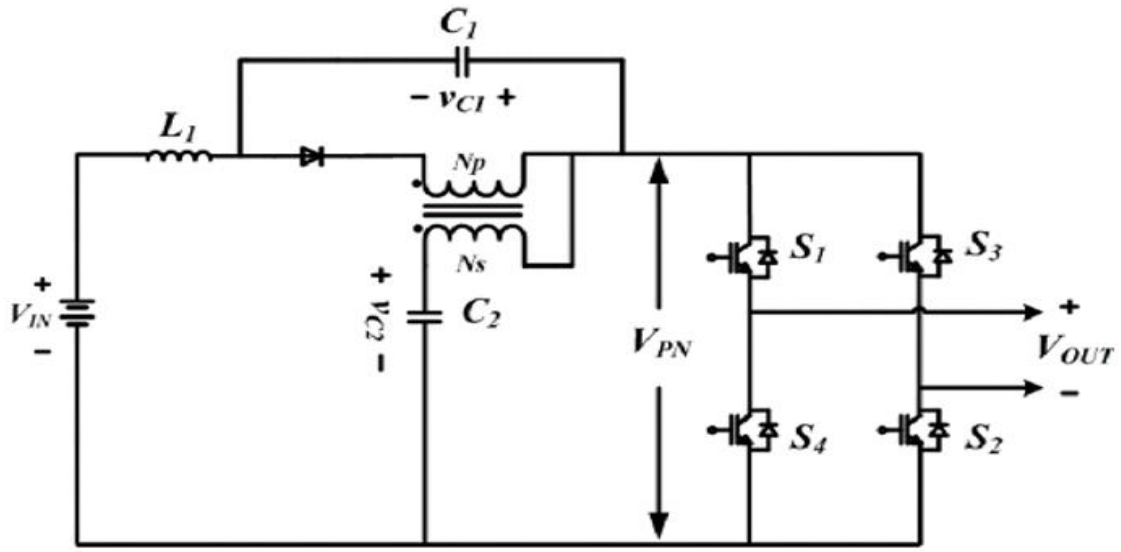


Figure 1.6: An LCCT-ZSI [13]

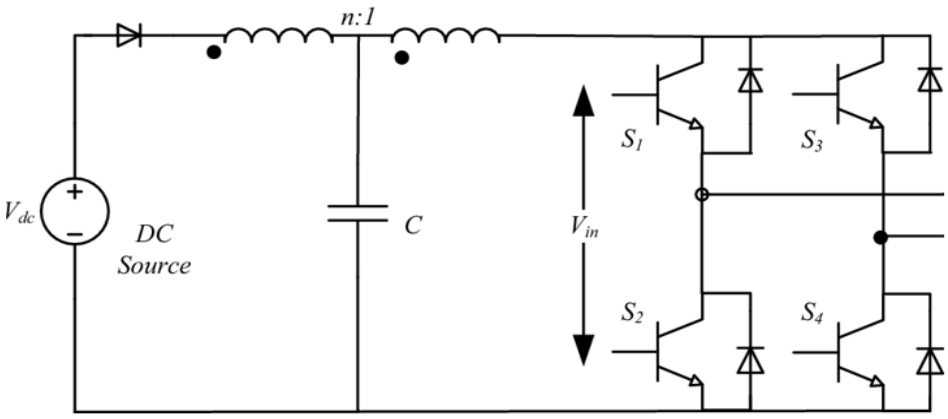


Figure 1.7: An LCCT-qZSI [13]

LCCT-ZSI in figure 1.6 holds two capacitors connected on either side of a transformer to prevent the transformer core from blocking DC [9]. LCCT-qZSI in figure 1.7 contains one capacitor connected shunt to a transformer to suppress voltage ripples at the transformer output [12]. Both topologies show significant improvement on the boost and hence the gain factor on the overall inverter, however; an LCCT-ZSI supersedes LCCT-qZSI in the voltage boosting capability because of capacitor C_1 which maintains a residual voltage across the impedance network at steady state [9], [12]. LCCT-qZSI shows great power conversion efficiency over LCCT-ZSI because of the LCCT-qZSI's impedance network ability to store more energy compared to LCCT-

ZSIs. In both LCCT-ZSIs and LCCT-qZSIs; greater voltage gains are possible by decreasing a transformer's turn's ratio [9].

S.M. Dehghan et al. proposed topology of Z-source inverter with two dc inputs and two ac outputs, termed a dual-input-dual-output Z-source inverter (DIDO-ZSI) [9]. Figure 1.8 below shows a circuit diagram of DIDO-ZSI.

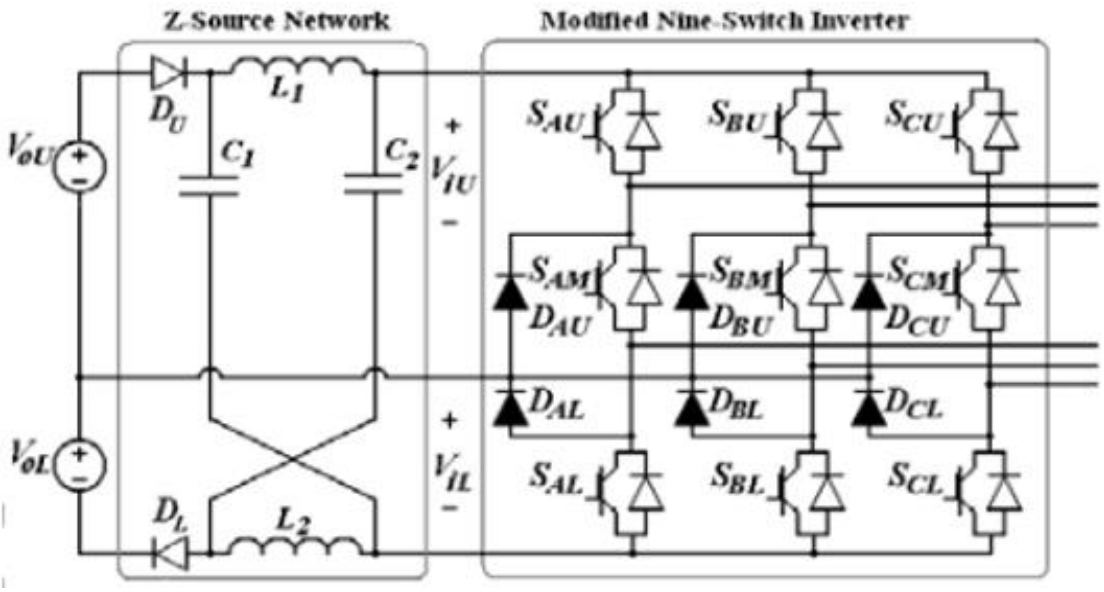


Figure 1.8: A DIDO-ZSI circuit diagram [17]

This inverter has two DC input power sources and two three-phase outputs. An impedance network is similar to that of a classical ZSI except for an additional diode D_L connected in series to L_2. The inverting stage is made of nine switching devices hence its name, the nine-switch inverter. Each of these switching devices has an anti-parallel diode or free-wheeling diode. This diode provides a bidirectional current flow and unidirectional voltage blocking capability. A DIDO-ZSI is composed of two upper and lower inverters. Three upper switching devices, three mid-switching devices and three lower diodes (D_{AL}, D_{BL} & D_{CL}) form the upper inverter [13], [14].

The output of the upper inverter is connected to the positive terminal of V_{iU} via upper switching devices and is connected to the negative terminal of V_{iU} via mid switching devices and lower extra diodes. The lower inverter includes three mid-switching devices, three lower switching devices and three upper extra diodes (D_{AU}, D_{BU} & D_{CU}). The output of the inverter is connected to the positive terminal of V_{iL} via mid-switches and upper diodes and connected to the negative terminal of V_{iL} via lower switches [9], [13], [14].

This inverter can boost a DC voltage to any required level and can control amplitude, frequency, and phase independently [13]. DIDO-ZSI can be used in applications that require two unregulated

DC-power sources feeding two independent loads. Both AC outputs remain operational even if one DC-power source is lost. This topology requires much less passive components rating as compared to those that would have been required in two independent ZSIs of the same capacity as one DIDO-ZSI [13].

Apart from the above-mentioned pieces of work, a lot more has been done under the name of Z-source inverters. *A. Pattanaphol et al*. used Z-source inverter to study the shading issue of photovoltaic cells [9]. Po Xu et al. introduced Z-source inverter for grid associated photovoltaic systems termed solar-powered grid-tie Z-source inverters [5]. *Omar Ellabban et al.* proposed a technique to control the speed of the motor using a bidirectional Z-source inverter [15] . *R. Senthikumar et al.* proposed a Z-source inverter for uninterruptible power supply (UPS) applications [16].

Therefore, when looking at the time when Z-source inverters were first introduced (2002) against the amount of work that researchers have done since then, one can conclude that Z-source inverters have taken attention of many researchers and that they are one successful family of power convertor that has found many different applications in our modern world.

1.5. Thesis aims and objective

The purpose of this research is to study the behaviour of a ZSI in response to different PWM control techniques or rather; the effect of different PWM techniques on a ZSI over a range of operating conditions. Furthermore; the knowledge gained from the latter mentioned study is then to be carefully utilized to develop an amendment to a classical ZSI to improve its response to the PWM control techniques, hence improving the power quality of a ZSI. Therefore; this study broadly separates a design of a ZSI into two main tasks, viz. the design of the main ZSI circuit as well as the design of a PWM control technique modulation a ZSI to output a desired waveform.

A ZSI is designed after which three most common PWM control techniques in literature [5], [17], [18]; viz. simple boost control (SBC), constant boost control (CBC), as well as maximum boost control (MBC), are formulated. These PWM control techniques are then applied to a ZSI and the operating conditions such as an input voltage (V_{in}) and modulation index (m) are varied while paying close attending to the key performance parameters of a ZSI. The key performance parameters include DC-link voltage ($V_{DC\text{-}link}$), boost factor (B), Gain factor (G), Output voltage amplitude (V_{ac}), Voltage stress across switching devices (V_{stress}) as well as the percentage of total harmonic distortion (%THD).

The relationships between the input and/or performance parameters are studied and understood. The gained knowledge is hence used to propose a different topology called Capacitor Boosted-

Z-Source Inverter (CB-ZSI). The naming of this topology is motivated by the fact that an amendment was done on a Z-impedance network of a classical ZSI in to transform it into a CB-Z-impedance network.

This proposed topology aims to improve the performance of an inverter and hence its output power quality by improving the key performance parameters (boost factor, gain factor, voltage stress across switching devices, etc.) in response to a range of input variables (input voltage, modulation index) at different PWM control techniques. The key performance parameters of a ZSI should serve as the asymptotes (baseline) for those of a CB-ZSI; that is, CB-ZSI's key performance parameter should always be better than those of a ZSI.

1.6. Thesis organization

Chapter 2 explains the theoretical background on three-phase Z-source inverters, three-phase low-pass filters and different PWM control techniques for three-phase Z-source inverters. The merits of ZSIs over voltage-source and current-source inverters are stated and the operation of ZSIs is explained in detail hence formulating the inverters' output equation. LC and LCL filter advantages and disadvantages are discussed based on their appropriateness to ZSI's power quality improvement. Lastly, simple boost, constant boost and maximum boost PWM control techniques are discussed stating distinctions amongst each other.

Chapter 3 discusses the methodology of this paper. The sequence of design and techniques used in the design of the simulation is explained. The method of collecting data from the simulated prototype is also explained which includes a specific design of data collection tables and the selection of ranges in which data is collected. Lastly, the criteria for judging improved or worse performance for the proposed CB-ZSI in chapter 5 is explained.

Chapter 4 implement what has been discovered in the literature in chapter 2. A classical ZSI is designed and implemented in MATLAB/SIMULINK. Simple boost, constant boost and maximum boost are also designed and applied to a ZSI. Input parameters are varied while collecting data for each PWM control technique using a specially designed table in chapter 3 to collect enough data. The collected data is then analysed and the conclusion is made on the performance of a ZSI at these different PWM control techniques.

Chapter 5 proposes a new topology, called a CB-ZSI, whose aim is to improve the performance from that of a classical topology investigated in chapter 4. Simple boost, constant boost and maximum boost PWM control techniques are applied to this topology while collecting the same data that was collected for a classical ZSI in chapter 4. This data is analysed and results are compared to baseline results that were obtained in chapter 4. A conclusion is then made on

whether a CB-ZSI has improved or worse performance relative to a classical ZSI based on criteria stated in chapter 3.

Chapter 6 gives an overall conclusion of this paper. In this chapter, it is stated whether the main aim and objectives stated in chapter 1 were fulfilled or not. If not; what more actions could have been done to fulfil them? Chapter 6 also features a summary of future directions to build on top work presented by this research study.

2. LITERATURE REVIEW

A Z-source inverter is a recent topology of inverter that was proposed in 2002 by Professor *F. Z. Peng* [6], [8], [9]. Before its proposition, a voltage-source and a current-source inverter, abbreviated as VSI and CSI respectively, were the common topologies used for inverting related applications such as interfacing the PV power to the utility grid [6], [7], [9], [13].

2.1. A voltage-source inverter (VSI)

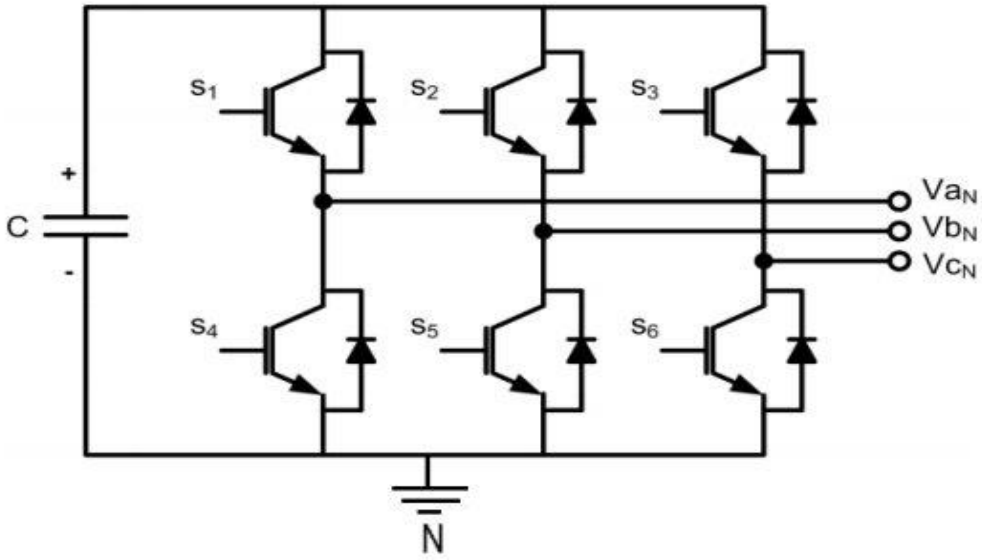


Figure 2.1: A traditional VSI [8]

Figure 2.1 shows a basic circuit of a traditional three-phase voltage-source inverter. A DC power source in parallel with a relatively large capacitor forms a DC voltage source that feeds the main inverting stage. Depending on the application of a VSI; a DC power source can be a battery, fuel cell stack, diode rectifier, and/or capacitor [8]. In a PV system application, a DC power source is a PV cell or an array of PV cells [3], [6]. A bridge comprises six electrical controlled switching devices (IGBTs/MOSFETs) each comprising of a power transistor and an anti-parallel or free-wheeling diode. This diode provides a bidirectional current flow and unidirectional voltage blocking capability. Despite VSIs' popularity in converting applications, it has conceptual and theoretical barriers and limitations [3], [6], [7], [9], [13].

The output voltage of a VSI is either limited to voltages ranging below or above the DC-link voltage. That is, the VSI either boosts or bucks the input voltage. When operating in the inverter mode (DC-AC power flow) the VSI bucks the input voltage and boost it in the rectifier mode (ACDC power flow). For applications where overdrive is desirable and the available dc voltage is limited, an additional dc-dc boost converter stage is needed to obtain the desired ac output.

This additional stage increases the overall costs of the system and compromises the overall system's efficiency [6], [7], [9].

The upper and lower switching devices of the same phase leg cannot be simultaneously gated-on as this would cause a shoot-through condition (single-phase leg, any two-phase legs or all three-phase legs shorted) consequently destroying a VSI. In some cases, electromagnetic Interference (EMI) noise mistakenly gate-on switching devices resulting in a shoot-through condition and that is a major drawback to VSI's reliability. In response to this issue with VSIs, engineers have adopted 'dead time' to block upper and lower switching devices from switching-on simultaneously thus preventing a shoot-through condition from occurring. However; 'dead-legs' results in more waveform distortion, etc. thus compromising the quality of the output power [3], [6], [7], [9], [12], [13].

2.2. A current-source inverter (CSI)

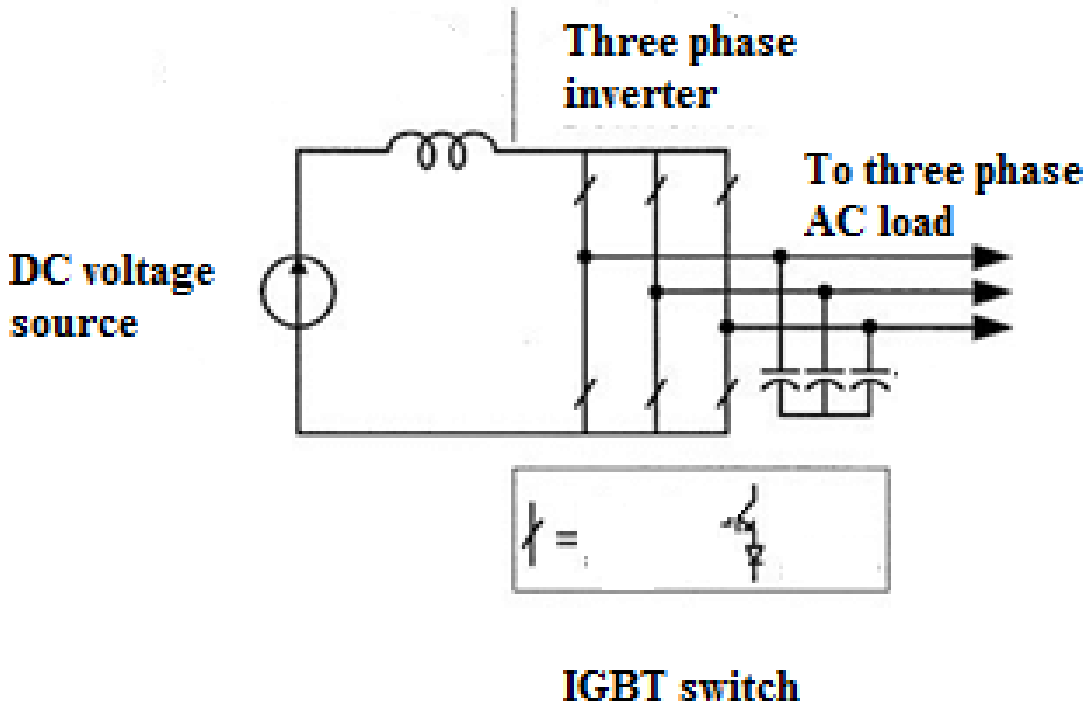


Figure 2.2: A traditional CSI [19]

Figure 2.2 shows a basic circuit of a traditional three-phase current-source inverter. A DC source is formed by connecting a DC power source in series with a relatively large inductor. The switching devices (IGBTs/MOSFETs) are traditionally composed of power switching devices with reverse block capability such as a gate-turn-off thyristor (GTO), silicon controlled switches (SCR) or power transistors with series diodes. These series diodes provide unidirectional current

flow and bidirectional voltage blocking capability. A CSI also has conceptual and theoretical barriers and limitations [1], [11], [17], [19].

Similar to the VSIs, the output voltage of the CSI is either limited to voltages ranging below (bucks) or above (boosts) the DC-link voltage. When operating in the inverter mode (DC-AC power flow) the CSI bucks the input voltage and boosts it operating in the rectifier mode (AC-DC power flow). For applications where overdrive is desirable and the available dc voltage is limited, an additional dc-dc boost converter stage is needed to obtain the desired ac output. This additional stage increases the overall costs of the system and compromises the system's efficiency [12], [17].

At least one upper switching device and one of the lower switching devices should be gated on and maintained so at any time. Else, the open circuit of a DC inductor would occur consequently destroying the inverter. In some cases, Electromagnetic Interference (EMI) noise mistakenly gate-off the switching devices resulting in the open circuit of the DC inductor and that is a major drawback to CSI's reliability. In response to this issue with CSIs, engineers have adopted 'overlap time' for safe current commutation to prevent this open circuit of a DC inductor condition from occurring. However; 'overlap time' results in more waveform distortion, etc. thus compromising the quality of the output power [7], [9], [12].

The main switching devices of a current source inverter have to block reverse voltage; that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBT). This prevents the direct use of low-cost and high-performance IGBT modules and intelligent power modules (IPMs) [10], [17], [19].

On top of the above-mentioned issues with regards to VSIs and CSIs, both these inverter topologies also suffer some common drawbacks. VSIs and CSIs either buck or boost the input voltage, they cannot buck-boost. This implies that the obtainable output voltage is limited to voltages either greater or below the input voltage [1]. The main circuitries of VSIs and CSIs are not interchangeable. The main circuit of the VSI cannot be used for the CSI application and the opposite is also true [1], [10], [19]. Both VSIs and CSIs are vulnerable to EMI noise which compromises their reliability. Z-source inverters have proven to overcome most of the VSIs' and CSIs' drawbacks. This is the motive behind the focus of researchers on the Z-source inverters. Figure 2.3 shows a basic diagram of a ZSI which has a DC input (battery/fuel cell/PV array), a Z-impedance network (L_1, L_2 and C_1, C_2) and a three-phase universal bridge made of switching devices (S_1, S_2, S_3, S_4, S_5 and S_6).

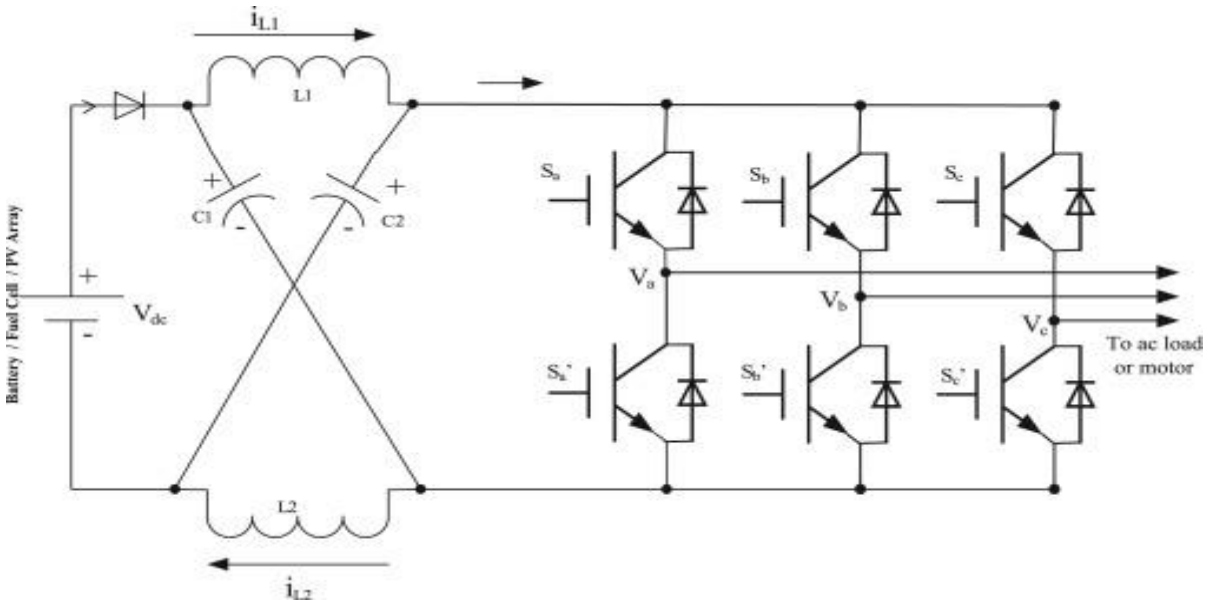


Figure 2.3: The basic ZSI circuit [6]

2.3. A classical three-phase Z-source inverter topology

2.3.1. A general overview

A z-source inverter is an improvement from the two above mentioned inverter topologies, viz. the VSI and CSI. As mentioned earlier, the ZSI overcome most of the conceptual and theoretical barriers and limitations that come with both the VSIs and CSIs. With a z-source inverter, an output ac voltage can theoretically be any value ranging from zero to infinity regardless of the input voltage [7], [9]. This implies that a z-source inverter is a buck-boost converter with a wide range of possible output voltages. Unlike traditional VSIs and CSIs which possess eight switching states or vectors, ZSIs have a ninth switching state called the shoot-through state which gives it the boosting capability. This shoot-through state is similar to the one mentioned earlier which is responsible for severe damage and unreliability in the case of VSIs. Therefore, a ZSI takes advantage of a VSI's weakness and makes it its strength instead.

Depending on the switching state, the operation of a ZSI can be classified into three modes of operation. The first mode occurs during one of the six active states. Active states occur when a DC-input voltage appears across the inductor and a capacitor (C_1 and L_2 or C_2 and L_1). During this mode, capacitors C_1 and C_2 are charged and stay charged at steady-state and energy flow to the load via the inductor. An inverter bridge can be seen as a current source when looking from the DC-link voltage [7], [9], [12].

The second mode occurs when a ZSI is operating in one of the two zero states. Zero states occur when the bridge short circuits the load either by all three upper or lower switching devices [3]. A

DC-input voltage appears across the inductor and a capacitor (C_1 and L_2 or C_2 and L_1) except that no current flow through them. A bridge can be taken as an open circuit in this mode [17], [19].

The third mode occurs when a ZSI is operating in one of the seven shoot-through states. Shoot-through can occur when any single-phase legs are shorted (3 possibilities; A or B or C), any two phase legs shorted (3 possibilities; AB or BC or AC) and when all three phases are shorted (1 possibility; ABC) [9], [17]. During this mode, a bridge can be seen as a short circuit when looking from the DC-link voltage and there is no voltage across the load. The capacitor voltage is boosted to the required value depending on the amount of shoot-through time (T_0). T_0 is inserted on portions of zero states or whole zero states (Depending on the PWM control technique used to give a ZSI the necessary boosting capabilities [3], [6], [7], [9]. Figures 2.4 and 2.5 show equivalent circuits of a ZSI when operating in non-shoot-through (mode 1 and mode 2) and shoot-through (mode 3) mode.

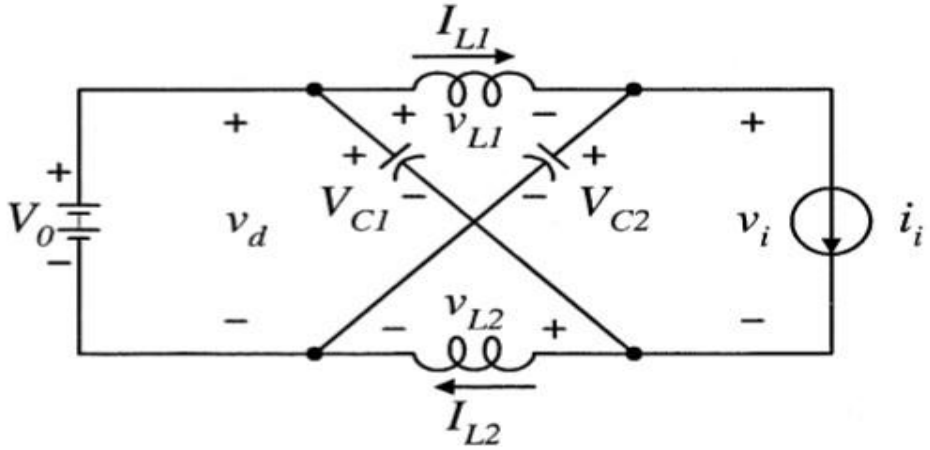


Figure 2.4: The ZSI in non-shoot-through state (mode 1 and 2) [3]

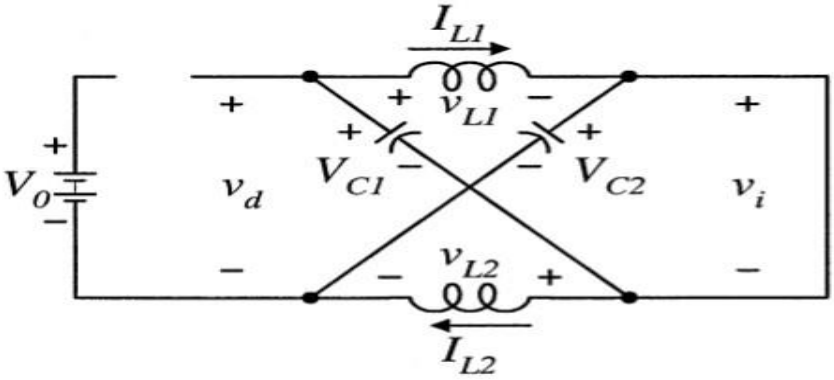


Figure 2.5: The ZSI in the shoot-through state (mode 3) [3]

When the ZSI is in the non-shoot-through state the inverter bridge is represented by a current source as seen from Figure 2.4. It is important to note the following; during any of the six active states, an inverter bridge is represented by a current source with finite current while during any of the two zero states, an inverter bridge is represented by a current source with zero current (open

circuit) [17]. When a ZSI is in shoot-through state the inverter bridge is represented by a short circuit as seen in Figure 2.5.

2.3.2. The circuit analysis

The analysis of a ZSI assumes that a z-impedance is symmetrical. That is; C_1 is equal to C_2 and L_1 is equal to L_2. This assumption results to (2.1) below:

$$V_{C1} = V_{C2} = V_C,\ V_{L1} = V_{L2} = V_L \tag{2.1}$$

During a shoot-through state (T_0 interval):

$$V_L = V_C\ ,\ V_{DC-link} = 0 \tag{2.2}$$

During a non-shoot-through state (T_1 interval):

$$V_L \neq V_C$$

$$V_L = V_{in} - V_C = V_C - V_{DC-link}$$

$$\therefore \widehat{V_{DC-link}} = V_C - V_L = 2V_C - V_{in} \tag{2.3}$$

It should be noted that V_{in} and $V_{DC\text{-}link}$ refer to V_0 and V_i respectively in figures 2.4 and 2.5. The average inductor voltage across inductors L_1 and L_2 is zero at steady state. This can be deduced from a definition of an inductor voltage which states that it is equal to a product of an inductor's characteristic inductance and a differential of current through it [3], [6], [7], [9], [12], [13]. [20]
Average inductor voltage-time product ($T = T_1 + T_0$ interval):

$$\overline{V_L} \times T = V_C \times T_0 + (V_{in} - V_C) \times T_1 = 0$$

$$\therefore \frac{V_C}{V_{in}} = \frac{T_1}{T_1 - T_0} \tag{2.4}$$

Average and peak DC-link voltage-time product ($T = T_1 + T_0$ interval):

$$\overline{V_{DC-link}} \times T = V_C \times T, \text{ at steady state} \tag{2.5}$$

$$\therefore \widehat{V_{DC-link}} = 2V_C - V_{in}$$

$$\widehat{V_{DC-link}} = \frac{T_1}{T_1 - T_0} \times V_{in} - V_{in} \quad (2.4 \text{ substituted in to } 2.3)$$

$$\widehat{V_{DC-link}} = \frac{2T_1 - T_1 + T_0}{T_1 - T_0} \times V_{in}$$

$$\therefore \frac{\widehat{V_{DC-link}}}{V_{in}} = \frac{T_1 + T_0}{T_1 - T_0}$$

$$\frac{\widehat{V_{DC-link}}}{V_{in}} = \frac{T_1 + T_0}{T_1 + T_0 - 2T_0} \quad (\text{substitute } T = T_1 + T_0)$$

$$\therefore \frac{\widehat{V_{DC-link}}}{V_{in}} = B = \frac{1}{1-2D_0}, D_0 \neq \frac{1}{2} \quad 2.6$$

2.4. The output filter design

Generally; harmonics in DC-AC converters can be removed by inserting an appropriate filter of high inductance [20], [21]. Inductive filters are easy to design but in the practical application of several kilowatts, inductive filters become expensive due to the large size of inductor and the dynamic response of the system becomes poor [20]. In the case of the ZSI application, the low pass filter is the one required to filter the high-frequency harmonics and pass-on low-frequency components. The most common low-pass filters are the LC and the LCL filters [22].

2.4.1. LC-filter

Figure 2.6 shows a typical circuit diagram of an LC-filter which has a series inductor (L) and a shunt capacitor(C) with V_{in} being the inverter side while V_{out} is the load side. It should be noted that for three-phase systems, figure 2.6 is considered as a per-phase equivalent representation of a three-phase LC filter.

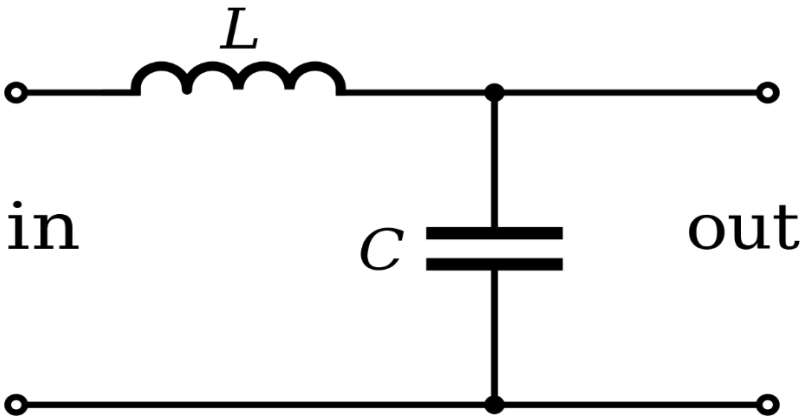


Figure 2.6: An LC filter [22]

LC-filters consist of a parallel capacitor and a series inductor. The addition of a parallel capacitor is an improvement from L-filter. This amendment of an L-filter to an LC-filter decreases a required inductance for the latter, thus reducing the overall cost and operational losses of LC-filter compared to L-filter. However, the use of a parallel capacitor comes with shortcomings such as high capacitance current and high inrush currents at fundamental frequency [20], [21].

2.4.2. LCL filter

Figure 2.7 shows a typical circuit diagram of an LCL-filter which has two series inductors (L_1 and L_2) and a shunt capacitor(C) with V_{in} being the inverter side while V_{out} is the load side and it

should be noted that for three-phase systems, figure 2.7 is considered as a per-phase equivalent representation of a three-phase LCL-filter.

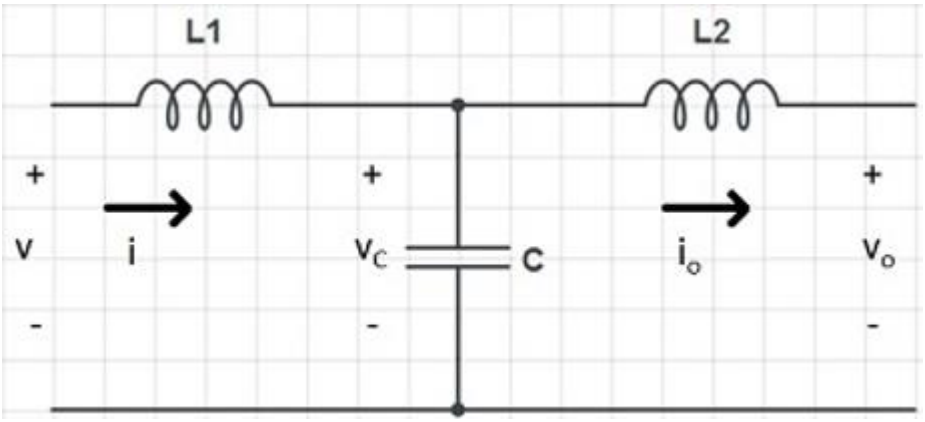


Figure 2.7: An LCL filter [20]

LCL filters overcome most of the issues related to L and LC-filters (first and second-order filters). LCL filters have notable merits over the second-order filters. Using LCL filters in a range of up to hundreds of kilovolt-amperes (kVA) provides excellent results however at relatively small values of inductor and capacitor hence reducing the filter overall costs. LCL filters give improved decoupling between grid and filter, as compare with first and second-order filters in case of grid-tie inverters. LCL-filters have a steep attenuation of -60dB/decade to switching frequency in bode as opposed to the first and second-order filters with -20dB/decade and -40dB/decade respectively [20], [22].

However, LCL filters oscillations may stay permanently and possibly damage the whole system due to a resonant condition. Around the resonant frequency, instability in current and voltage can be introduced due to resonance. To mitigate this effect, a damping resistor is added to an LCL-filter circuit [20]. By adding this damper, the damping and attenuation reduces [21]. 2.7 is a transfer function of the LCL filter and figure 2.7 and 2.8 show LCL filters with a series and parallel damping resistor incorporated, respectively. Series damping resistor results to a larger equivalent impedance of R and C as opposed to the parallel damping resistor. Therefore; high-frequency harmonics current flowing through C is bigger in series damped compared to a parallel damped filter. Hence; a series damped LCL-filter has a better effect on suppressing high-frequency harmonics [20], [21], [22].

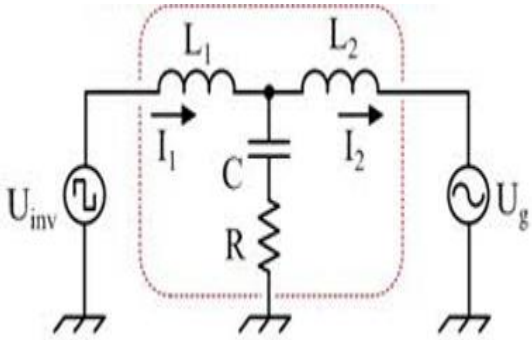


Figure 2.8: With series damping resistor [21]

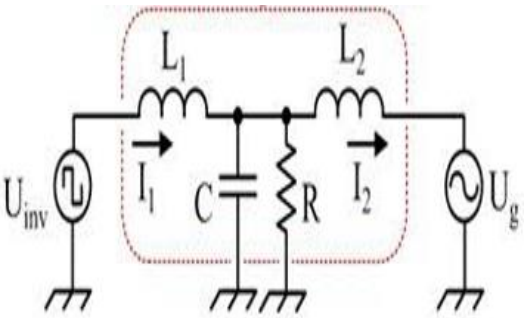


Figure 2.9: With parallel damping resistor [21]

The design of an LCL-filter can be achieved using 2.7 to 2.11. Z_B, C_B, V_φ and P are a base impedance, base capacitance, inverter output phase voltage as well as the inverter rated power respectively. The calculated values are the same for all three phases in a three-phase system [20], [21], [22].

$$Z_B = \frac{V_{(\varphi)}}{P} \tag{2.7}$$

$$C_B = \frac{1}{\omega Z_B} \tag{2.8}$$

$$C_1 = \frac{0.01}{0.05} \times C_B \tag{2.9}$$

$$L_1 = \frac{V_{IN}}{6 \times f_{SW} \times \Delta I_{max}} \quad where\ \Delta I_{max} = 0.1 I_{max} \tag{2.10}$$

$$L_2 = \frac{\sqrt{\frac{1}{{k_a}^2} - 1}}{C_1 \times {\omega^2}_{sw}} \quad (where\ k_a\ is\ an\ attenuation\ factor\ of\ 20\%) \tag{2.11}$$

2.5. The PWM control techniques

The PWM control technique, in the context of three-phase inverters, can be defined as a method of generating appropriate PWM signal for switching the switching devices of a universal bridge such that a desired AC waveform is obtained at the output terminals of a ZSI [1], [18], [23]. Since the ZSI was proposed in 2003, lots of work has been done in this subject, especially on PWM control methods [9]. Three most common PWM control strategies in literature are discussed in this paper; viz. a simple boost control (SBC), constant boost control (CBC) and maximum Boost Control (MBC) techniques [1], [3], [6], [7], [9], [12], [13] [18], [23].

2.5.1. Simple Boost Control

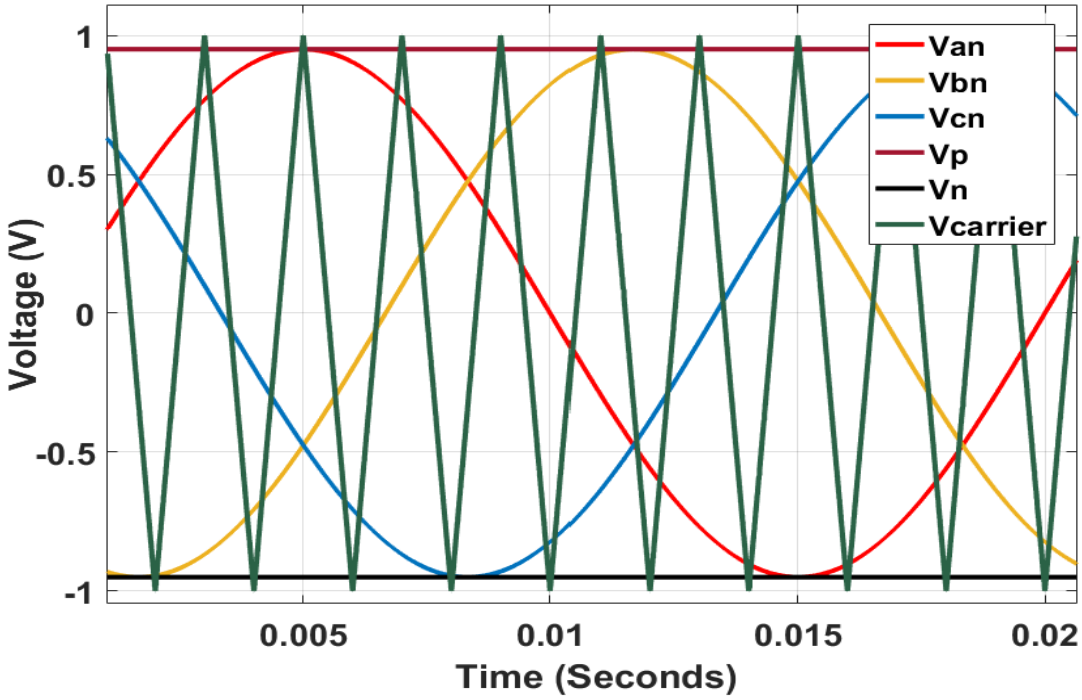


Figure 2.9: Simple boost control waveforms

Figure 2.10 shows a signal diagram of an SBC technique. A simple boost control uses two straight lines (V_p and V_n), a set of three-phase reference voltages (V_{an}, V_{bn} and V_{cn}) and the triangular carrier wave ($V_{carrier}$). A carrier wave is either equal to, greater than or less than the two straight lines (V_p and V_n). When a carrier wave is greater than V_p or less than V_n, a ZSI is operating in a shoot-through state (mode 3) else; it is operating at in either an active or zero state (mode 1 and mode 2).

When a triangular waveform is greater than an upper straight line or lower than a bottom straight line; a ZSI operates in a shoot-through state. Otherwise, a ZSI operates like a VSI and SBC technique operates like sine-PWM (SPWM) technique which is a traditional control technique used to control VSIs. This method is the simplest; however, the resulting voltage stress across the switching devices is relatively high because some traditional zero states are not utilized. Output voltage for SBC technique is given by 2.12 below [5], [10], [12], [18], [23]:

$$V_{ABC(\varphi)} = \sqrt{3}\, m_{SBC} B_{SBC} \frac{V_{in}}{2} \qquad 2.12$$

(where m_{SBC} and B_{SBC} are modulation index and boost factor for SBC technique respectively)

2.5.2. Constant Boost Control

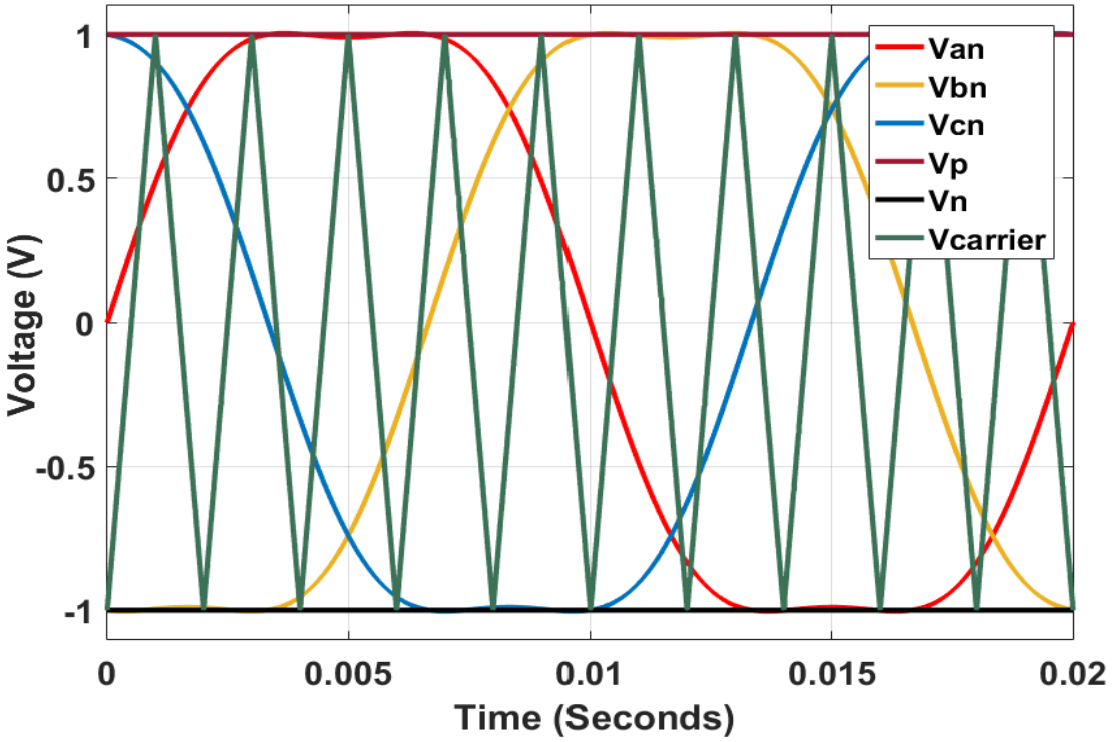


Figure 0.1: Constant boost control waveforms

Figure 2.11 shows a signal diagram of a CBC technique. A constant boost control also uses two straight lines (V_p and V_n), a set of three-phase reference voltages (V_{an}, V_{bn} and V_{cn}) injected with a third harmonic signal and the triangular carrier wave ($V_{carrier}$). A carrier wave is either equal to, greater than or less than the two straight lines (V_p and V_n). When a carrier wave is greater than V_p or less than V_n, a ZSI is operating in a shoot-through state (mode 3) else; it is operating at in either an active or zero state (mode 1 and mode 2) [10], [12], [18].

Constant boost control reduces the volume and cost of the design components, by keeping a shoot-through duty ratio constant. At the same time, a greater voltage boost for any given modulation index is desired and the reduced voltage stress across the switches is possible with Constant Boost Control. A constant boost control achieves the greater voltage gain (over SBC) while always keeping the shoot-through and hence duty ratio constant. Figure 15 shows the sketch map of the maximum constant boost control with third harmonic injection. Output voltage for CBC technique is given by 2.13 below [10], [12], [18]:

$$V_{ABC(\varphi)} = \sqrt{3}\, m_{CBC} B_{CBC} \frac{V_{in}}{2} \qquad 2.13$$

where m_{CBC} and B_{CBC} are modulation index and boost factor for CBC technique respectively.

2.5.3. Maximum Boost Control

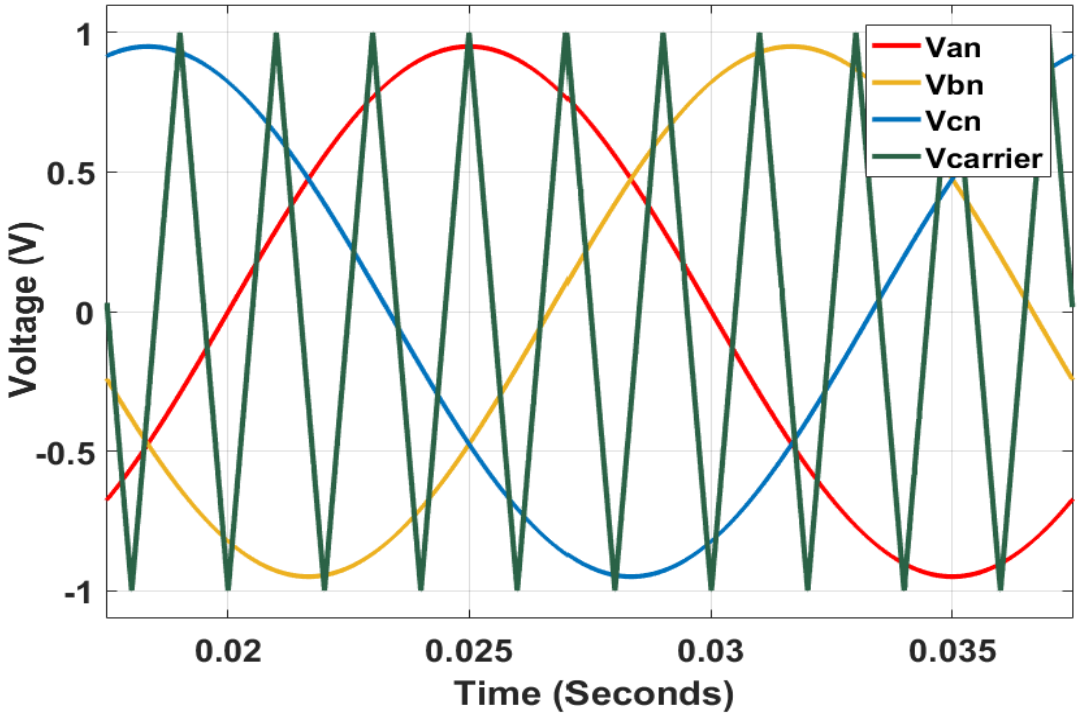


Figure 0.2: Maximum boost control waveforms

Figure 2.12 shows a signal diagram of a MBC technique. A maximum boost control uses two a set of three-phase reference voltages (V_{an}, V_{bn} and V_{cn}) and the triangular carrier wave ($V_{carrier}$) only. A carrier wave is either equal to, greater than or less than the peak value s (positive and negative peak) of a three-phase reference signals. When a carrier wave is greater than positive peaks or less than negative peaks of a three-phase reference signal, a ZSI is operating in a shoot-through state (mode 3) else; it is operating at in either an active or zero state (mode 1 and mode 2) [5], [10], [12], [18], [23].

This strategy achieves a reduction in the voltage stress across the switching devices under the desired voltage gain. This is very important for the efficient control of the ZSI. The maximum boost control does this by turns all traditional zero states into a shoot-through state [11]. It is implemented in a very similar manner to simple boost control except that the two constant enveloping lines are not included. The third harmonic injection can also be used to extend the modulation index range. Turning all zero states into shoot-through states can minimize the voltage stress. However, this method introduces a low-frequency current ripple that is associated with the output frequency in the inductor current and the capacitor voltage. This will cause a higher requirement of the passive components when the output frequency becomes very low. Therefore, the maximum boost control is suitable for applications that have a fixed or relatively high output frequency. Output voltage for CBC technique is given by 2.14 below [10], [12], [18]:

$$V_{ABC(\varphi)} = \sqrt{3}\, m_{MBC} B_{MBC} \frac{V_{in}}{2} \quad 2.14$$

(where m_{MBC} and B_{MBC} are modulation index and boost factor for CBC technique respectively)

2.6. Conclusion

This chapter compared three-phase ZSIs to three-phase VSIs and CSIs in terms of performance and reliability. The basic design principles of a three-phase ZSI, LCL-filter and PWM control techniques were then underlined. Their basic principles form the basis for the development of chapter 4. Chapter 3 discusses a methodological approach that was used to achieve the objectives of this research study.

3. METHODOLOGY

This chapter outline the methodological approach that was used in this research study to fulfil the aims and objectives discussed of the research study outlined in chapter 1. As discussed earlier in chapter 1, the purpose of this research study is to investigate the performance response of a Z-source inverter when different PWM control techniques are applied to it while varying the input variables and; use the gained knowledge from the aforementioned study to develop a different inverter topology with an improved performance relative to a classical Z-source inverter.

A systematic approach that was employed to achieve the above mentioned objective involved the following series of steps:

- Review of literature
- Design of a three-phase Z-source inverter and a PWM control techniques
- Selection of a software tool on which implement a ZSI and a CB-ZSI
- Collection and analysis of results of a ZSI
- Development of a performance criteria of a CB-ZSI
- Design of a three-phase CB-ZSI
- Collection and analysis of results of a CB-ZSI
- Conclusion

3.1. Literature review

Literature review focused on the background theory and design principles of Z-source inverters, three-phase filters and PWM control techniques. ZSIs were compared to traditional topologies of inverters (VSI and CSI), in terms of operational inherent reliability and the output power quality. Particular attention was paid to different applications currently in the industry and future directions of ZSIs thus, motivating a necessity of this dissertation.

The in-depth study of the operation of a classical three-phase Z-source inverter was done. This involved the equivalent circuit analysis of a Z-source inverter across its three possible operating states viz. the active, zero and shoot-through states. This analysis resulted in a primary equation of a boost factor (2.6) which holds across all three PWM techniques.

Three most common PWM control techniques in literature viz. simple boost, constant boost and maximum boost control technique; were studies [1], [3], [6], [7], [9], [12], [13] [18], [23]. Parameters such as a boost factor (B), gain factor (G), voltage stress across switching devices (V_{stress}) and percentage of total harmonics distortion (%THD) were compared across all three PWM techniques and the interdependent relationships between these parameters for the same PWM control technique were also studied.

Boolean algebra was also studied. The study focused on the formulation and interpretation of truth tables which is a tool that was used to span a complete switching behaviour of each of the three PWM techniques. The methods of formulating Boolean functions from a truth table were also investigated during a literature survey which was found to be divided into two methods viz. sum-of-product (SOP) and product-of-sum (POS) methods [24]. The methods optimizing Boolean functions formulated using SOP and/or POS methods were also part of a literature survey which incorporated the use of Boolean algebra identities and the use of karnaugh maps (k-maps) [24].

3.2. Design of a three-phase Z-source inverter circuit

The design of a ZSI circuit was as per the following specifications; input DC voltage ranging from 200 V to 500 V, switching frequency at 10.05 kHz and a total power rating of 2000 W. An input range of 200V-500V was selected for this research study in alignment to reference publications that were consulted in a literature survey whose input voltages in their studies fall in between this range, therefore; results of this research study can directly be compared to those of reference publications.

Furthermore, a range of 200-500V simulates a real situation of renewable energy sources that have low characteristic DC-output voltages such as photovoltaic cells or arrays [25]. A switching

frequency of 10.05 kHz was selected using (4.2) which states that a normalized frequency (m_f) should be an odd multiple of 3 to be able to use a single triangular carrier wave (f_Δ) across all three phases in PWM control techniques design. Furthermore; at normalized frequencies of more than 21, the output voltage of the ZSI is exclusively independent on the frequency and entirely dependent of m_f [6].

A power rating of 2000W is a relatively low power rating that was selected to cater for future consideration of possible implementing a practical prototype of a Z-source inverter (in chapter 4) and a Capacitor Boosted-Z-Source Inverter (in chapter 5). During implementation, a prototype of this power rating will be realizable without incurring excessive cost since low power rated components will be required. The circuit design of a ZSI had four main steps which are presented in a block diagram in figure 3.2.

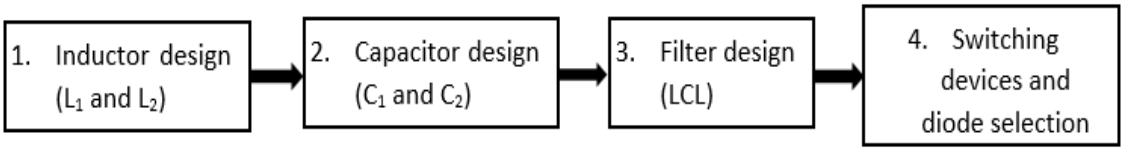


Figure 3.1: Z-source inverter design block diagram

The inductor design was achieved via (4.1) to (4.3), capacitor design was achieved via (4.4) and (4.5), LCL-filter design is covered in chapter 2 and was achieved via (2.7) to (2.11) and the selection of switching devices and a power diode was achieved via (4.6) to (4.8). All these equations used in a ZSI circuit design were discovered in a literature survey and at this point after the design process presented by figure 3.2, a circuit diagram shown in figure 2.3 (connected to 2kW load via a three-phase LCL-filter) was completely designed.

3.3. Design of PWM control techniques

During a literature survey, three main PWM control techniques appeared most frequently with others being often based on these main threes. Hence, this research study implements these PWM control techniques which are the simple boost control (SBC), constant boost control (CBC) and maximum boost control (MBC) pulse modulation width (PWM) techniques[1], [3], [6], [7], [9], [12], [13] [18], [23].

Figure 3.3 shows a general block diagram for a design of each of the three mentioned PWM control techniques.

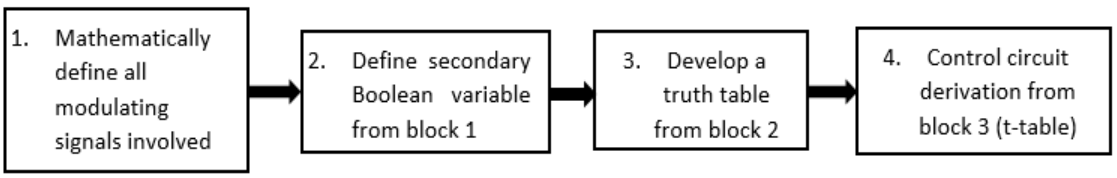


Figure 3.2: PWM control technique design block diagram

The first block of figure 3.3 involves mathematical definition of modulation signals for each of the three PWM control techniques. Those are a fundamental three-phase reference waveform ($V_{ac(3\varphi)}$) and a triangular carrier wave ($V_{carrier}$) for a maximum boost PWM technique [7], [9], [12], [13]; a fundamental three-phase reference waveform, a triangular carrier waveform and two constant voltages ($V_{constant}$) enveloping a fundamental reference waveform for simple boost PWM control technique [1], [3], [6], [12]; a third harmonic-injected fundamental three-phase reference waveform ($V_{ac(3\varphi,\ TH\text{-}Injected)}$), a triangular carrier waveform and two constant voltages enveloping a fundamental reference waveform for a constant boost PWM technique [10], [12], [18], [23].

The second block formulate secondary variable which are functions of aforementioned modulating signals for each PWM control technique. These secondary variables are of Boolean type; that is, they are either 0 or 1 when a value less than or greater than zero is assigned to them, respectively. The main purpose of these secondary variables is tell relationships between all the modulating signals at any given time across a period of fundamental reference signals $V_{ac(3\varphi)}$ or $V_{ac\ (3\varphi,\ TH\text{-}Injected)}$. That is, by looking at the states of secondary variable at any given instance; one can precisely tell the order of modulating signals ($V_{a(\varphi)}$, $V_{b(\varphi)}$, $V_{c(\varphi)}$, $V_{a(\varphi)\text{-}TH\text{-}Injected}$, $V_{b(\varphi)\text{-}TH\text{-}Injected}$, $V_{c(\varphi)\text{-}TH\text{-}Injected}$, $V_{carrier}$ and $V_{constant}$) from the highest to the lowest at any particular time point. Refer to an example below based on row 28 of table 4.9 in chapter 4 and figure 3.4 for a graphical interpretation of information presented by the secondary variables.

IJKLMN = 001000 mean:

- $V_{a(\varphi)}$ is less than $V_{b(\varphi)}$
- $V_{b(\varphi)}$ is less than $V_{c(\varphi)}$
- $V_{c(\varphi)}$ is greater than $V_{a(\varphi)}$
- $V_{a(\varphi)}$ is less than $V_{carrier}$
- $V_{b(\varphi)}$ is less than $V_{carrier}$
- $V_{c(\varphi)}$ is less than $V_{carrier}$

$$\therefore V_{a(\varphi)} < V_{b(\varphi)} < V_{c(\varphi)}\ and\ V_{carrier} > V_{c(\varphi)} > V_{b(\varphi)} > V_{a(\varphi)}$$

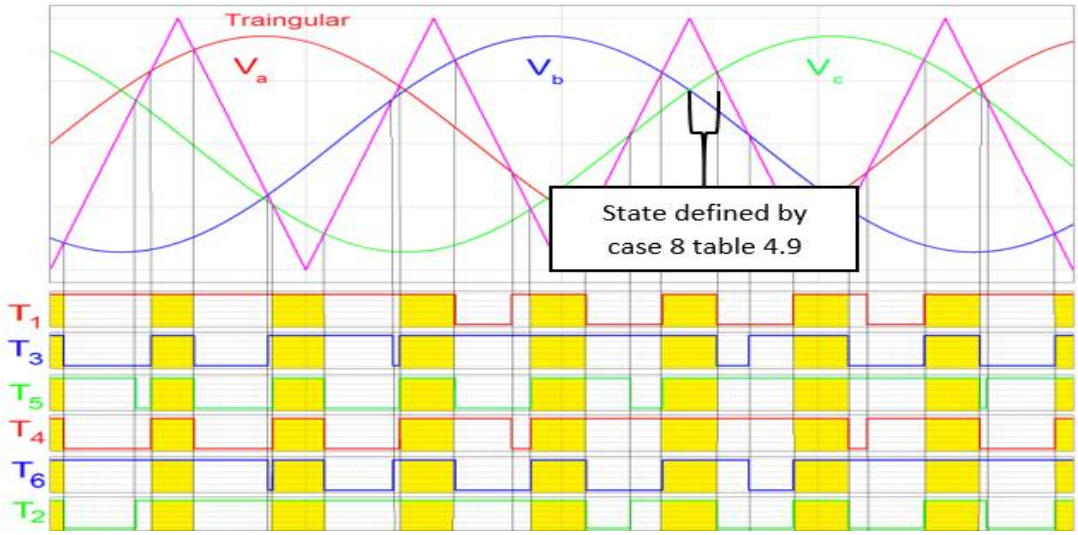


Figure 3.3: MBC modulating signals showing case 8 in table 4.9 [14]

Figure 3.4 shows state where secondary variables IJKLMN are having a Boolean value of 001000. This is a shoot-through state by definition and the switching devices of a highest phase signal, $V_{c(\varphi)}$, are gated-on simultaneously (for a duration for which IJKLMN = 001000 holds). As evident in figure 3.4, T_5 (which represents SSS_2 table 4.9) and T_2 (which represents SSS_5 table 4.9) are gated on for this duration. It should be noted that the states of secondary variable change many more times in one period (T) subject to frequency of a triangular carrier wave in a simulation or physical prototype, figure 3.4 shows a low frequency triangular carrier for explanatory purposes.

Therefore; secondary variables formulated across PWM control techniques (D, E, F, G, H for SBC and I, J, K, L, M, N for MBC PWM technique) pinpoint the active states (mode 1 of operation in chapter 2), zero states (mode 2 of operation in chapter 2) and shoot-through states (mode 3 of operation in chapter 2). This information is then used to create truth-tables that define switching behaviours of PWM control circuits for all possible states of secondary variables for each PWM technique. SOP method that was used to derive Boolean equations that describe switching behaviours of PWM control circuits. Kanaurgh maps (k-maps) were used to optimise Boolean equations for PWM control circuits before they were implemented on a simulation tool. Figure 3.4 shows a k-map for optimising MBC PWM technique Boolean functions SSS_1 – SSS_6.

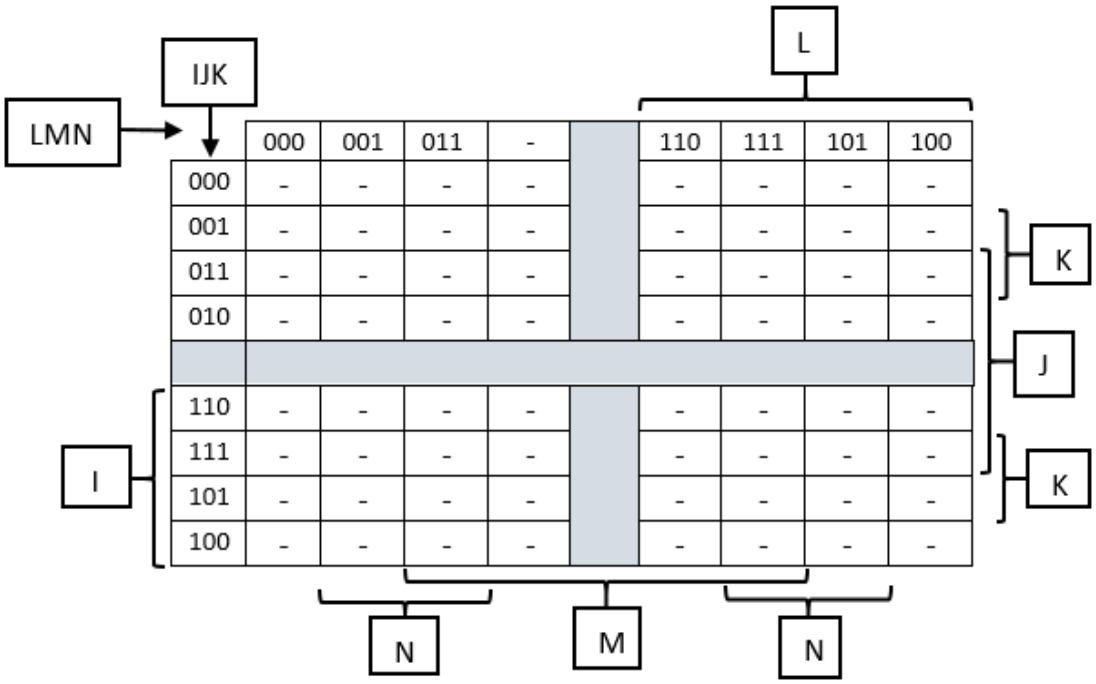


Figure 3.4: K-map for optimising Boolean equations SSS1 – SSS6

Figure 3.4 shows a k-map for a Boolean equation with 6 variables (I, J, K, L, M and N in the case of MBC PWM technique presented in this research study). Equations SSS_1 – SSS_6 had up to 24 terms in their raw form and were optimised to up to 8 terms thanks to the k-map optimisation method.

3.4. Selection of a simulation tool

After a paper design of a Z-source inverter and PWM control techniques was complete, it was crucial to select a suitable software tool in which to implement the designed ZSI and PWM control techniques.

Two software packages were under consideration, viz. power system computer aided design (PSCAD) and Matlab. The suitability of software was influenced by the ease of usability, analysis of percentage of harmonics distortion capability as well as the flexibility in displaying results such that the graphical results can be exported to editor window to edit them to improve the imagine quality of figures in the dissertation.

Both PSCAD and Matlab have capabilities of modelling a ZSI and the PWM control circuits and they both features a Fast-Fourier transform (FFT) based methods of analysing the percentage of total harmonics distortion [19]. However, PSCAD had the following limitations: It only supports plots in time domain and cannot plot harmonic magnitude or phase versus frequency and graphical results cannot be exported as picture files [19]. These limitations undermine the

collection of results for a purpose of reporting in dissertation while Matlab on the other hand; takes advantage of PSCAD's limitations and turns them into its strength with regards to appropriateness to this research study. Apart from the above stated facts, literature has shown bias towards Matlab over any other possible software in implementation of inverter related projects.

Hence, Matlab was a selected software package used to model all Z-source inverter and PWM control circuits for this research study.

3.5. Results of a ZSI and discussion

After a ZSI and PWM control techniques were successfully implemented in Matlab results were taken from the simulation. A sample table shown below was used to collect data from a simulated ZSI prototype for each of the three PWM control techniques.

Table 3.1 Sample table for collecting results

Varying input voltage and modulation index																	
1.	m	0.65	0.65	0.65	0.65	0.75	0.75	0.75	0.75	0.85	0.85	0.85	0.85	0.95	0.95	0.95	0.95
2.	V_{IN}	200	300	400	500	200	300	400	500	200	300	400	500	200	300	400	500
3.	V_{DClink}	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
4.	$V_{AC(3\varphi)}$	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
5.	Stress − ratio	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
6.	B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
7.	mB	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
8.	%THD	-	-	-	-	-	-	-	-	-	-	—	-	-	-	-	-

Table 3.1 above is a tool that was used to collect results in this research study. The second column of this table feature the two main input variables, viz. the input voltage and a modulation index as well as six key performance parameters of a ZSI, viz. the DC-link voltage, output AC-voltage amplitude, voltage stress ratio across the switching devices, boost factor, gain factor as well as the percentage of total harmonics distortion.

As stated earlier in section 3.2; an input range of 200V-500V was selected because most input voltages of the reference publications for this research study fall in between this range therefore; results of this research study can directly be compared to those of reference publications. A modulation index range of 0.65 – 0.95 was carefully selected such that all PWM control technique are defined in this range. SBC, CBC and MBC PWM control techniques have different operating

ranges of a modulation index and therefore, a common range for all three PWM control techniques had to be selected. Furthermore, the range of 0.65 - 0.95 if far away from the asymptotes defined by (4.24), (4.26) and (4.39) of SBC, CBC and MBC PWM control techniques respectively and hence all three PWM control techniques are at stable operating state in modulation index in this range.

Therefore, the collection of data included the population of table 3.1 for each PWM control technique and graphical results were displayed for one case in a table. This case was chosen to be column 3; the third column where the input voltage is 200V at a modulation index of 0.65.

The analysis of results involved graphically presenting the relationships and trends discovered after populating table 3.1 for all three PWM control techniques. The relationships presented were; output voltage amplitude vs input DC-voltage (at a constant modulation index of 0.65), output voltage amplitude vs modulation index (at a constant input voltage of 200V), DC-link voltage vs input DC-voltage (at a constant modulation index of 0.65), DC-link voltage vs modulation index (at a constant input voltage of 200V), voltage stress across switching devices vs modulation index and the percentage of total harmonics distortion vs modulation index.

Relationships between these key performance parameters were recognised and classified as linear of nonlinear, increasing or decreasing relationships and the rate of change (gradient) was also noted. To confirm validity of a simulation of a ZSI and a PWM control technique (for all three PWM control techniques), a random column was chosen from table 3.1 for which theoretical and practical key performance parameters were compared. This is achieved in table 4.6, 4.8 and 4.11 in chapter 4.

3.6. Development of a CB-Z-Source Inverter performance criteria

A Capacitor Boosted-Z-Source Inverter was simply going to be given merits based on showing improved readings on the key performance parameters as compared to those of a Z-source inverter for the same input conditions. That is; a larger DC-link voltage and hence the boost factor, a larger gain factor and hence the amplitude of an AC output voltage, a smaller voltage stress across the switching devices and less percentage of total harmonic distortion; in a CB-ZSI than in a ZSI when all three different PWM control techniques are applied at similar input conditions.

3.7. Design of a CB-Z-Source Inverter

A similar approach that was employed in ZSI circuit analysis was also used in CB-ZSI circuit analysis. In a classical ZSI, inductor voltages (V_{L1} and V_{L2}) are zero at steady state [1], [3], [6],

[7], [9], [12], [13] [18], and therefore; a hypothesis was made that adding a shunt capacitance across inductors of a ZSI transforming it to a CB-ZSI will maintain a residual voltage at steady state and hence inductor voltages are no longer zero at steady state for a CB-ZSI.

This implied that a much larger DC-link voltage can be maintained at larger modulation indexes and/or smaller input voltages. A DC-link voltage is directly proportional boost factor, therefore a boost factor and hence a gain factor also increase in a CB-ZSI compared to a ZSI for the same modulation index [9], [12], [13]. This suggests a reduced voltage stress across the switching devices because a CB-ZSI can operate at larger modulation indexes but still possess a lager boost factor and hence the gain factor. Less stress on the switching devices imply less switching losses and that switches operation in their linear region hence less total harmonic distortion due to switching devices [8].

Therefore, a shunt capacitance C_p was added and the shoot-through and non-shoot equivalent circuits of a CB-ZSI were analysed thus resulting into a different boost factor equation (5.12).

3.8. Results of a CB-Z-Source Inverter and discussion

A similar approach that was employed in a ZSI to display results was also applied to a CB-ZSI. This was ensured for simplified comparison between the two topologies. A similar tool (table 3.1) was used and shunt capacitance was chosen to be 1% and 2% of the original impedance capacitances (C_1 and C_2). Discussion of results in this section discussed the effect of varying capacitance of shunt capacitors C_p's and pointed out relationships that existed between key performance parameters.

3.9. Conclusion

This section stated whether the objectives of the whole research study were fulfilled. The judgement was done based on the criteria developed in section 3.6 and the overall course of the study. The future directions for future development of work contained in this research study were highlighted.

4. SIMULATION AND RESULTS OF DIFFERENT PWM CONTROL TECHNIQUES

This chapter aims to implement the discussion developed in chapter 2. The z-source inverter (ZSI) circuit is designed after which different PWM control techniques are formulated and applied to it. The results for each PWM control scheme are then presented and discussed in detail. The critical performance parameters analysed include DC-link voltage ($V_{DC\text{-}link}$), boost factor (B), modulation index (m), voltage stress (V_{stress}), voltage gain (G) as well as the percentage of total harmonic distortion (%THD).

The design of a ZSI circuit is as per the following specifications; input DC voltage ranging from 200 V to 500 V, switching frequency at 10.05 kHz and a total power rating of 2000 W. A PWM control technique of merit would be the one having a wider operation range for the critical performance parameters without compromising the quality of output power. That is; a wider boost factor, modulation index and output voltage operating range without incurring excessive voltage stress on the switching devices and rendering fundamental frequency as well as the total harmonic distortion and phase sequence out of specification [5].

4.1. Basic ZSI design

The design of a ZSI circuit is broadly divided into four sections, viz. capacitor design, inductor design, filter design as well as the power diode design and the selection of power electronic switching devices. In the following subsections, the four sections of ZSI design are presented and the designed values give the lower limit that designed components can be, however; in a practical application where components have standard values, it is often impossible to get the exact component rating that comes out in the design calculations. An example of this case is resistor series, E3, E6, E12, etc. The chosen values should be above and close as possible to the designed value [19].

4.1.1. Inductor design

The inductor design is a process of calculating a minimum inductance requirement for a Z-impedance network viz. L_{1min} and L_{2min}. To archive the minimum inductance design; the average inductor current $\bar{I}$, the current ripple ΔI and a DC-link voltage $V_{DC\text{-}link}$ should be calculated first. (4.1) and hence (4.2) below are used to archive a ripple current [9], [12], [18].

$$\bar{I} = \frac{P}{V_{IN}} \tag{4.1}$$

After working out $\bar{I}$ the ripple current ΔI can be calculated by working out the maximum and minimum current. The maximum peak-to-peak current can be calculated via (4.2) [9], [12] as follows:

$$I_{MAX} = \overleftrightarrow{I} + 30\% \ and$$

$$I_{MIN} = \overleftrightarrow{I} - 30\%$$

$$\therefore \ \Delta I = I_{MAX} - I_{MIN} \quad 4.2$$

In design, it is of paramount importance to cater for the worst-case scenario; this improves the stability and reliability of the design [18]. For this reason, a boost factor B of 5 is chosen as the upper limit. Theoretically; as long as the ZSI operates at boost factor range of 1 to 5, all calculated element, viz. the capacitor, an inductor and the switching devices will successfully withstand the stresses subjected to them. A shoot-through time T_0 can now be calculated using (4.3) and hence the minimum inductance requirement L_{min} uses (4.4) [3], [6], [7], [9], [12], [13], [20]:

$$\frac{1}{1 - 2(T_0/T)} = \leq B \quad 4.3$$

$$L_{min} = \frac{V_{DC\_link}(\max) \times T_0}{\Delta I} \ where \ V_{DC\_link}(\max) = B \times V_{in} \quad 4.4$$

4.1.2. Capacitor design

The capacitor design is a process of calculating a minimum capacitance requirement for a Z-impedance network viz. C_{1min} and C_{2min}. To archive minimum capacitance design; an average inductor current (already calculated via 4.1), shoot-through time (already calculated via 4.3) and capacitor ripple voltage ΔV_c are required first. Voltage ripple is calculated via (4.5) and hence the minimum capacitance requirement via (4.6) [3], [6], [7], [9], [12], [13], [20].

$$\Delta V_C = V_{DClink} \times 3\% \quad 4.5$$

$$\therefore C_{min} = \frac{\overleftrightarrow{I} \times T_0}{\Delta V_C} \quad 4.6$$

4.1.3. Filter design

LCL-filters are the most preferred choice over LC and L-filters. The reason behind this choice is the weight, size and cost of LCL-filters over LC and L-filters. LCL filters produce excellent results in the range of a hundred kilovolt-amperes but yet the values of inductors and capacitors are small relative to the values that would have been required for LC and L-filters. LCL-filters

give superb attenuation of -60 Db/decade to switching frequency compared to LC and L-filters [14], [20], [21], [22]. The LCL filter design can be done using (2.7) to (2.12).

$$C_B = \frac{1}{\omega Z_B}$$

$$where\ Z_B = \frac{V_{(\varphi)}}{P}$$

$$\therefore C_1 = \frac{0.01}{0.05} \times C_B$$

$$L_1 = \frac{V_{IN}}{6 \times f_{SW} \times \Delta I_{MAX}}$$

Where $\Delta I_{MAX} = 0.1 I_{MAX}$

$$\therefore L_2 = \frac{\sqrt{\frac{1}{{k_a}^2} - 1}}{C_1 \times {\omega^2}_{sw}}$$

(where k_a is the attenuation factor which is 20%)

4.1.4. Selection of switching devices and a diode

The maximum voltage across the diode as well as the power electronic switches equal to the peak DC-link, and the inductor current has been calculated in the inductor design; therefore, maximum line-to-line voltage and load current are calculated via (4.7) and (4.8) below. Hence the maximum current through the switches occurs at maximum power transfer and can be calculated via (4.9) [3], [6], [9] , [13].

$$V_{L-L(max)} = V_{(\varphi)} \times \sqrt{2} \quad 4.7$$

$$I_{LOAD} \frac{P}{\sqrt{3} \times \cos \emptyset \times V_{L-L(max)}} \quad (@\ unity\ power\ factor) \quad 4.8$$

$$\therefore \quad I_{switch\,(max)} = \frac{1}{2} \times I_{LOAD} + \frac{2}{3} \times I_L \quad 4.9$$

The switching devices and a diode to be selected generally have current and voltage ratings exceeding the above calculated values by at-least 25% as a safe working margin [9]. Figure 4.1 below shows the basic flow diagram of the z-source inverter. Figure 4.1 shows five main blocks of a ZSI which are a DC-power supply, a Z-impedance network, a three-phase H-bridge, a three-phase filter and a set of three-phase terminals on which a three-phase load is connected.

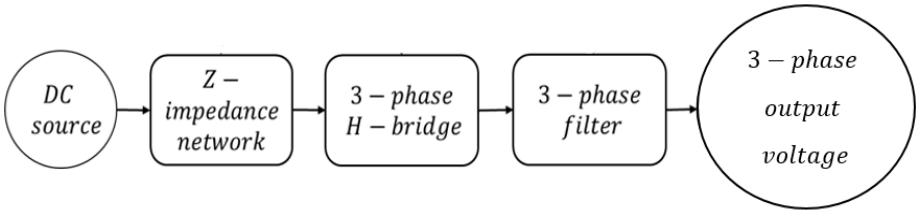


Figure 4.1: Basic ZSI block diagram

4.2. PWM control schemes

The upcoming subsections detail designs of different PWM control scheme and investigation of critical performance parameters for each PWM control schemes. The results are then tabulated after-which they are discussed. The discussion mainly points out the relationships that exist between these critical performance parameters and supports them with theoretical equations developed in a literature review in chapter 2.

4.2.1. Sine pulse width modulation (SPWM)

4.2.1.1. Design of sine pulse width modulation (SPWM) control circuit and presentation of results

SPWM control technique is a traditional PWM used to control VSIs and CSIs and does not boost voltage (no shoot-through time); therefore, it is only featured in this dissertation to serve as a reference for other PWM techniques (SBC, CBC and MBC) concerning performance. (4.10) is a three-phase fundamental frequency voltage waveform and is generally the main goal for all 3-phase DC-AC converters and thus a three-phase ZSI. Depending on the application, V_m and/or ω may/may not vary e.g. ω varies in variable speed drives (VSDs), however; phase difference between phase waveforms remain the same [9], [17].

$$V_{AC(3\varphi)} = \begin{cases} V_{A(\varphi)} \\ V_{B(\varphi)} \\ V_{C(\varphi)} \end{cases} = \begin{cases} V_m \sin(\omega t) \\ V_m \sin(\omega t - 120°) \\ V_m \sin(\omega t - 240°) \end{cases} \quad 4.10$$

The normalized frequency m_f should be an odd multiple of 3 to be able to use a single triangular carrier wave f_Δ across all three phases. At normalized frequencies, m_f of more than 21, the output voltage of the ZSI is exclusively independent on the frequency and entirely dependent on m_f [6]. Therefore; the output voltage of the ZSI when a sine PWM control technique is used is given by (4.11) [3], [6], [9], [12], [13].

$$V_{ABC(\varphi)} = \sqrt{3}\, m_{SPWM} \frac{V_{IN}}{2} \; ; \quad 0 < m < 1 \; where \; m_f = \frac{f_\Delta}{f} \quad 4.11$$

The sine PWM control technique is based on a comparison between a fundamental and a triangular carrier wave. For upper switching devices (S_1, S_3, S_5) the control PWM signal is high

(1) whenever a triangular carrier wave $V_{carrier}$ is greater than a fundamental wave $V_{ac(3\varphi)}$ and is low (0) whenever the triangular carrier wave is lower than the fundamental wave. For lower switching devices (S_2, S_4, S_6) the control PWM signal is high whenever a triangular carrier wave $V_{carrier}$ is lower than a fundamental wave and is low whenever the triangular carrier wave is greater than the fundamental wave [2].

Defined below are three variables A, B and C that are all functions of time. When these functions are taken through a Boolean operator, they can tell which one is greater between $V_{a(\varphi)}$, $V_{b(\varphi)}$ and $V_{c(\varphi)}$ against $V_{carrier}$ respectively.

$$A = V_{A(\varphi)} - V_{(carrier)} \quad 4.12$$

$$B = V_{B(\varphi)} - V_{(carrier)} \quad 4.13$$

$$C = V_{C(\varphi)} - V_{(carrier)} \quad 4.14$$

The desired switching pattern of the PWM generator controlling a ZSI can completely be defined using the above formulated secondary variables (A, B and C) in conjunction with switching states ($S_1 – S_6$). Therefore, the table below is a truth table showing states of each switching device at all secondary variable state possibilities, thus defining a complete switching behaviour of the PWM controller required to give out the required three-phase signal (4.1).

Table 4.1: Truth table for the traditional ZSI mode PWM controller

Phase leg A		
A	S_1	S_4
0	0	1
1	1	0
Phase leg B		
B	S_2	S_5
0	0	1
1	1	0
Phase leg C		
B	S_2	S_5
0	0	1
1	1	0

Six Boolean equations defining a switching behaviour of six switching devices across three phase legs of a three-phase ZSI can be derived from the above truth table. Sum of Product (SOP) is the method used to derive the equations which, when put together, results in the SPWM control PWM generator flow diagram in figure 4.2. Below is the list of equations:

$$S_1 = A\ (upper\ switch) \quad 4.15$$

$$S_4 = \bar{A}\ (lower\ switch) \quad 4.16$$

$$S_2 = B\ (upper\ switch) \quad 4.17$$

$$S_5 = \bar{B}\ (upper\ switch) \quad 4.18$$

$$S_3 = C\ (upper\ switch) \quad 4.19$$

$$S_6 = \bar{C}\ (lower\ switch) \quad 4.20$$

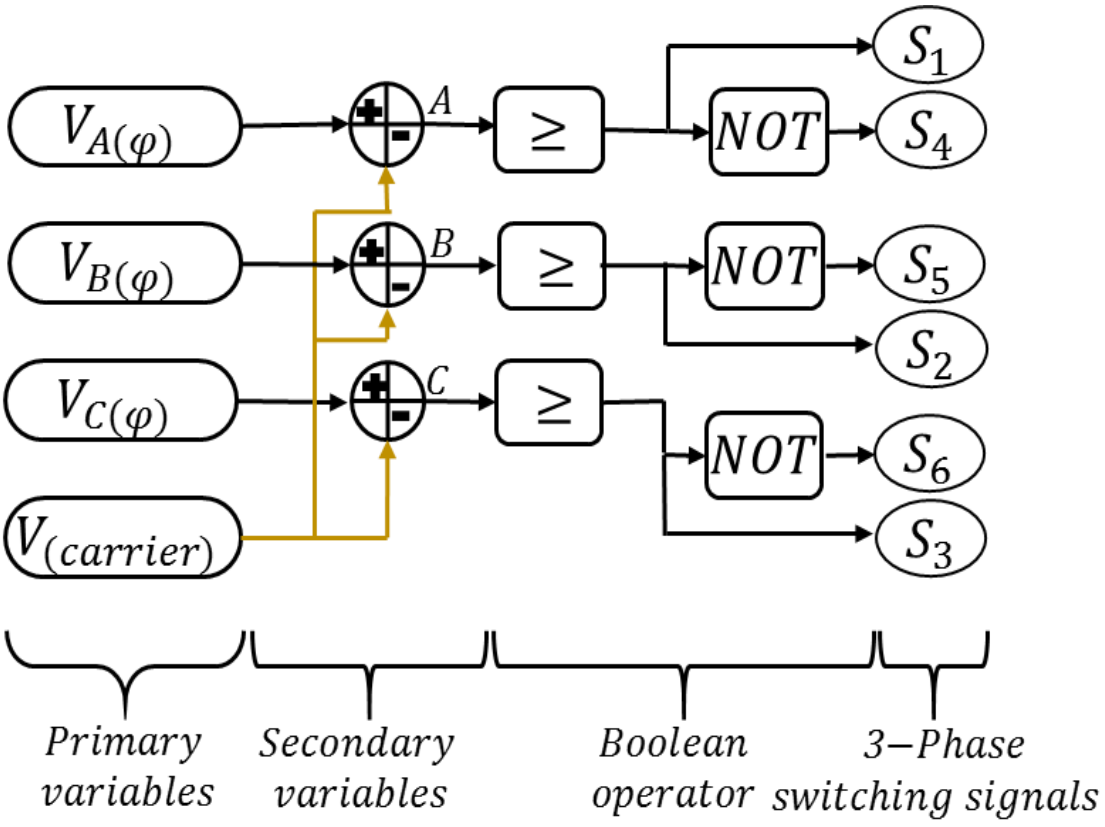


Figure 4.2: SPWM technique PWM generator

In figure 4.2 switching devices S_1 and S_4 make up phase leg A whose switching behaviour is defined by (4.15) and (4.16) respectively; S_2 and S_5 make up phase leg B whose switching behaviour is defined by (4.17) and (4.18) respectively while S_3 and S_6 make up phase leg C whose switching behaviour is defined by (4.19) and (4.20) respectively. From this point onwards, the results will be presented as per the following colour coding: Phase A – red, phase B – yellow and phase C – blue; as per South African wiring colour coding [5].

To analyse relationships between critical performance parameters, sample results are recorded at different input voltages V_{in} viz. 200V, 300V, 400V and 500V. For each input voltage point, the

modulation index m is varied as follows; 0.65, 0.75, 0.85 and 0.95. The following list of figures are results sampled for V_{in} of 200V and m at 0.65, the rest of the results are presented in table 4.2.

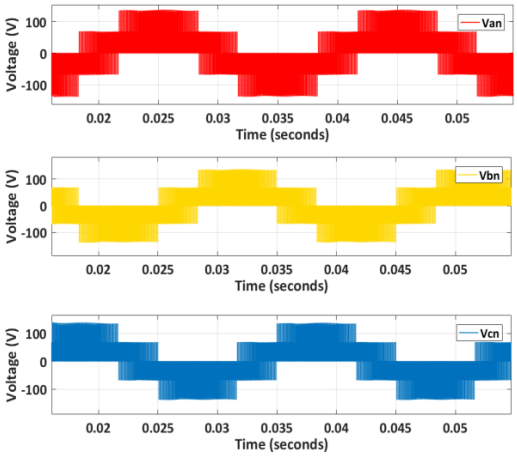


Figure 4.3: Unfiltered phase voltages (SPWM)

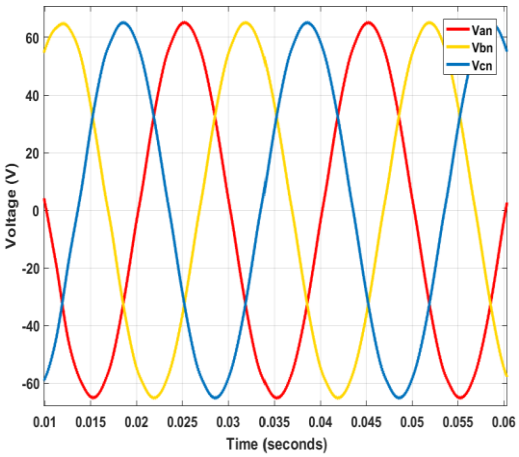


Figure 4.4: Filtered phase voltage (SPWM)

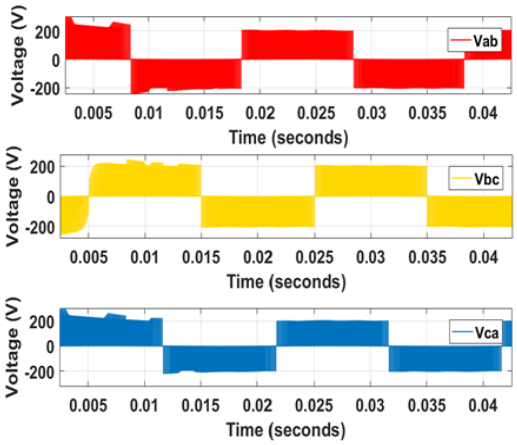


Figure 4.5: Unfiltered line voltages (SPWM)

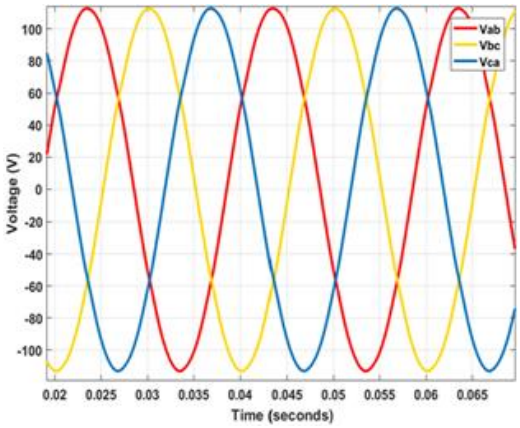


Figure 4.6: Filtered line voltage (SPWM)

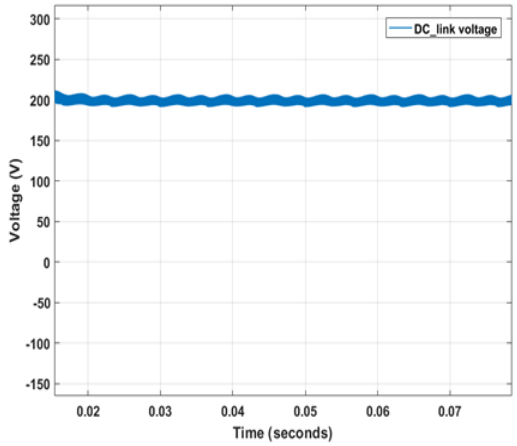


Figure 4.7: DC-link voltage (SPWM)

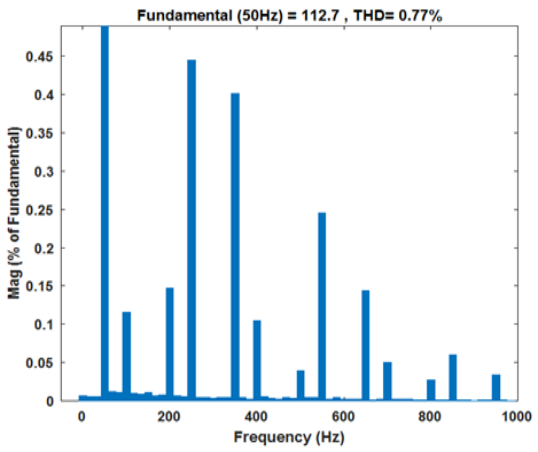


Figure 4.8: %THD (SPWM)

Figure 4.3 and 4.4 show unfiltered and filtered phase voltages, figure 4.5 and 4.6 show unfiltered and filtered line voltages, figure 4.7 show a DC-link voltage while figure 4.8 shows the percentage of total harmonic distortion of a line voltage. All this set of results was sampled at V_{in} of 200 and a modulation index of 0.65. Figure 4.3 to 4.8 confirm the expected results as per (4.11). The amplitude of phase and line waveforms, as well as a DC-link voltage conform to (4.11) and the %THD is below 5% which is the South African national grid specification for percentage of total harmonics distortion as stipulated by SANS 10142 standard documents [5].

Table 4.2: Summary of VSI mode results

Varying input voltage and modulation index as per (4.11)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	203.4	305.5	407.5	509.6	199.3	299.4	399.4	499.5
4	$V_{AC(3\varphi)}$	112.6	169.0	225.2	281.5	130.1	194.9	260.0	325.0
5	$Stress-ratio$	0.554	0.553	0.553	0.553	0.651	0.651	0.651	0.651
6	%THD	0.760	0.770	0.770	0.770	0.280	0.280	0.280	0.280
Table 4.2 continued below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	199.3	299.3	399.3	499.4	199.2	299.3	399.3	499.3
4	$V_{AC(3\varphi)}$	147.1	220.8	294.5	368.0	164.4	246.8	329.1	411.5
5	$Stress-ratio$	0.738	0.738	0.738	0.737	0.825	0.825	0.824	0.824
6	%THD	0.240	0.240	0.240	0.240	0.200	0.210	0.200	0.200

4.2.1.2. Analysis of results

A couple of trends and relationships can be highlighted in table 4.2. The voltage stress on the switching devices is exclusively dependent on the modulation index; it remains the same despite the changes in the input voltage but decreases with an increase in modulation index as evident in table 4.2. For a constant voltage, the DC-link voltage and hence the voltage stress decreases with

an increase in modulation index. The percentage of total harmonic distortion is exclusively dependent on the modulation index and decreases with an increase in the modulation index. For a constant input voltage, the output voltage increases with an increase in the modulation index. Refer to the following graphs for the above-mentioned relationships.

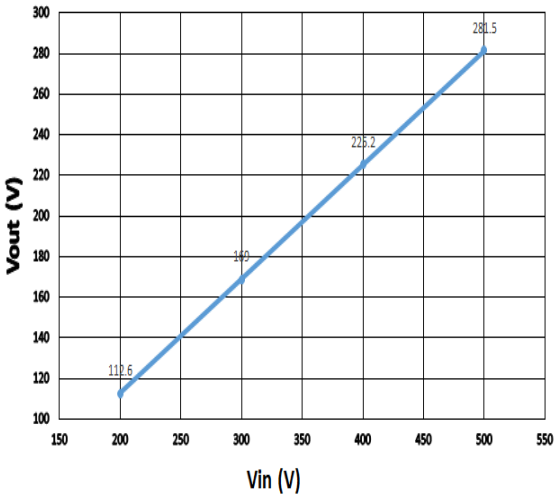


Figure 4.9: V_{in} vs V_{out} for SPWM (m = 0.65)

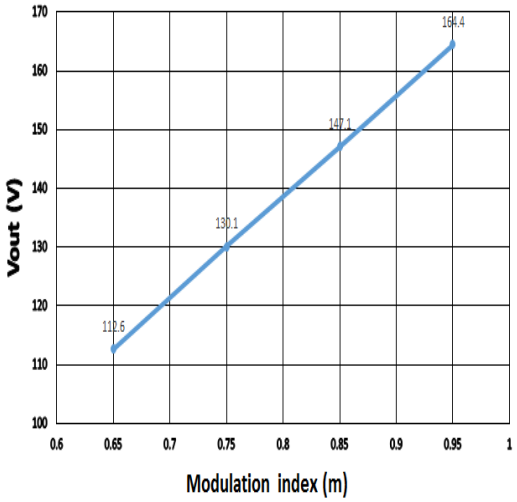


Figure 4.10: m vs V_{out} for SPWM (Vin = 200V)

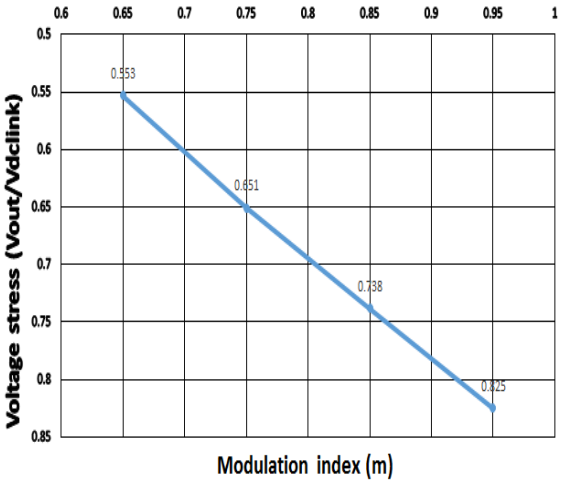


Figure 4.11: ($V_{out}/V_{dc\text{-}link}$) vs m for SPWM

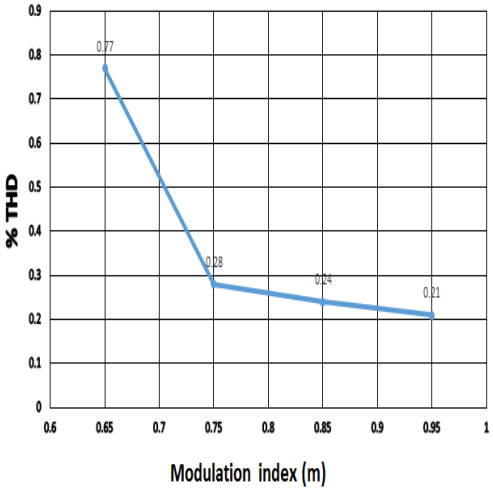


Figure 4.12: %THD vs m for SPWM

Figure 4.9 together rows 2 and 4 of table 4.2 shows that V_{out} increases with an increase in V_{in} to according to (4.11). (4.11) states that the input voltage and the output voltage are linearly related to the proportional factor being $\frac{\sqrt{3}}{2} *$m (where m is 0.65 for figure 4.9). Therefore; the gradient of the graph of figure 4.9 is expected to be $\frac{\sqrt{3}}{2} *0.65$. Refer to the calculation below:

$$V_{ABC(\varphi)} = k_1 V_{in} \quad (4.21)$$

$$k_1 = \frac{V_{ABC(m=0.95)} - V_{ABC(m=0.65)}}{V_{in(m=0.95)} - V_{in(m=0.65)}} \quad (4.22)$$

Figure 4.10 together with row 1 and 4 of table 4.2 also shows that V_{out} increases with an increase in m according to (4.11). In this case, an input voltage is kept constant while the modulation index is varied, hence the linear relationship, in this case, is between the output voltage and the modulation index with the proportional factor being $\frac{\sqrt{3}V_{IN}}{2}$ where V_{in} is 200V in the case of figure 4.10. Refer to the calculation below:

$$V_{ABC(\varphi)} = k_2 m \quad (4.23)$$

$$k_2 = \frac{V_{ABC(m=0.95)} - V_{ABC(m=0.65)}}{m_{(m=0.95)} - m_{(m=0.65)}} \quad (4.24)$$

Figure 4.11 together with row 3 and 4 show that the voltage stress across the switching devices is decreasing with increase in modulation index, a lower ratio of output voltage to DC-link voltage implies a high voltage stress (larger voltage difference) while a higher ratio implies a lower voltage stress (smaller voltage difference) for SPWM control (because a gain factor is less than 1, the opposite is true for other boost based PWM control techniques). This is the case because a duty cycle of a switching signal decreases with the increase in the modulation index. Therefore; DC-link voltage is higher for lower modulation indexes [9].

Figure 4.12 together with row 1 and 6 shows that the % total harmonics distortion is exclusively dependent on the modulation index. It does not change with variation in the input voltage, however, it decreases with an increase in the modulation index. This is because stress across switching devices is lowered at high modulation indexes and due to smaller duty ratios; there are also much lower switching losses during the inverter operation [19]. Table 4.3 summarises the analysis of the results presented in figures 4.9 and 4.10.

Table 4.3: Summary of figure 4.7 and 4.8 results

k_1 (theoretical)	k_1 (actual)	k_2 (theoretical)	k_2 (theoretical)
$\frac{\sqrt{3}}{2}\times 0.65=0.56$	0.56	$\frac{\sqrt{3}}{2}\times 200=173.0$	172.7

4.2.2. Simple boost pulse width modulation technique (SBC)

4.2.2.1. Design of simple boost pulse width modulation control circuit and presentation of results

On top of the two modulating signals for SPWM control technique $V_{ac(3\varphi)}$ and $V_{carrier}$ that were defined in subsection 4.2.1; a simple boost PWM technique adds two more straight lines that envelope the fundamental three-phase signal on both the positive and negative peak (refer to chapter 2) defined mathematically as follows [3], [6], [9], [12]:

$$V_{constant} = \begin{cases} C \\ -C \end{cases} \text{ where } V_M \leq C \leq 1 \text{ and } -1 \leq -C \leq -V_M \quad 4.25$$

The desired switching behaviour of the simple boost PWM generator controlling clocking the ZSI's switching devices can completely be defined using five secondary variables formulated from the three modulating signals viz. $V_{ac(3\varphi)}$, $V_{carrier}$ and $V_{constant}$. Therefore, let:

$$D = V_{A(\varphi)} - V_{(carrier)} \quad 4.26$$

$$E = V_{B(\varphi)} - V_{(carrier)} \quad 4.27$$

$$F = V_{C(\varphi)} - V_{(carrier)} \quad 4.28$$

$$G = C - V_{(carrier)} \quad 4.29$$

$$H = V_{(carrier)} - (-C) \quad 4.30$$

The desired switching pattern of the SBC PWM generator controlling the ZSI can completely be defined using the above formulated secondary variables viz. D, E, F, G and H together with the switching states SS_1 – SS_6 of switching devices. Therefore; table 4.4 below is a truth table showing states of each switching device at all secondary variable state possibilities, thus defining a complete behaviour of the SBC PWM controller required to give out the required three-phase signal (4.1).

Table 4.4: Truth table for the simple boost PWM controller

+VE Peak shoot-through			-VE Peak shoot-through		
Phase leg A					
D	G	SS_1	$\overline{D}$	H	SS_4
0	**0**	**1**	**0**	**0**	**1**
0	1	0	0	1	0
1	0	impossible	1	0	impossible
1	1	1	1	1	1
Phase leg B					
E	G	SS_2	$\overline{E}$	H	SS_5
0	**0**	**1**	**0**	**0**	**1**
0	1	0	0	1	0
1	0	impossible	1	0	impossible
1	1	1	1	1	1
Phase leg C					
F	G	SS_3	$\overline{F}$	H	SS_6
0	**0**	**1**	**0**	**0**	**1**
0	1	0	0	1	0
1	0	impossible	1	0	impossible
1	1	1	1	1	1

Table 4.4 translates directly to a PWM controller that implements a simple boost PWM control technique. The highlighted states with bold font are the shoot-through state. 'Impossible' states consider mathematically impossible cases e.g. where $V_{carrier}$ is greater than $V_{constant}$ but less than $V_{a(\varphi)}$, $V_{b(\varphi)}$ or $V_{c(\varphi)}$, which are states that cannot happen unless a fault condition in a practical circuit induces them.

Six Boolean equations for all six switching devices across all three-phase legs of a three-phase ZSI can be derived from the above table. Sum of Product is the method used to derive these equations which then give rise to the flow diagram figure 4.13. Below is a list of equations:

$$SS_1 = \bar{D}\bar{G} + DG\ (upper\ switch) \quad 4.31$$

$$SS_4 = D\bar{H} + \bar{D}H\ (lower\ switch) \quad 4.32$$

$$SS_2 = \bar{E}\bar{G} + EG\ (upper\ switch) \quad 4.33$$

$$SS_5 = E\bar{H} + \bar{E}H\ (lower\ switch) \quad 4.34$$

$$SS_3 = \bar{F}\bar{G} + FG\ (upper\ switch) \quad 4.35$$

$$SS_6 = F\bar{H} + \bar{F}H\ (lower\ switch) \quad 4.36$$

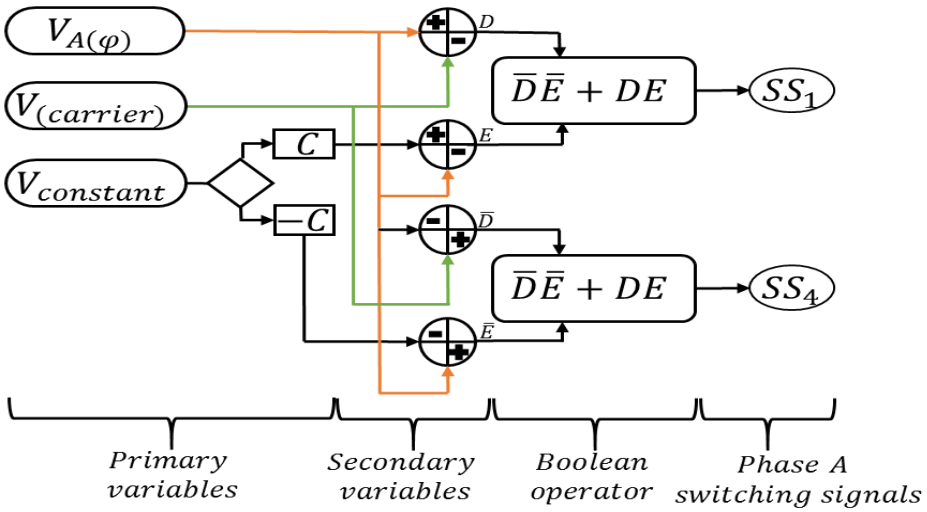


Figure 4.13: Simple boost technique PWM generator

The above flow diagram in figure 4.13 defines a control circuit for phase leg A only. However; a similar circuit applies to both phase legs B and C. The difference lies in the phase shift that differentiates between the three phases. Therefore; switching devices SS_1 and SS_4 make up phase leg A whose switching behaviour is defined by (4.31) and (4.32) respectively, S_2 and S_5 would make up phase leg B whose switching behaviour is defined by (4.33) and (4.34) respectively while S_3 and S_6 would make up phase leg C whose switching behaviour is defined by (4.35) and (4.36) respectively

The ratio of peak values of $V_{a(\varphi)}$, $V_{b(\varphi)}$ and $V_{c(\varphi)}$ in relation to that of $V_{carrier}$ is used to vary the modulation index and hence a shoot-through duty ratio and hence a boost factor. The output voltage for the SBC PWM control technique is given by (2.12) below and figure 4.14 - 4.19 is a set of results for the SBC PWM technique sampled when V_{in} was 200V and m at 0.65. The rest of the results are presented in table 4.5.

$$V_{ABC(\varphi)} = \sqrt{3}\, mB_{SBC} \frac{V_{IN}}{2}$$

$$where\ B_{SBC} = \frac{1}{2m-1}; 0.5 < m < 1 \qquad 4.37$$

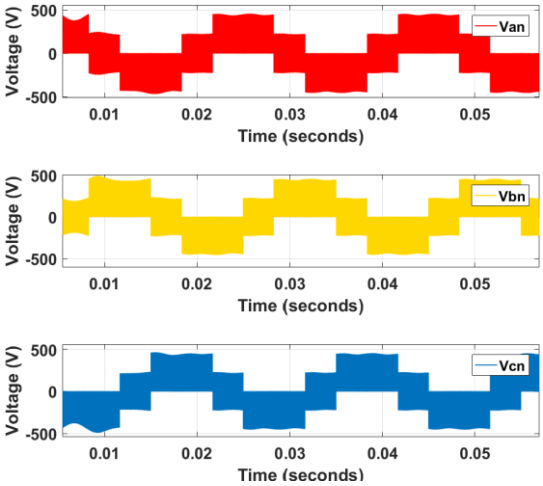


Figure 4.14: Unfiltered phase voltages (SBC)

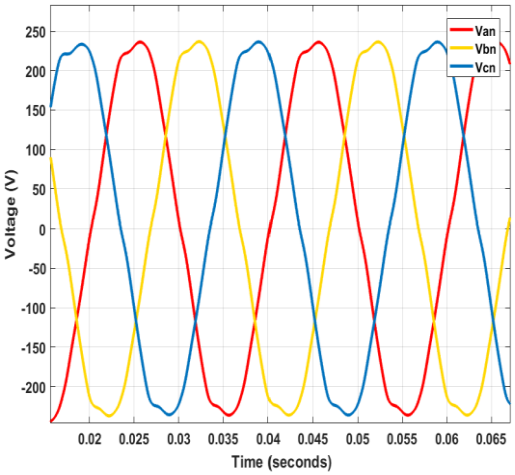


Figure 4.15: Filtered phase voltage (SBC)

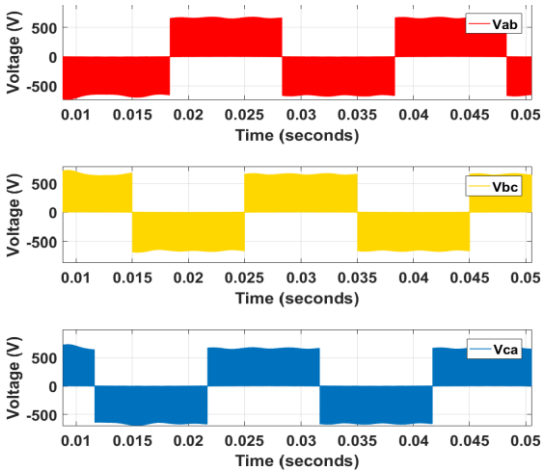


Figure 4.16: Unfiltered line voltages (SBC)

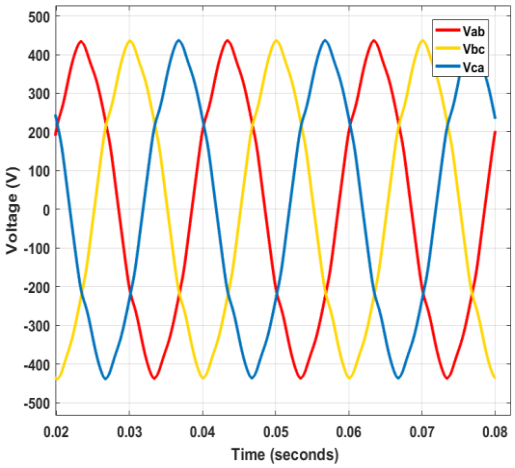


Figure 4.17: Filtered line voltage (SBC)

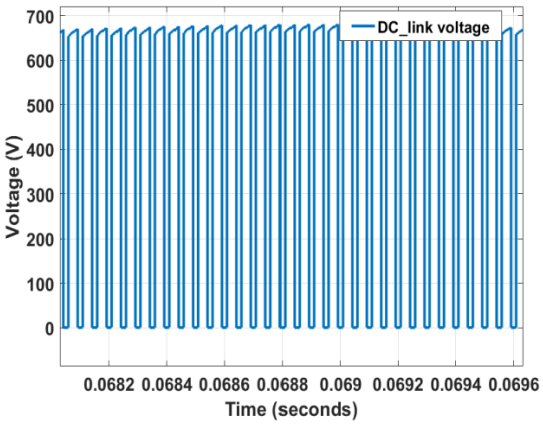


Figure 4.18: CD-link voltage (SBC)

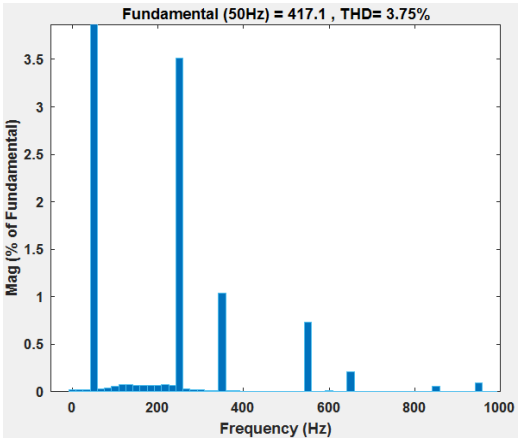


Figure 4.19: %THD (SBC)

Figure 4.14 and 4.15 show unfiltered and filtered phase voltages, figure 4.16 and 4.17 show unfiltered and filtered line voltages, figure 4.7 show a DC-link voltage while figure 4.8 shows the

percentage of total harmonic distortion of a line voltage. All this set of results was sampled at V_{in} of 200 and a modulation index of 0.65. Figure 4.3 to 4.8 confirm the expected results as per (2.12). The amplitude of phase and line waveforms, as well as a DC-link voltage, conform to (2.12) and the %THD is below 5% which is the South African national grid specification for percentage of total harmonics distortion as stipulated by SANS 10142 standard documents [5].

Table 4.5: Summary of SBC mode results

Varying input voltage and modulation index as per (2.12)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	644.8	968.7	1292	1616	389.2	584.3	779.8	975.1
4	$V_{AC(3\varphi)}$	216.5	325.0	433.8	542.0	150.0	225.0	300.0	375.0
5	$Stress-ratio$	2.980	2.981	2.980	2.982	2.595	2.597	2.599	2.600
6	B	3.224	3.229	3.230	3.232	1.946	1.948	1.950	1.950
7	mB	2.096	2.099	2.100	2.101	1.460	1.461	1.462	1.463
8	%THD	3.750	3.750	3.750	3.750	1.140	1.140	1.140	1.140
Table 4.5 continues below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	284.2	426.9	569.5	712.2	221.2	332.3	443.3	554.5
4	$V_{AC(3\varphi)}$	121.5	182.4	243.4	304.0	105.6	158.5	211.5	264.0
5	$Stress-ratio$	2.339	2.340	2.339	2.342	2.095	2.096	2.096	2.100
6	B	1.421	1.423	1.424	1.424	1.106	1.108	1.109	1.109
7	mB	1.208	1.210	1.210	1.211	1.051	1.052	1.053	1.053
8	%THD	0.140	0.140	0.140	0.140	0.140	0.140	0.140	0.140

4.2.2.2. Analysis of results of simple boost pulse width modulation

A couple of relationships can be pulled out of table 4.5. The voltage stress across the switching devices, the boost factor (and hence the gain factor) as well as the percentage of total harmonics distortion are exclusively dependent on the modulation index. All these parameters show a decrease with the increase in the modulation index. The output voltage, as well as the DC-link voltage, is dependent on both the input voltage and modulation index. Both the output voltage and the DC-link voltage increase with the increase in either the input voltage or the modulation index; the opposite is also true. Refer to the following figures for above-mentioned relationships:

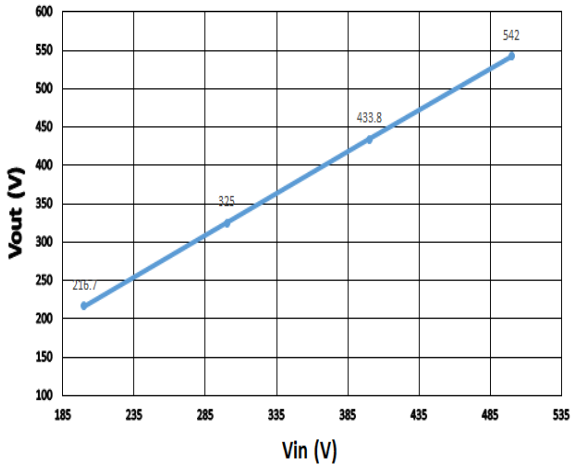


Figure 4.20: V_{out} vs V_{in} for SBC (m = 0.65)

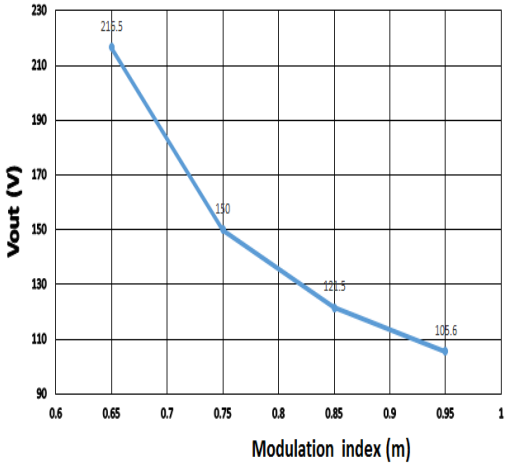


Figure 4.21: V_{out} vs m for SBC (Vin = 200V)

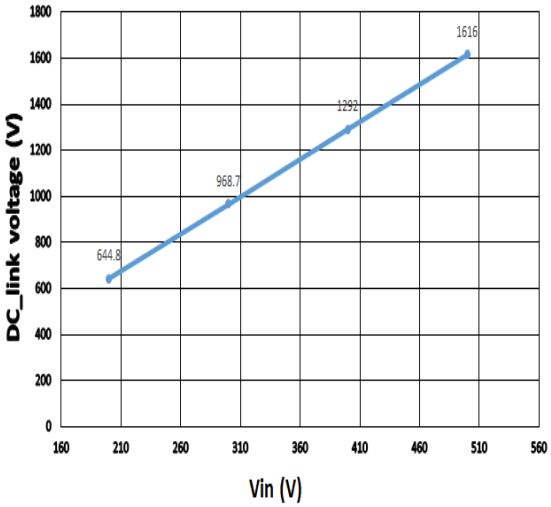


Figure 4.22: $V_{DC\text{-}link}$ vs V_{in} for SBC (m = 0.65)

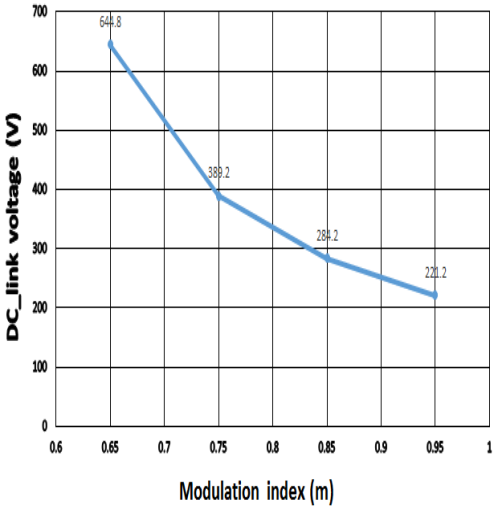


Figure 4.23: $V_{DC\text{-}link}$ vs m for SBC (Vin = 200V)

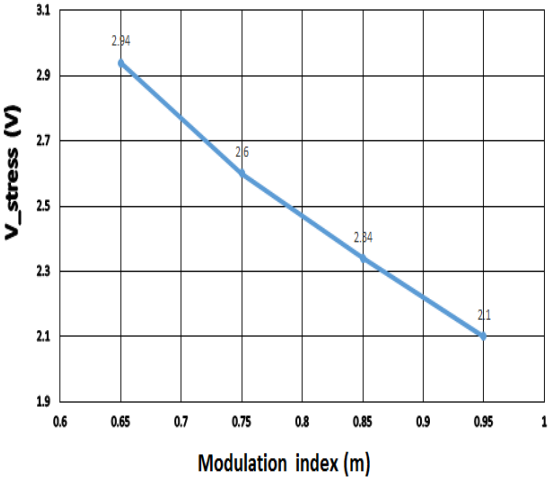


Figure 4.24: V_{stress} vs m for SBC

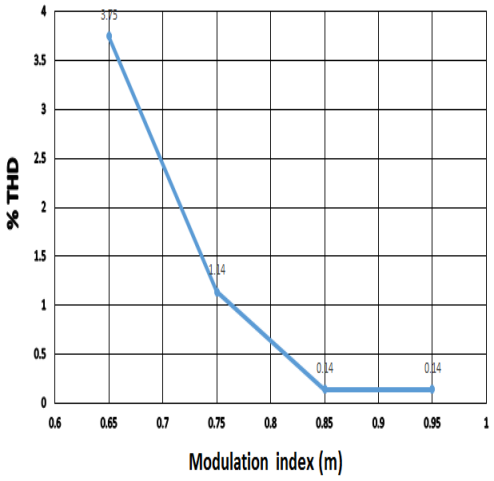


Figure 4.25: % THD for m SBC

Figures 4.20 – 4.24 are derived from table 4.5 and confirms the expected relationships as per (2.12) and (4.37). Figure 4.20 together row 2 and 4 of table 4.5 shows that V_{out} increases with an

increase in V_{in} to according to (2.12). Figure 4.21 together with row 1 and 4 of table 4.5 also shows that V_{out} increases with increase in m according to (2.12). Figure 4.22 shows that a DC-link voltage increases with an increase in input voltage according to (2.12). Figure 4.23 shows that DC-link voltage decreases with an increase in modulation index according to (2.12). Figure 4.24 together with row 3 and 4 show that the voltage stress across the switching devices is decreasing with increase in modulation index. Figure 4.25 together with row 1 and 6 shows that the % total harmonics distortion is exclusively dependent on the modulation index; it does not change with variation in the input voltage, however, it decreases with an increase in the modulation index.

Taking column 18 as an example (V_{in} = 500 V, m = 0.95), refer to the following calculations and table 4.6 that compare the actual and theoretical values for this case.

Theoretically:

$$B_{SBC} = \frac{1}{2m-1} = 1.11$$

$$\therefore V_{ABC(\varphi)} = \sqrt{3}\, mB \frac{V_{IN}}{2} = 457.1\, V_{line}\ (263.9\, V_{phase})$$

$$V_{DClink} = BV_{IN} = 555.6\, V$$

$$V_{stress} = \frac{V_{DClink}}{V_{ABC(\varphi)}} = 2.105$$

Table 4.6: Theoretical vs practical parameters for SBC method

Parameter	Theoretical value	Practical value
B	1.111	1.109
V_{DClink}	555.6	554.5
Stress_ratio	2.105	2.100
$V_{ABC(\varphi)}$	263.9 V_{phase}	264.0 V_{phase}

4.2.3. Constant boost PWM technique (CBC)

4.2.3.1. Design of Constant boost PWM technique control circuit and presentation of results

The only difference between Simple boost PWM technique and constant boost PWM technique is the formulation of a three-phase fundamental reference waveform. For the CBC control

technique, a fundamental reference signal is injected with a third harmonic signal of 16% magnitude to form a third-harmonic injected three-phase fundamental waveform [17].

$$V_{ac(3\varphi,TH-Injected)} = \begin{cases} V_{A(\varphi)} + V_{(3rd\ harmonic)} \\ V_{B(\varphi)} + V_{(3rd\ harmonic)} \\ V_{C(\varphi)} + V_{(3rd\ harmonic)} \end{cases}$$

$$\therefore V_{ac(3\varphi,TH-Injected)} = \begin{cases} 1.156\sin(\omega t) + 0.167sin(3\omega t) \\ 1.156\sin(\omega t - 120°) + 0.167sin(3\omega t) \\ 1.156\sin(\omega\ - 240°) + 0.167sin(3\omega t) \end{cases} \quad 4.38$$

Except for the above-stated formulation difference of the fundamental signal and the new definition of the boost factor below, everything remains similar to a case of the SBC PWM control technique. The output voltage for the CBC PWM control technique is given by (2.12) below and figure 4.14 - 4.19 is a set of results for the SBC PWM technique sampled when V_{in} was 200V and m at 0.65. The rest of the results are presented in table 4.7.

$$V_{ABC(\varphi)} = \sqrt{3}\, mB_{CBC}\frac{V_{IN}}{2}$$

$$B_{CBC} = \frac{1}{\sqrt{3}m - 1}; 0.577 < m < 1.155 \quad 4.39$$

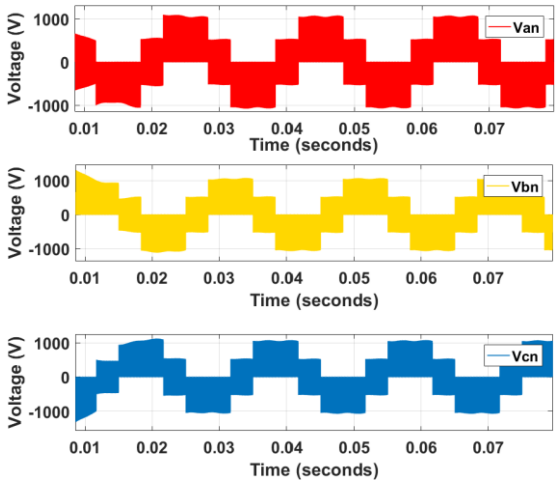


Figure 4.26: Unfiltered phase voltages for CBC

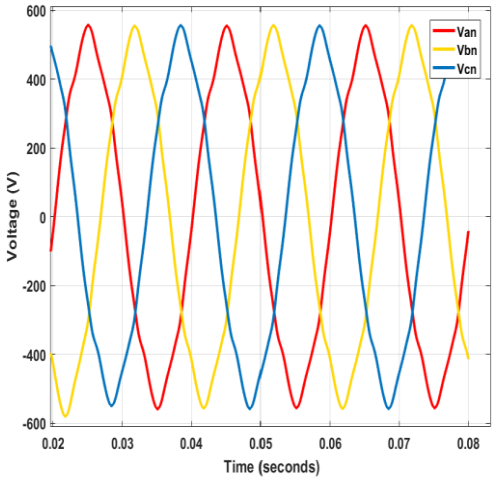


Figure 4.27: Filtered phase voltage for CBC

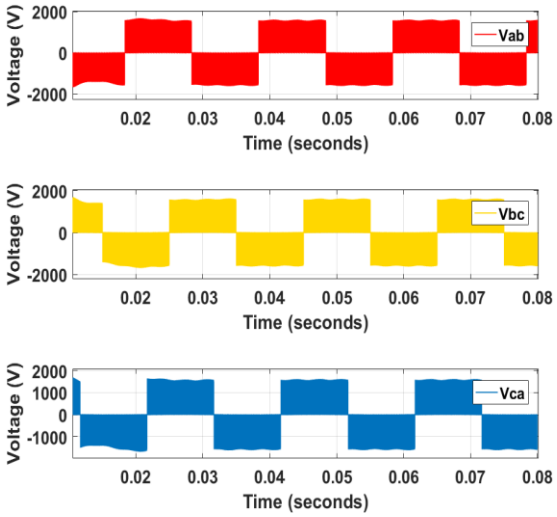


Figure 4.28: Unfiltered line voltages for CBC

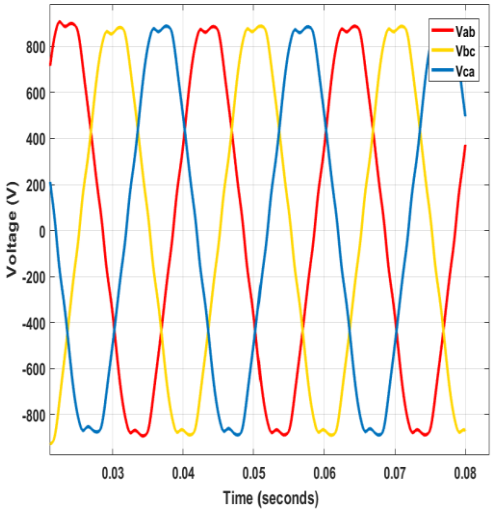


Figure 4.29: Filtered line voltage for CBC

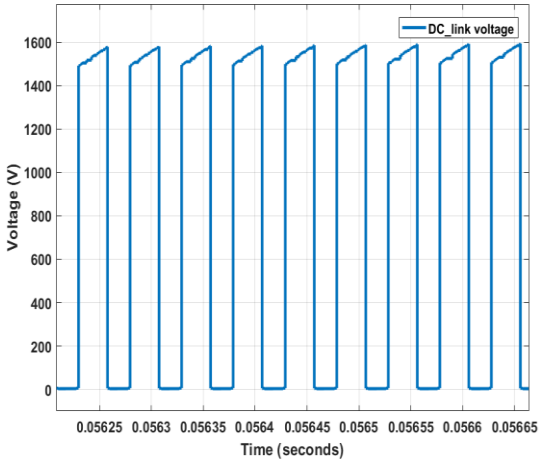


Figure 4.30: V_{stress} vs m for CBC

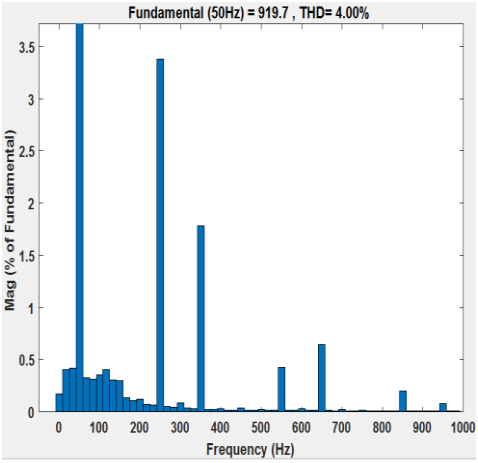


Figure 4.31: % THD for m CBC

Figure 4.26 and 4.27 show unfiltered and filtered phase voltages, figure 4.28 and 4.29 show unfiltered and filtered line voltages, figure 4.30 shows a DC-link voltage while figure 4.8 shows the percentage of total harmonic distortion of a line voltage. All this set of results was sampled at V_{in} of 200 and a modulation index of 0.65. Figures 4.27 to 4.31 confirm the expected results as per (2.12). The amplitude of phase and line waveforms, as well as a DC-link voltage, conform to (2.12) and the %THD is below 5% which is the South African national grid specification for percentage of total harmonics distortion as stipulated by SANS 10142 standard documents [5].

Table 4.7: Summary of CBC mode results

Varying input voltage and modulation index as per (2.13)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	1590	2401	3200	4000	670.0	1000	1350	1680
4	$V_{AC(3\varphi)}$	888.0	1337	1780	2230	440.0	655.0	875.1	1092
5	Stress − ratio	1.791	1.796	1.797	1.794	1.523	1.527	1.543	1.538
6	B	7.950	8.003	8.000	8.000	3.350	3.333	3.375	3.360
7	mB	5.168	5.202	5.200	5.200	2.513	2.500	2.531	2.520
8	%THD	4.000	4.000	4.000	4.000	3.720	3.720	3.720	3.720
Table 4.7 continues below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	422.0	640	850.0	1050	310.0	465.0	620.0	780.0
4	$V_{AC(3\varphi)}$	332.0	490.1	650.3	803.0	260.2	391.0	521.2	650.0
5	Stress − ratio	1.271	1.306	1.307	1.308	1.191	1.189	1.189	1.200
6	B	2.110	2.133	2.125	2.100	1.550	1.550	1.550	1.560
7	mB	1.794	1.813	1.806	1.785	1.473	1.473	1.473	1.482
8	%THD	2.680	2.680	2.680	2.680	3.950	3.950	3.950	3.950

4.2.3.2. Analysis of results of constant boost pulse width modulation

A couple of relationships can be pulled out of table 4.7. The voltage stress across the switching devices, the boost factor (and hence the gain factor) as well as the percentage of total harmonics distortion are exclusively dependent on the modulation index and all decrease with the increase in the modulation index. The output voltage, as well as the DC-link voltage, is dependent on both the input voltage and modulation index. Both the output voltage and the DC-link voltage increase with the increase in either the input voltage or the modulation index; the opposite is also true. Refer to the following figures for the above-mentioned relationships:

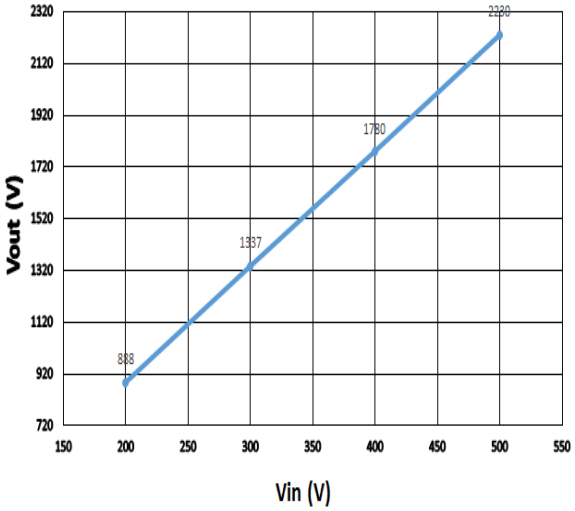


Figure 4.32: V_{out} vs V_{in} for CBC (m = 0.65)

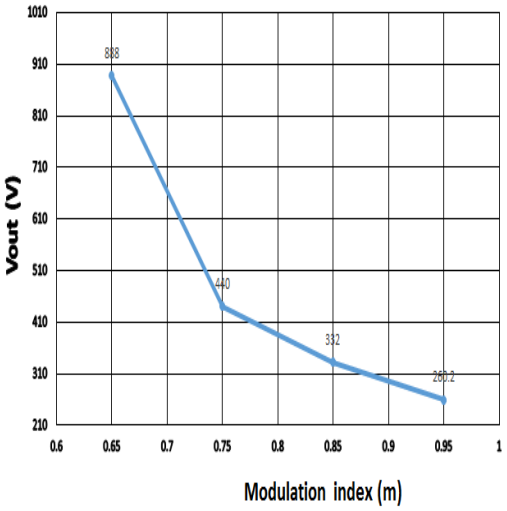


Figure 4.33: V_{out} vs m for CBC (Vin = 200V)

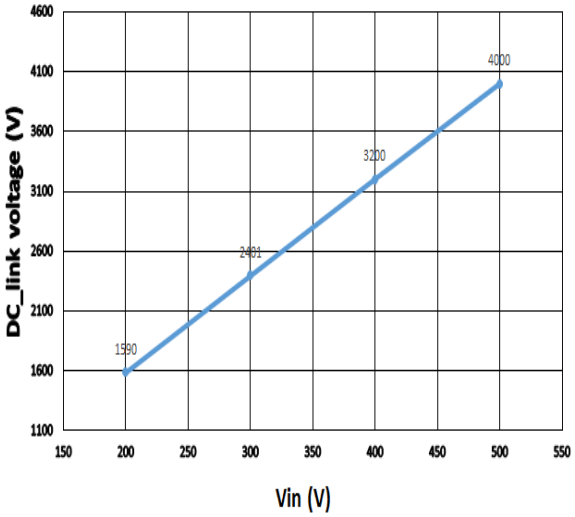


Figure 4.34: $V_{DC\text{-}link}$ vs V_{in} for CBC (m = 0.65)

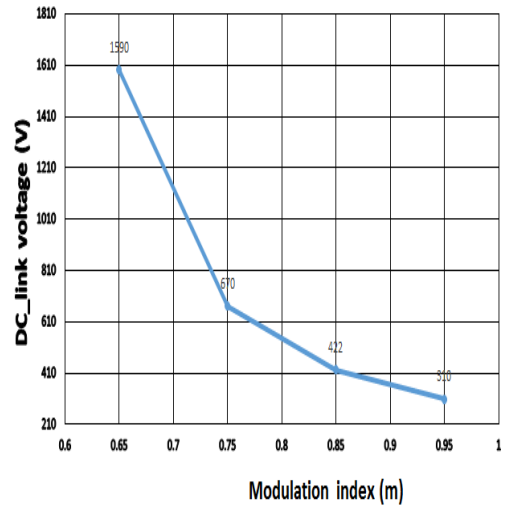


Figure 4.35: $V_{DC\text{-}link}$ vs m for CBC (Vin = 200V)

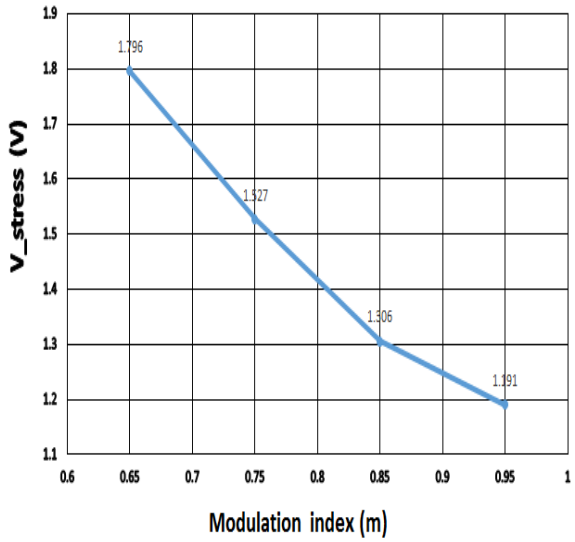


Figure 4.36: V_{stress} vs m for CBC

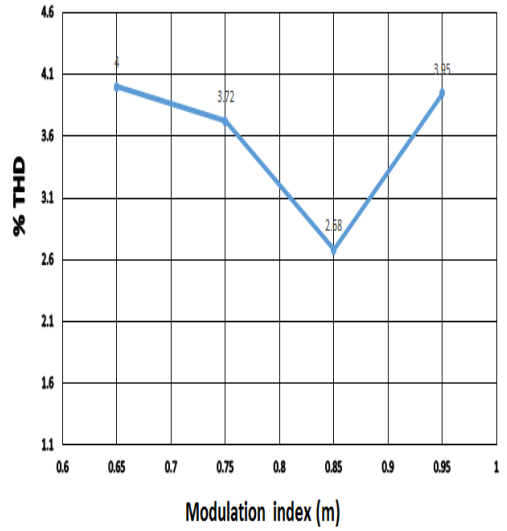


Figure 4.37: % THD for m CBC

Figures 4.32 – 4.37 are derived from table 4.5 and confirm the expected relationships as per (2.13) and (4.39). Figure 4.32 together rows 2 and 4 of table 4.7 shows that V_{out} increases with an increase in V_{in} to according to (2.13). Figure 4.33 together with row 1 and 4 of table 4.7 also shows that V_{out} increases with an increase in m according to (2.13). Figure 4.34 shows that a DC-link voltage increases with an increase in input voltage according to (2.13). Figure 4.35 shows that DC-link voltage decreases with an increase in modulation index according to (2.13). Figure 4.36 together with row 3 and 4 show that the voltage stress across the switching devices is decreasing with an increase in modulation index. Figure 4.37 together with row 1 and 6 shows that the % total harmonics distortion is exclusively dependent on the modulation index; it does not change with variation in the input voltage, it has a non-linear relationship with modulation index.

Taking column 17 as an example (V_{in} = 400 V, m = 0.95); refer to the following calculations and table 4.8 that compare the actual and theoretical values for this case.

Theoretically:

$$B_{CBC} = \frac{1}{\sqrt{3}m - 1} = 1.55$$

$$\therefore V_{ABC(\varphi)} = \sqrt{3}\, mB_{CBC}\frac{V_{IN}}{2} = 509.9\, V_{line}\ (294.4\, V_{phase})$$

$$V_{DClink} = B_{CBC}V_{IN} = 619.7\, V$$

$$V_{stress} = \frac{V_{DClink}}{V_{ABC(\varphi)}} = 1.22$$

Table 4.8: Theoretical vs practical parameters

Parameter	Theoretical value	Practical value
B	1.549	1.550
V_{DClink}	619.7	620.0
Stress_ratio	1.215	1.189
$V_{ABC(\varphi)}$	294.4 V_{phase}	300.9 V_{phase}

4.2.4. Maximum boost PWM technique

4.2.4.1. Design of Maximum boost PWM technique control circuit and presentation of results

This control scheme makes use of $V_{ac(3\varphi)}$ and $V_{carrier}$ only. All of the zero states are converted to the shoot-through state in order to obtain a maximum boost factor. The behaviour of the signal generator for maximum boost technique can completely be defined by the following six secondary Boolean variables:

$$I = V_{A(\varphi)} - V_{B(\varphi)} \quad 4.40$$

$$J = V_{B(\varphi)} - V_{C(\varphi)} \quad 4.41$$

$$K = V_{C(\varphi)} - V_{A(\varphi)} \quad 4.42$$

$$L = V_{A(\varphi)} - V_{(carrier)} \quad 4.43$$

$$M = V_{B(\varphi)} - V_{(carrier)} \quad 4.44$$

$$N = V_{C(\varphi)} - V_{(carrier)} \quad 4.45$$

The desired switching pattern of the PWM generator controlling the ZSI can completely be defined using the above formulated secondary variables, I-N together with the switching states of switching devices, SSS_1 – SSS_6. Therefore; table 4.9 below is a truth table showing states of each switching device at all secondary variable state possibilities, thus defining a complete behaviour of the MBC PWM controller required to give out the required three-phase signal (4.1).

Table 4.9 translates directly to a PWM controller that implements a maximum boost control technique. The highlighted states with bold font are the shoot-through state. 'Impossible' states consider contradictory cases such as $V_{a(\varphi)}$ being greater than $V_{b(\varphi)}$ which is also greater $V_{c(\varphi)}$ however $V_{c(\varphi)}$ is greater than $V_{a(\varphi)}$ in contrast (I, J, K = 1). These are kind of states which cannot happen unless a fault condition in a practical circuit induces them.

Table 4.9: Truth table for the maximum boost PWM controller

+VE peak shoot-through									
Case	I	J	K	L	M	N	SSS_1	SSS_2	SSS_3
0	0	0	0	0	0	0	impossible	impossible	impossible
1	0	0	0	0	0	1	impossible	impossible	impossible
2	0	0	0	0	1	0	impossible	impossible	impossible
3	0	0	0	0	1	1	impossible	impossible	impossible
4	0	0	0	1	0	0	impossible	impossible	impossible
5	0	0	0	1	0	1	impossible	impossible	impossible
6	0	0	0	1	1	0	impossible	impossible	impossible
7	0	0	0	1	1	1	impossible	impossible	impossible
8	**0**	**0**	**1**	**0**	**0**	**0**	**impossible**	**impossible**	**1**
9	0	0	1	0	0	1	impossible	impossible	1
10	0	0	1	0	1	0	impossible	impossible	1
11	0	0	1	0	1	1	impossible	impossible	1
12	0	0	1	1	0	0	0	1	1
13	0	0	1	1	0	1	impossible	impossible	1
14	0	0	1	1	1	0	0	0	1
15	0	0	1	1	1	1	1	1	1
16	**0**	**1**	**0**	**0**	**0**	**0**	**impossible**	**1**	**impossible**
17	0	1	0	0	0	1	1	1	0
18	0	1	0	0	1	0	impossible	1	impossible
19	0	1	0	0	1	1	impossible	1	impossible
20	0	1	0	1	0	0	impossible	1	impossible
21	0	1	0	1	0	1	0	1	0
22	0	1	0	1	1	0	impossible	1	impossible
23	0	1	0	1	1	1	1	1	1
24	**0**	**1**	**1**	**0**	**0**	**0**	**impossible**	**1**	**impossible**
25	0	1	1	0	0	1	impossible	1	impossible
26	0	1	1	0	1	0	impossible	1	impossible
27	0	1	1	0	1	1	impossible	1	impossible
28	0	1	1	1	0	0	0	1	1
29	0	1	1	1	0	1	0	1	0
30	0	1	1	1	1	0	Impossible	1	impossible
31	0	1	1	1	1	1	1	1	1
32	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**impossible**	**impossible**
33	1	0	0	0	0	1	1	impossible	impossible
34	1	0	0	0	1	0	1	0	1
35	1	0	0	0	1	1	1	0	0
36	1	0	0	1	0	0	1	impossible	impossible
37	1	0	0	1	0	1	1	impossible	impossible
38	1	0	0	1	1	0	1	impossible	impossible
39	1	0	0	1	1	1	1	1	1
40	**1**	**0**	**1**	**0**	**0**	**0**	**impossible**	**impossible**	**1**
41	1	0	1	0	0	1	impossible	impossible	1
42	1	0	1	0	1	0	1	0	1

Table 4.9 continued									
43	1	0	1	0	1	1	impossible	impossible	1
45	1	0	1	1	0	1	impossible	impossible	1
46	1	0	1	1	1	0	0	0	1
47	1	0	1	1	1	1	1	1	1
48	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**impossible**	**impossible**
49	1	1	0	0	0	1	1	1	0
50	1	1	0	0	1	0	1	impossible	impossible
51	1	1	0	0	1	1	1	0	0
52	1	1	0	1	0	0	1	impossible	impossible
53	1	1	0	1	0	1	1	impossible	impossible
54	1	1	0	1	1	0	1	impossible	impossible
55	1	1	0	1	1	1	1	1	1
56	1	1	1	0	0	0	impossible	impossible	impossible
57	1	1	1	0	0	1	impossible	impossible	impossible
58	1	1	1	0	1	0	impossible	impossible	impossible
59	1	1	1	0	1	1	impossible	impossible	impossible
60	1	1	1	1	0	0	impossible	impossible	impossible
61	1	1	1	1	0	1	impossible	impossible	impossible
62	1	1	1	1	1	0	impossible	impossible	impossible
63	1	1	1	1	1	1	impossible	impossible	impossible

Deriving the Boolean equations for switching devices by a mere SOP method would lead to unnecessarily long equations. Each equation would have 22 to 24 terms which would require for not less than 132 to 144 individual gates to implement a corresponding control circuit. However; thanks to an optimising tool called a karnaugh map (k-map), equations for all six switching devices can be optimised such that they have 5 to 7 terms.

Phase leg A (SSS_1 and SSS_4):

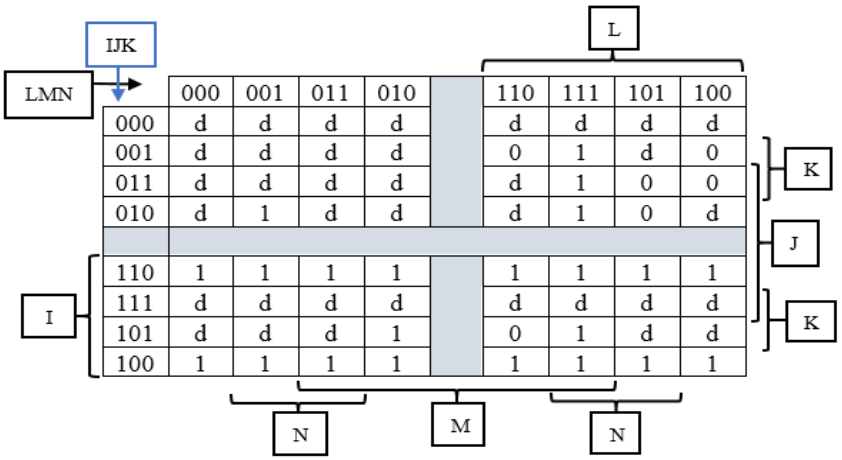


Figure 4.38: Phase leg A k-map

Figure 4.38 is a k-map for optimising a Boolean equation defining switching behaviour of the upper switching device of phase leg A (SSS_1). An optimum equation for the upper switching device of phase leg A can be derived from the above k-map utilising the SOP method. A Boolean function for the lower switching device (SSS_4) is hence derived from that of the upper switching device by negating all individual secondary variables across the equation of SSS_1. Note that 'd' denotes an 'impossible' state.

$$SSS_1 = I\bar{J}\bar{K} + IJ\bar{K} + I\bar{J}LMN + J\bar{K}\bar{L}\bar{M}N + J\bar{K}LMN + \bar{I}KLMN \quad 4.46$$

$$SSS_4 = \bar{I}JK + \bar{I}\bar{J}K + \bar{I}\,J\bar{L}\bar{M}\bar{N} + \bar{J}\,KLM\bar{N} + \bar{J}\,K\bar{L}\bar{M}\bar{N} + I\bar{K}\bar{L}\bar{M}\bar{N} \quad 4.47$$

Phase leg B (SSS_2 and SSS_5):

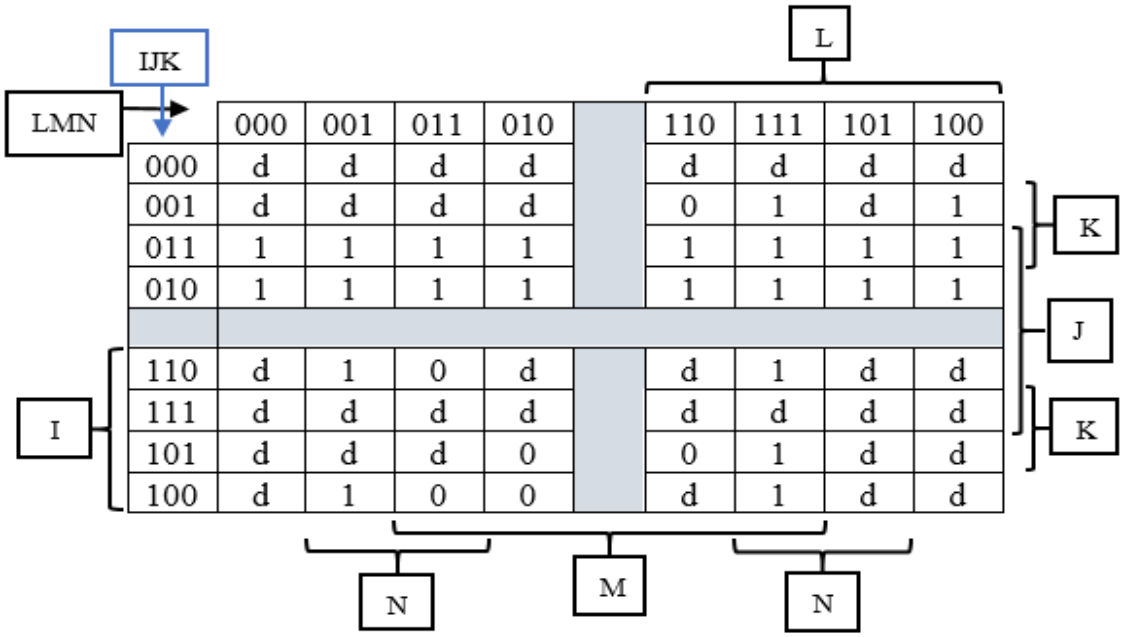


Figure 4.39: Phase leg B k-map

Figure 4.39 is a k-map for optimising a Boolean equation defining switching behaviour of the upper switching device of phase leg A (SSS_2). An optimum equation for the upper switching device of phase leg A can be derived from the above k-map utilising the SOP method. A Boolean function for the lower switching device (SSS_5) is hence derived from that of the upper switching device by negating all individual secondary variables across the equation of SSS_2. Note that 'd' denotes an 'impossible' state.

$$SSS_2 = \bar{I}J + I\bar{J}LMN + \bar{I}KLMN + \bar{I}\,KL\bar{M}\bar{N} + J\bar{K}LMN + J\bar{K}\bar{L}\bar{M}N \quad 4.48$$

$$SSS_5 = I\bar{J} + \bar{I}J\bar{L}\bar{M}\bar{N} + I\bar{K}\bar{L}\bar{M}\bar{N} + I\bar{K}\bar{L}MN + \bar{J}\,K\bar{L}\bar{M}\bar{N} + \bar{J}\,KLM\bar{N} \quad 4.49$$

Phase leg A (SSS_3 and SSS_6):

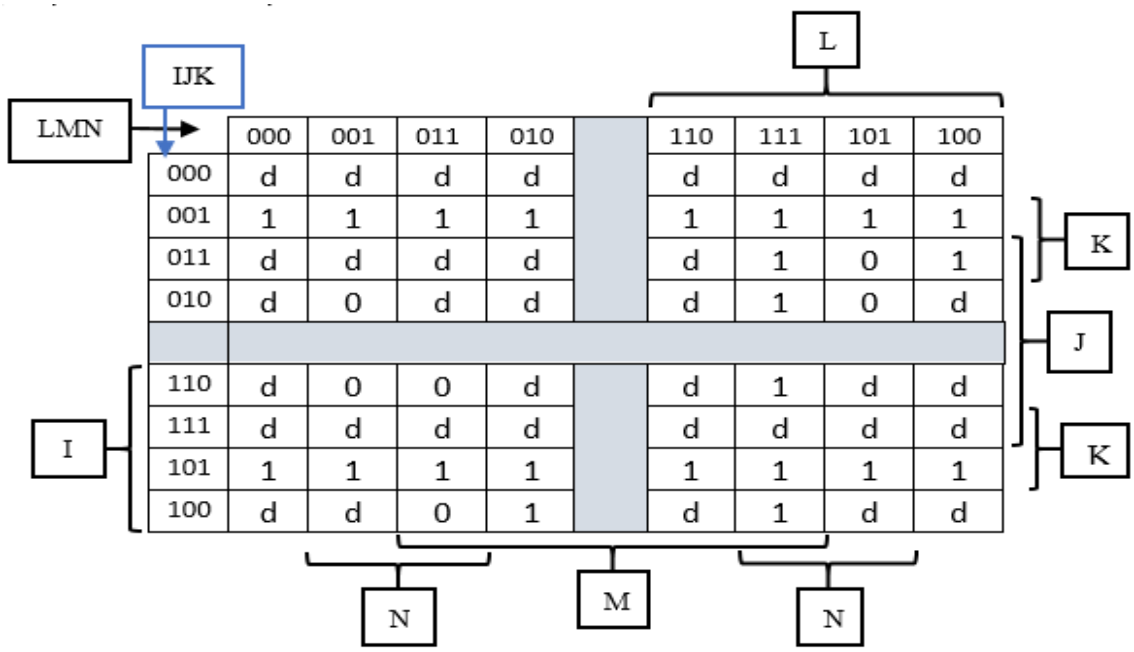


Figure 4.40: Phase leg C k-map

Figure 4.40 is a k-map for optimising a Boolean equation defining switching behaviour of the upper switching device of phase leg A (SSS_3). An optimum equation for the upper switching device of phase leg A can be derived from the above k-map utilising the SOP method. A Boolean function for the lower switching device (SSS_6) is hence derived from that of the upper switching device by negating all individual secondary variables across the equation of SSS_3. Note that 'd' denotes an 'impossible' state.

$$SSS_3 = I\bar{J}K + \bar{I}\bar{J}K + \bar{I}KLMN + I\bar{J}\,\bar{L}M\bar{N} + I\bar{J}LMN + J\bar{K}LMN + \bar{I}KL\bar{M}\bar{N} \quad 4.50$$

$$SSS_6 = \bar{I}J\bar{K} + IJ\bar{K} + I\bar{K}\bar{L}\bar{M}\bar{N} + \bar{I}\,JL\bar{M}N + \bar{I}\,J\bar{L}\bar{M}\bar{N} + \bar{J}K\bar{L}\bar{M}\bar{N} + I\bar{K}\bar{L}MN \quad 4.51$$

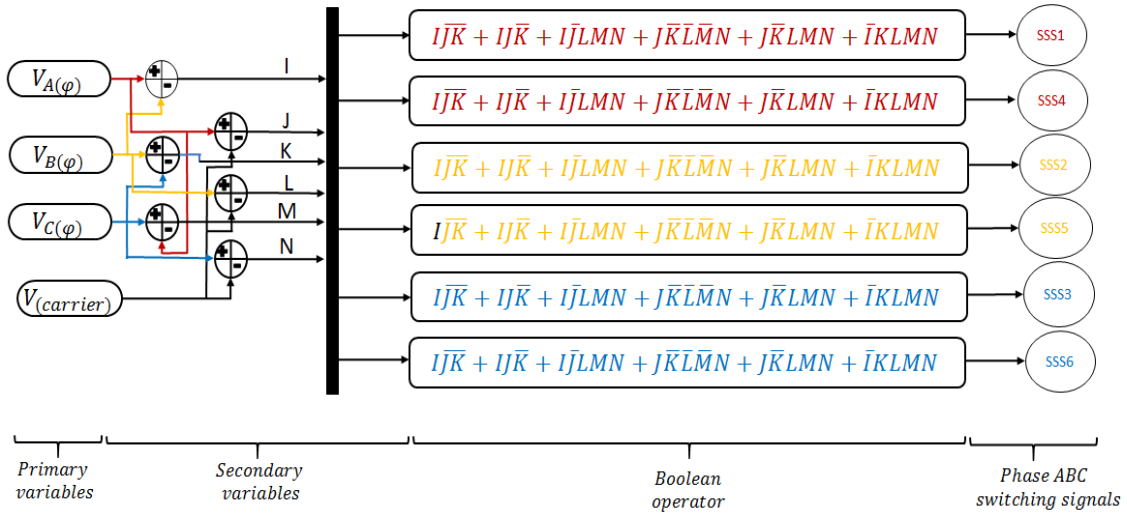


Figure 4.41: MBC technique PWM generator

The above flow diagram in figure 4.41 defines a control circuit for all phase legs, A, B and C. Switching devices SSS_1 and SSS_4 make up phase leg A whose switching behaviour is defined by (4.46) and (4.47) respectively, SSS_2 and SSS_5 make up phase leg B whose switching behaviour is defined by (4.48) and (4.49) respectively while SSS_3 and SSS_6 make up phase leg C whose switching behaviour is defined by (4.50) and (4.51) respectively. The following list of figures is a sample of results taken when V_{in} was 200V and m at 0.65. The rest of the results are presented in table 4.10.

$$V_{ABC(\varphi)} = \sqrt{3}\, mB_{MBC}\frac{V_{IN}}{2}$$

$$B_{MBC} = \frac{\pi}{3\sqrt{3}m - \pi}; 0.605 < m < 1 \qquad 4.52$$

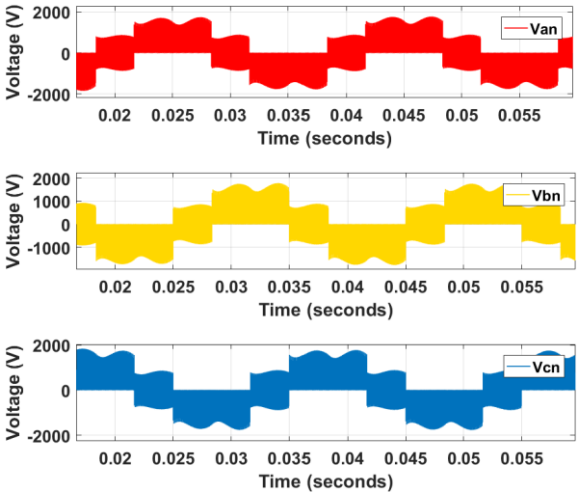


Figure 4.42: Unfiltered phase voltages for MBC

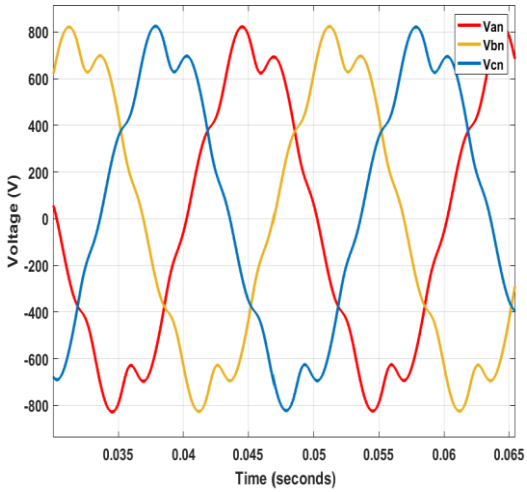


Figure 4.43: Filtered phase voltage for MBC

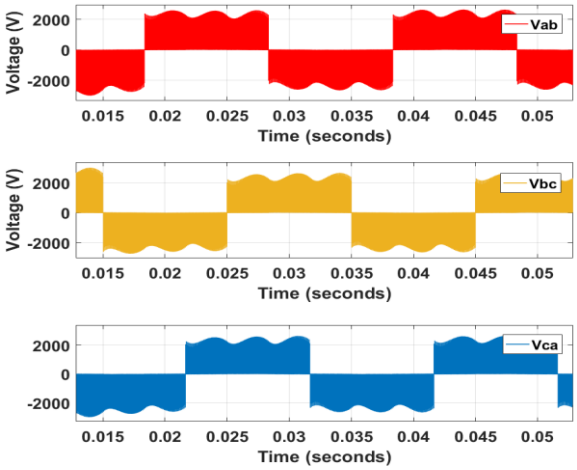


Figure 4.44: Unfiltered line voltages for MBC

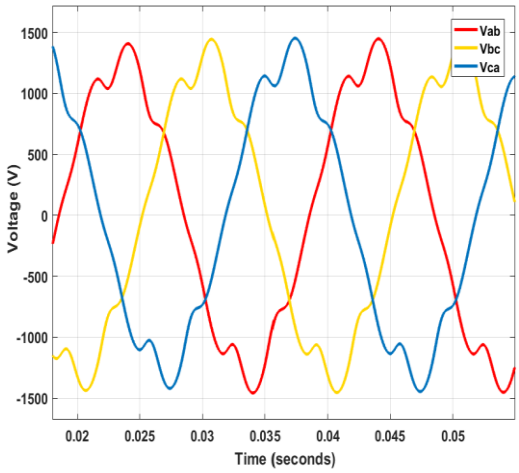


Figure 4.45: Filtered line voltage for MBC

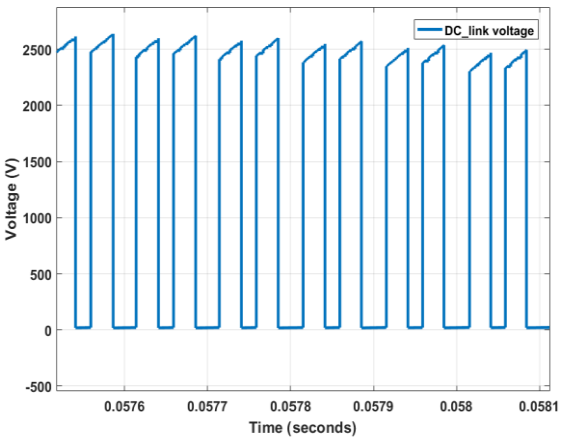


Figure 4.46: V_{stress} vs m for MBC

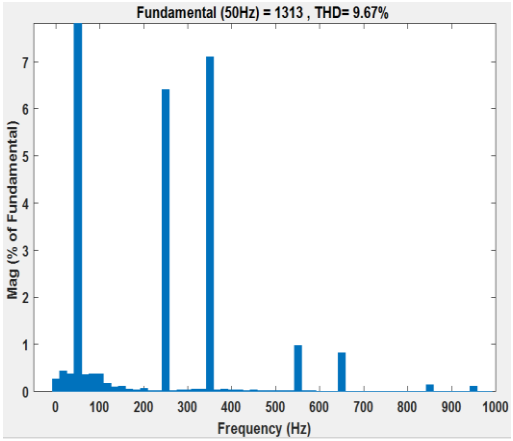


Figure 4.47: % THD for m MBC

Table 4.10: Summary of MBC mode results

Varying input voltage and modulation index as per (2.14)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	2601	3903	4900	6000	810.0	1225	1625	2050
4	$V_{AC(3\varphi)}$	1465	2195	2950	3615	595.1	895	1189	1487
5	Stress – ratio	1.776	1.778	1.651	1.658	1.361	1.369	1.367	1.379
6	B	13.01	13.01	12.25	12.00	4.05	4.083	4.063	4.100
7	mB	8.453	8.457	7.963	7.800	3.038	3.063	3.047	3.075
8	%THD	10.37	10.37	10.37	10.37	9.260	9.260	9.260	9.26
Table 4.10 continues below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	500.2	755.0	1005	1252	375.0	550.0	720.0	900.0
4	$V_{AC(3\varphi)}$	380.5	563.7	750.2	927.5	303.2	449.6	594.7	740.1
5	Stress – ratio	1.316	1.339	1.339	1.349	1.237	1.223	1.212	1.216
6	B	2.501	2.517	2.513	2.504	1.875	1.741	1.800	1.800
7	mB	2.126	1.813	1.806	1.785	1.781	1.473	1.710	1.710
8	%THD	15.03	15.03	15.03	15.03	15.03	15.03	15.03	15.03

4.2.4.2. Analysis of results of constant boost pulse width modulation

A couple of relationships can be pulled out of table 4.10. The voltage stress across the switching devices, the boost factor (and hence the gain factor) as well as the percentage of total harmonics distortion are exclusively dependent on the modulation index and all decrease with the increase in the modulation index. The output voltage, as well as the DC-link voltage, is dependent on both the input voltage and modulation index. Both the output voltage and the DC-link voltage increase with the increase in either the input voltage or the modulation index; the opposite is also true. Refer to the following figures for above-mentioned relationships:

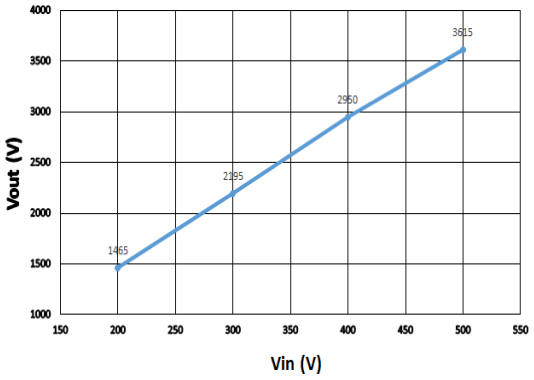


Figure 4.48: V_{out} vs V_{in} for MBC (m = 0.65)

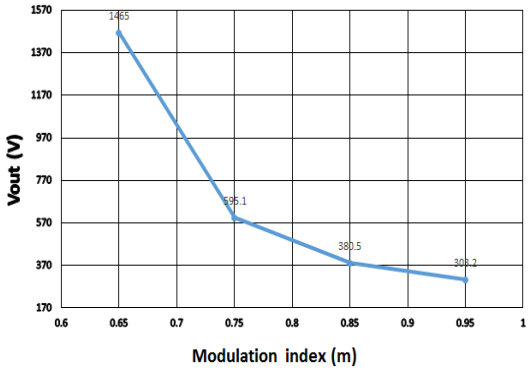


Figure 4.49: V_{out} vs m for MBC (Vin = 200V)

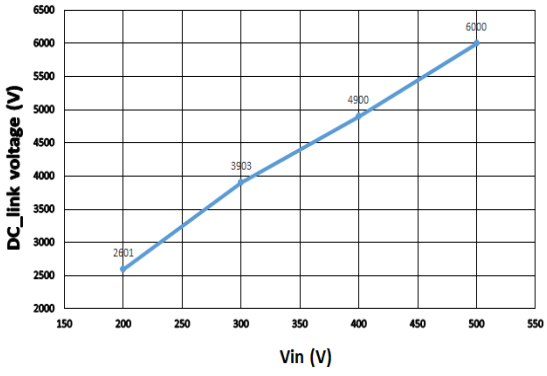


Figure 4.50: $V_{DC\text{-}link}$ vs V_{in} for MBC (m = 0.65)

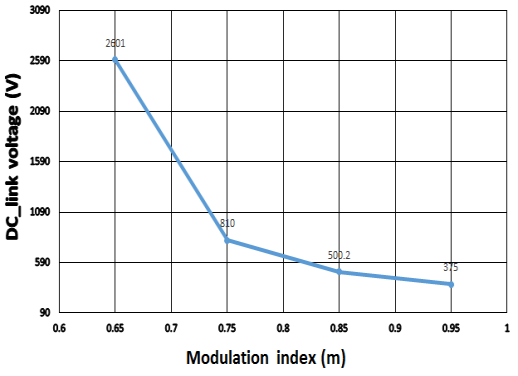


Figure 4.51: $V_{DC\text{-}link}$ vs m for MBC (Vin = 200V)

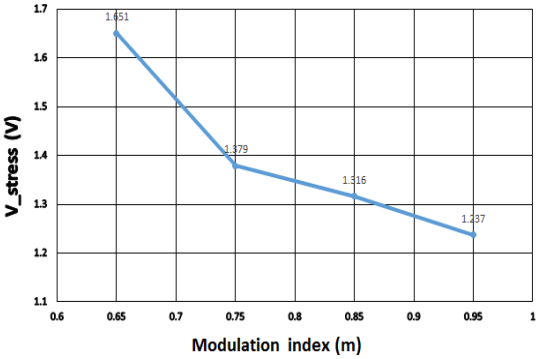


Figure 4.52: V_{stress} vs m for MBC

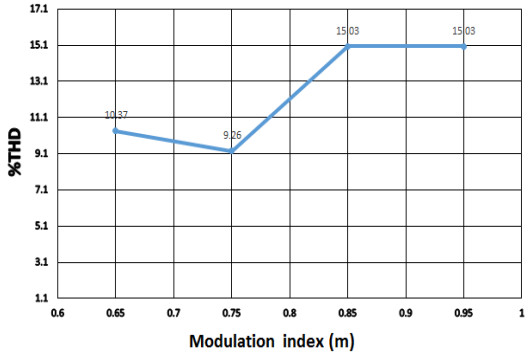


Figure 4.53: % THD for m MBC

Figures 4.48 – 4.53 are derived from table 4.10 and confirm the expected relationships as per (2.14) and (4.52). Figure 4.48 together rows 2 and 4 of table 4.10 shows that V_{out} increases with an increase in V_{in} to according to (2.14). Figure 4.49 together with row 1 and 4 of table 4.10 also shows that V_{out} increases with an increase in m according to (2.14). Figure 4.50 shows that a DC-link voltage increases with an increase in input voltage according to (2.14). Figure 4.51 shows that DC-link voltage decreases with an increase in a modulation index according to (2.14). Figure 4.52 together with row 3 and 4 show that the voltage stress across the switching devices is decreasing with increase in modulation index. Figure 4.53 together with row 1 and 6 shows that the % total harmonics distortion is exclusively dependent on the modulation index; it does not change with variation in the input voltage, it has a non-linear relationship with modulation index.

Taking column 12 as an example (V_{in} = 300 V, m = 0.85); refer to the following calculations and table 4.11 that compare the actual and theoretical values for this case.

Theoretically:

$$B_{MBC} = \frac{\pi}{3\sqrt{3}m - \pi} = 2.464$$

$$\therefore V_{ABC(\varphi)} = \sqrt{3}\, mB_{MBC}\frac{V_{IN}}{2} = 544.1\ V_{line}\ (314.1\ V_{phase})$$

$$V_{DClink} = B_{MBC}V_{IN} = 739.1\ V$$

$$V_{stress\_ratio} = \frac{V_{DClink}}{V_{ABC(\varphi)}} = 1.358$$

Table 4.11: Theoretical vs practical parameters

Parameter	Theoretical value	Practical value
B	2.464	2.513
V_{DClink}	739.1	750.2
Stress_ratio	1.358	1.339
$V_{ABC(\varphi)}$	314.1 V_{phase}	325.5 V_{phase}

4.3. Conclusion

In this chapter, a basic ZSI circuit was designed employing a standard approach and equations discovered in the literature. An LCL filter, which is a better choice over an L or LC-filters in terms of cost and performance, was also designed according to the specification of a ZSI. The SBC, CBC and MBC PWM control techniques were then designed using the basic tools of digital systems such as truth tables, sum-of-products (SOP), karnaugh maps, etc. These control technics were then applied to a previously designed ZSI circuit and the results were captured for and each analysed for each control circuit.

Tables 4.6, 4.8 and 4.11 show a comparison of theoretical results and simulated results for an SBC, CBC and MBC control technique respectively. None of all the compared parameters shows an error of more than 4% between simulated and theoretical value. This implies a successful design a ZSI and the control circuits of all three PWM control techniques and a reliable reference for a proposed CB-ZSI topology in chapter 5 (as stipulated by the performance criteria in chapter 3).

5. PROPOSED THREE-PHASE CAPACITOR BOOSTED-Z-SOURCE INVERTER(CB-ZSI) TOPOLOGY

The purpose of this chapter is to propose a different of a Z-source inverter termed a Capacitor Boosted-Z-Source Inverter (CB-ZSI). The naming of this proposed inverter is motivated by the fact that the change is done on the z-impedance of the traditional inverter by adding two capacitors shut to the original impedance inductors thus improving the boosting capability of an inverter. The addition of two shunt capacitors C_{p1} and C_{p2} to inductors L_1 and L_2 respectively (topological amendment), has proven to alter the response of the traditional Z-source inverter when the previously developed PWM control techniques in chapter 4 (SBC, CBC and MBC) are applied to a CB-ZSI. In this chapter, a CB-ZSI is developed and compared to a ZSI to performance.

Injection of the ninth harmonic signal to the fundamental reference waveform (PWM control technique amendment), termed the ninth harmonic injection (NHI), was investigated but proven to be to worsen the performance of both the ZSI and CB-ZSI. Even though the boost factor is improved, however; %THD, voltage stress across switching devices as well as the voltage ripples at DC-link voltage increase drastically. As a results, this PWM control technique is not investigated any further in this research study.

This chapter begins with a brief comparison of results for SBC, CBC and MBC applied to a ZSI presented in chapter 4. This is to put references of comparison in place for the above stated proposition (CB-ZSI) to be able to judge it on whether it show better or worse performance relative to what we already have in literature (ZSI).

5.1. Comparison of SBC, CBC and MBC critical parameters for a ZSI

It should the noted that all critical parameters (except %THD) presented in table 4.2, 4.5, 4.7 and 4.10 are direct functions of modulation index (m) and boost factor (B). Therefore; this section will focus mainly on these two parameters, and with reference to relevant equations developed in chapter 2, one can extrapolate the effect on other critical parameter other than m and B. Refer to figure 5.1 and 5.2 below:

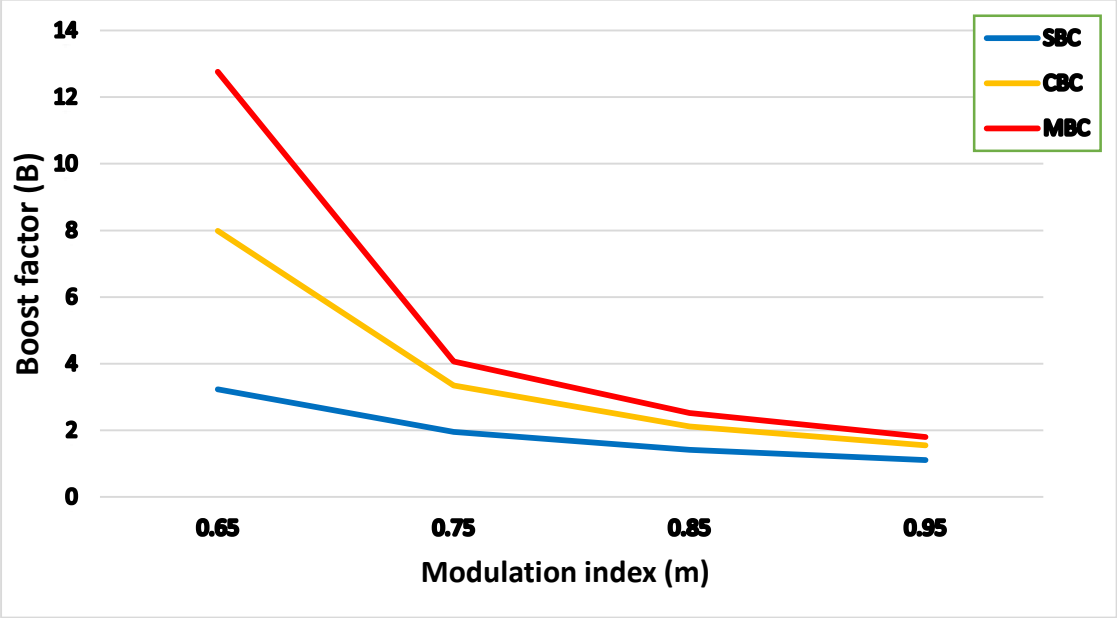


Figure 4.54: Boost factor vs modulation index (SBC, CBC and MBC)

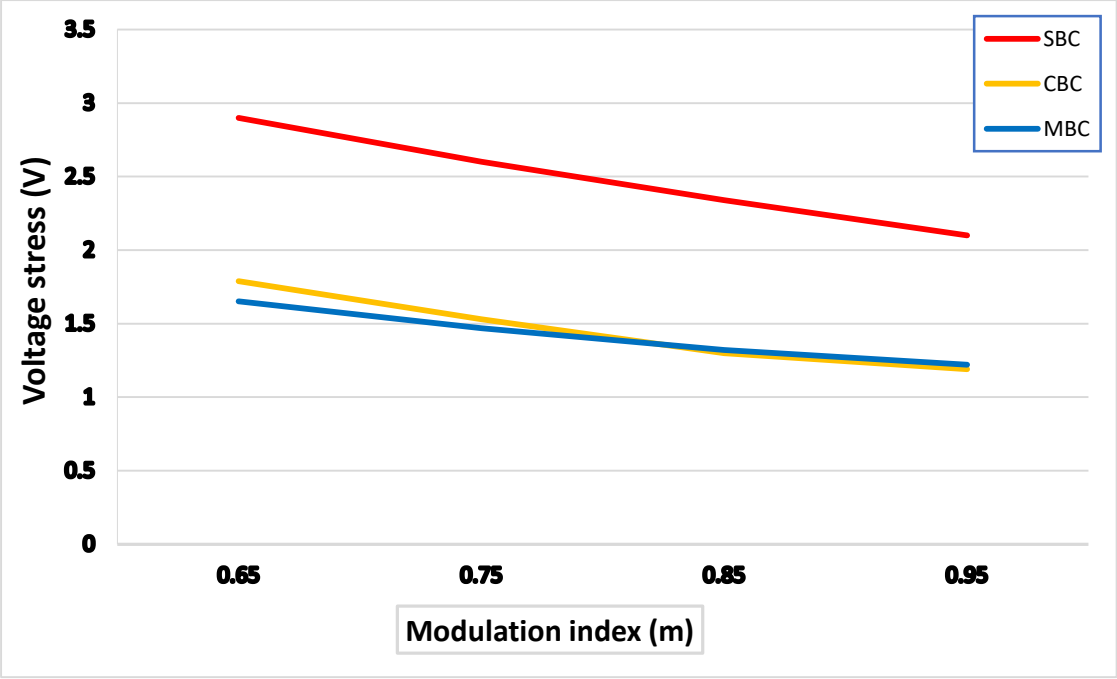


Figure 4.55: Voltage stress vs modulation index (SBC, CBC and MBC)

Figure 5.1 shows the relationship between the boost factor and modulation index. Generally; increasing modulation index decreases the boost factor across all three PWM control techniques. However; MBC exhibit the highest while SBC exhibit the lowest boost factor for any given modulation index, CBC is sandwiched in between the two extremums. This is supported by (4.37), (4.39) and (4.52). There are different acceptable ranges for B_{SBC}, B_{CBC} and B_{MBC}, however; for comparison between these PWM control techniques, a common modulation index range for

which all three boost factors are defined is selected (refer to (5.1)). Therefore, figure 5.1 states that:

$$\frac{1}{2m-1} < \frac{1}{\sqrt{3}m-1} < \frac{\pi}{3\sqrt{3}m-\pi}$$

$$\therefore B_{SBC} < B_{CBC} < B_{MBC} \; where \; 0.605 < m < 1 \qquad 4.53$$

Figure 5.2 shows the relationship between the voltage stress across switching devices and modulation index. Again in general; increasing modulation index decreases the voltage stress across all three PWM control techniques. However; SBC exhibit the highest while MBC exhibit the lowest voltage stress for any given modulation index, CBC is sandwiched in between the two extremums but converges to MBC as the modulation index increases.

5.4. The proposed CB-ZSI development

5.4.1. Circuit analysis on different modes of operation

The CB-ZSI also has three modes of operation just like a traditional ZSI circuit. The modes of operation include six active states, two zero states and a shoot-though which occur in 7 distinct ways. Figure 5.3 shows the block diagram of the proposed CB-ZSI with the inclusion of capacitors C_{p1} and C_{p2} parallel to L_1 and L_2 respectively. C_{p1} and C_{p2} maintains a positive residual voltage across L_1 and L_2 respectively at steady state (which is zero for a ZSI), thus improving the boosting capability of a CB-ZSI. Figure 5.4 and 5.5 show equivalent circuits for the CB-ZSI when operation in a shoot-through and non-shoot-through state respectively.

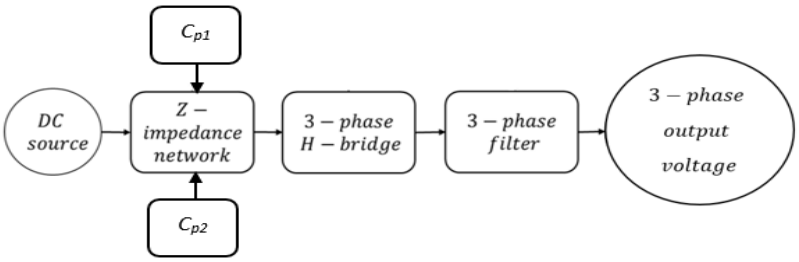


Figure 4.56: The proposed CB-ZSI topology

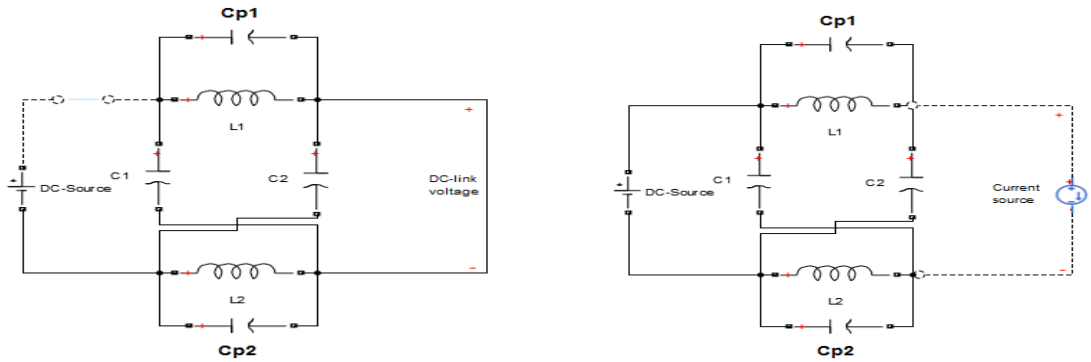


Figure 4.57: Equivalent shoot-through circuit CB-ZSI

Figure 4.58: Equivalent non-shoot-through CB-ZSI

$$V_{C1} = V_{C2} = V_{\mathrm{C}},\ V_{L1} = V_{L2} = V_{\mathrm{L}},\ V_{C\mathrm{p}1} = V_{C\mathrm{p}2} = V_{\mathrm{Cp}} \quad 4.54$$

During a shoot-through state (T_0 interval):

$$V_L = V_C = V_{\mathrm{Cp}}\ ,\ V_{DC-link} = 0 \quad 4.55$$

During a non-shoot-through state (T_1 interval):

$$V_L = V_{\mathrm{Cp}} \neq V_C$$

$$V_L = V_{in} - V_C = V_C - V_{DC-link}$$

$$\therefore \widehat{V_{DC-link}} = V_C - V_L = 2V_C - V_{in} \quad 4.56$$

For a traditional ZSI, the average inductor voltage across inductors L_1 and L_2 is zero at steady state. However; for the CB-ZSI, average inductor voltage across inductors L_1 and L_2 is no longer zero. This is simple because of the shunt capacitors C_{p1} and C_{p2} parallel to the inductors L_1 and L_2 respectively. These capacitors maintain a potential difference which tends to be negative with respect to V_{in} across the inductors (refer to figure 5.4 and 5.5).

Average inductor voltage-time product ($T = T_1 + T_0$ interval):

$$\overline{V_L} \times \mathrm{T} = V_C \times \mathrm{T}_0 + (V_{in} - V_C) \times \mathrm{T}_1 = \overline{V_{Cp}} \times T \quad 4.57$$

$$\text{Let } \overline{V_{Cp}} = V_a \times \mathrm{T}_0 + V_b \times \mathrm{T}_1 \quad 4.58$$

$$\text{where } V_a = \mathrm{k}_a V_C, V_b = \mathrm{k}_b V_C, \mathrm{k_a}, \mathrm{k_b} - \text{proportional factors (\%)} \quad 4.59$$

$$\therefore V_C \times \mathrm{T}_0 + (V_{in} - V_C) \times \mathrm{T}_1 = -(\mathrm{k}_a V_C \times \mathrm{T}_0 + \mathrm{k}_b V_C \times \mathrm{T}_1)$$

$$\frac{V_C}{V_{in}} = \frac{T_1}{(1-k_b)T_1 - (1+k_a)T_0} \quad 4.60$$

It should be noted that period remains constant and exclusively independent of k_a and k_b. These two constant factors only affect a duty-ratio of the diode's switching action, a duty-ratio of the voltage waveform across inductors L_1 and L_2, capacitors C_1 and C_2 steady state voltage as well as the DC-link voltage. Therefore:

$$\mathrm{T} = (1-k_b)T_1 + (1+k_a)T_0 \text{ , constant for different } \mathrm{k_a}, \mathrm{k_b} \text{ sets} \quad 4.61$$

$$\therefore k_a \times T_0 = k_b \times T_1$$

$$\frac{T_0}{T_1} = \frac{k_b}{k_a}\ , k_a \gg k_b \quad 4.62$$

Average and peak DC-link voltage-time product (T = T_1 + T_0 interval):

$$\overline{V_{DC-link}} \times T = V_C \times T, \text{ at steady state} \quad (4.63)$$

$$\therefore \widehat{V_{DC-link}} = 2V_C - V_{in}$$

$$\widehat{V_{DC-link}} = \frac{2T_1}{(1-k_b)T_1 - (1+k_a)T_0} \times V_{in} - V_{in}$$

$$\widehat{V_{DC-link}} = \frac{2T_1 - (1-k_b)T_1 + (1+k_a)T_0}{(1-k_b)T_1 - (1+k_a)T_0} \times V_{in}$$

$T_1 \approx (1-k_b)T_1$, for small k_b values

$$\therefore \frac{\widehat{V_{DC-link}}}{V_{in}} = \frac{(1-k_b)T_1 + (1+k_a)T_0}{(1-k_b)T_1 - (1+k_a)T_0} = \frac{T}{(1-k_b)T_1 - (1+k_a)T_0}$$

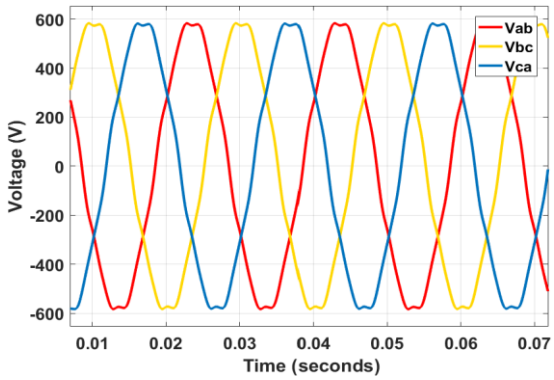
$$\frac{\widehat{V_{DC-link}}}{V_{in}} = \frac{T}{(1-k_b)T_1 + (1+k_a)T_0 - 2(1+k_a)T_0}$$

$$\therefore \frac{\boldsymbol{\widehat{V_{DC-link}}}}{\boldsymbol{V_{in}}} = \boldsymbol{B} = \frac{\mathbf{1}}{\mathbf{1-2(1+k_a)D_0}}, \boldsymbol{k_a \neq \frac{2D_0+1}{2D_0}} \quad (4.64)$$

5.4.2. Results and analysis

(5.8) suggests that with the inclusion of shunt capacitors C_{p1} and C_{p2} the switching duty-ratio of the impedance network of a CB-ZSI changes in a sense that it increases, however; the switching frequency remain unchanged (same to that of the ZSI) as stated by (5.9). (5.12) shows that for a CB-ZSI a shoot-through duty ratio is increased by a factor k_a hence increasing a boost factor relative to that of ZSI for the same modulation index.

k_a and k_b are factor that are functions of shunt capacitors C_{p1} and C_{p2} as well as the initial shoot-through duty ratio of the traditional ZSI before applying the modification to CB-ZSI. In this investigation, C_{p1} and C_{p2} chosen to be 1% and 2% of C_1 and C_2 at two different cases and the results are captured and analysed.



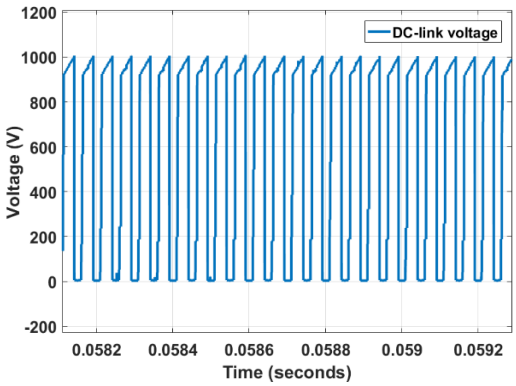


Figure 4.59: Filtered phase voltage for SBC(CB-ZSI,C_p=1%)

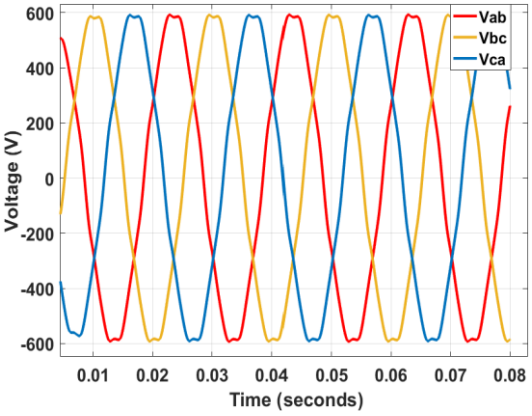


Figure 4.60: DC-link voltage for SBC(CB-ZSI, C_p=1%)

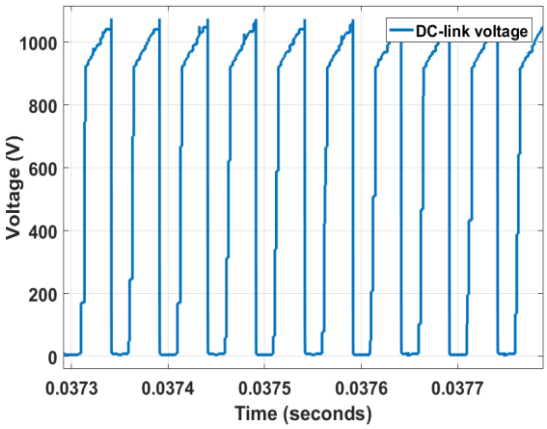


Figure 4.61: Filtered phase voltage for SBC (, C_p=2%)

Figure 4.62: DC-link voltage for SBC (CB-ZSI, C_p=2%)

Figure 5.6 to 5.9 are sample results taken for input voltage equal to 200.0 V and a modulation index of 0.65. These results generally conform with the prediction of (5.12). Figure 5.6 - 5.7 and figure 5.8 - 5.9 show filtered line output voltage and DC-link voltage for shunt capacitance of 1 and 2% respectively, when SBC is applied to a CB-ZSI. Output line voltage and DC-link voltage of a ZSI are 580.0V (peak) and 1000V (peak) respectively at shunt capacitance of 1%; 596.0V (peak) and a 1080V (peak) at shunt capacitance of 2% respectively. The two parameters have a higher reading in a CB-ZSI compared to a ZSI, refer to table 4.5 ($V_{ac3\varphi}$ = 375.0V (peak), $V_{DC\text{-}link}$ = 644.8V (peak).

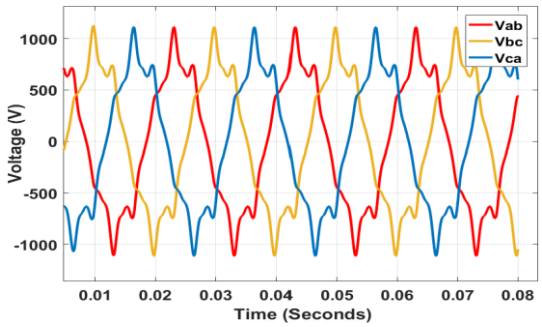


Figure 4.63: Filtered phase voltage for CBC(CB-ZSI, C_p=1%)

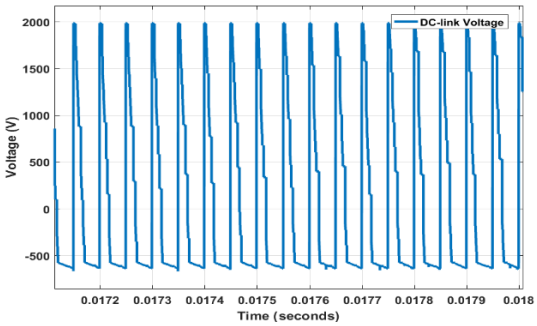
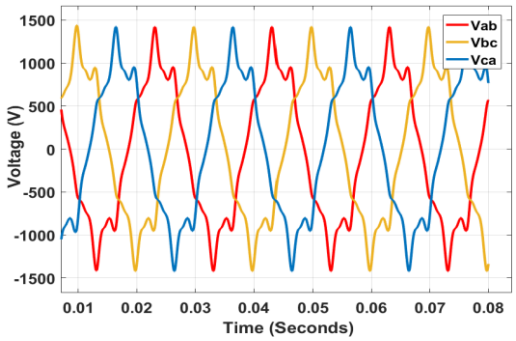


Figure 4.64: DC-link voltage for CBC(CB-ZSI, C_p=1%)



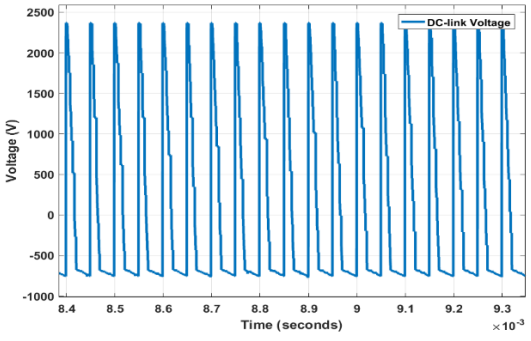


Figure 4.65: Filtered phase voltage for CBC(CB-ZSI, C_p=2%)

Figure 4.66: DC-link voltage for CBC(CB-ZSI, C_p=2%)

Figure 5.10 to 5.13 are sample results taken for input voltage equal to 200 V and a modulation index of 0.65. These results also generally conform with the prediction of (5.12). Figure 5.10 - 5.11 and figure 5.12 - 5.13 show filtered line output voltage and DC-link voltage for shunt capacitance of 1 and 2% respectively, when MBC is applied to a CB-ZSI. Output line voltage and DC-link voltage of a ZSI are 1120V (peak) and 2004V (peak) respectively at shunt capacitance of 1%; 1485V (peak) and a 2370V (peak) at shunt capacitance of 2% respectively. The two parameters have a hire reading in a CB-ZSI compared to a ZSI, refer to table 4.5 ($V_{ac3\varphi}$ = 888.0V (peak), $V_{DC\text{-}link}$ = 1590V (peak).

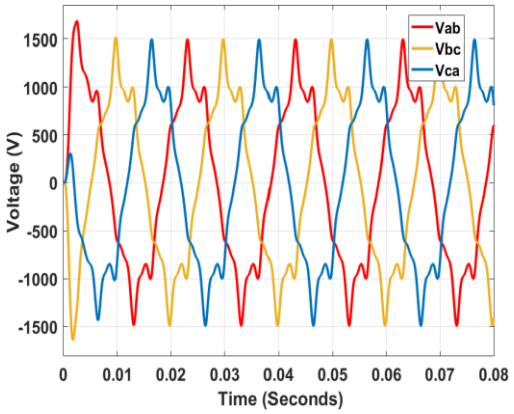


Figure 4.67: Filtered phase voltage for MBC(CB-ZSI, C_p=1%)

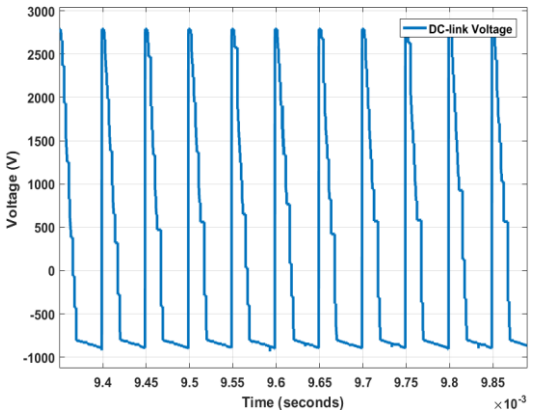


Figure 4.68: DC-link voltage for MBC(CB-ZSI, C_p=1%)

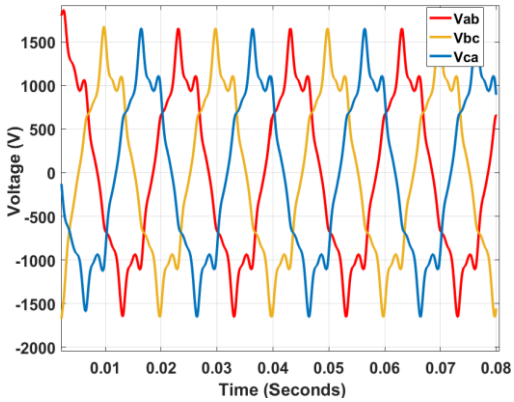


Figure 4.69: Filtered phase voltage for MBC(CB-ZSI, C_p=2%)

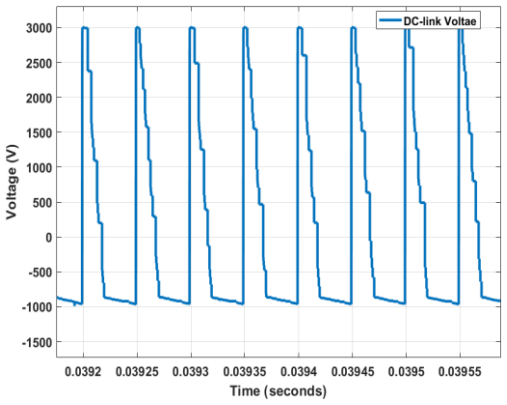


Figure 4.70: DC-link voltage for MBC(CB-ZSI, C_p=2%)

Figure 5.10 to 5.13 are sample results taken for input voltage equal to 200 V and a modulation index of 0.65. These results also generally conform with the prediction of (5.12). Figure 5.10 - 5.11 and figure 5.12 - 5.13 show filtered line output voltage and DC-link voltage for shunt

capacitance of 1 and 2% respectively, when MBC is applied to a CB-ZSI. Output line voltage and DC-link voltage of a ZSI are 1500V (peak) and 2800V (peak) respectively at shunt capacitance of 1%; 1630V (peak) and a 3000V (peak) at shunt capacitance of 2% respectively. The two parameters have a hire reading in a CB-ZSI compared to a ZSI, refer to table 4.5 ($V_{ac3\varphi}$ = 1465V (peak), $V_{DC\text{-}link}$ = 2601V (peak).

Two main facts can be concluded from figure 5.6 to 5.17. Firstly, a CB-ZSI shows an increase in the boost factor with increase in shunt capacitance (because of increase in DC-link voltage) compared to a ZSI for the same input voltage and modulation index; secondly, increasing the shunt capacitance increases a gain factor of a CB-ZSI compared to a ZSI for the same input voltage and modulation index. The above stated facts hold across all three PWM control techniques, viz. SBC, CBC and MBC. The rest of the detailed results are populated in table 5.1 – 5.4.

Table 5.4 compares filtered line output voltage and DC-link voltage of CB-ZSI at shunt capacitance of 1 and 2% to those of a ZSI (shunt capacitance at 0%) when SBC, CBC and MBC are applied to both topologies with V_{in} being 200V and a modulation index of 0.65. Table 5.1 – 5.3 show responses of other critical parameters in a CB-ZSI in response to change in modulation index and/or input voltage when the shunt capacitance is kept constant (at 0%, 1%, and 2% respectively) with PWM technique being SBC, CBC and MBC per case.

Table 4.12: Summary of SBC mode results (CB-ZSI)

Varying input voltage and modulation (C_p = 1% of C_1)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	1009	1512	2017	2520	608.1	912.9	1217	1520
4	$V_{AC(3\varphi)}$	573.6	862.1	1149	1438	393.3	590.8	788.0	986.0
5	$Stress-ratio$	1.759	1.754	1.755	1.753	1.546	1.545	1.544	1.542
6	B	5.045	5.040	5.043	5.040	3.041	3.043	3.043	3.040
7	mB	3.280	3.276	3.278	3.276	2.281	2.282	2.282	2.280
8	%THD	3.120	3.120	3.120	3.120	2.540	2.550	2.540	2.540
Table 5.1 continues below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	432.0	648.2	863.0	1080	341.0	511.5	681.0	851.1
4	$V_{AC(3\varphi)}$	305.5	459.3	612.6	765.5	243.9	366.5	488.8	611.0
5	$Stress-ratio$	1.414	1.412	1.409	1.411	1.398	1.396	1.393	1.393
6	B	2.160	2.161	2.158	2.160	1.705	1.705	1.703	1.702

7	mB	1.836	1.837	1.834	1.836	1.620	1.620	1.617	1.617
8	%THD	1.820	1.810	1.810	1.810	0.800	0.880	0.800	0.810

Table 4.13: Summary of CBC mode results (CB-ZSI)

Varying input voltage and modulation (C_p = 1% of C_1)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	2000	3040	4040	5050	842.8	1281	1702.4	2128
4	$V_{AC(3\varphi)}$	1118	1795	2382	2981	471.1	756.4	1004	1256
5	$Stress-ratio$	1.695	1.694	1.696	1.694	1.299	1.308	1.309	1.298
6	B	10.00	10.13	10.10	10.10	4.214	4.280	4.256	4.256
7	mB	6.500	6.590	6.565	6.565	3.161	3.210	3.192	3.192
8	%THD	2.07	2.070	2.070	2.070	1.920	1.920	1.920	1.920
Table 5.2 continues below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	520.5	791.1	1051	1314	389.8	593.1	787.9	985.1
4	$V_{AC(3\varphi)}$	332.0	490.1	650.3	803.0	260.2	391.0	521.2	650.0
5	$Stress-ratio$	1.248	1.252	1.245	1.260	1.140	1.144	1.137	1.151
6	B	2.603	2.637	2.628	2.628	1.949	1.997	1.970	1.970
7	mB	2.210	2.241	2.233	2.234	1.852	1.878	1.871	1.871
8	%THD	1.383	1.383	1.383	1.383	1.383	1.383	1.383	1.383

Table 4.14: Summary of MBC mode results (CB-ZSI)

Varying input voltage and modulation (C_p = 1% of C_1)									
1	m	0.650	0.650	0.650	0.650	0.750	0.750	0.750	0.750
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	2800	4205	5590	6989	1350	2030	2670	3340
4	$V_{AC(3\varphi)}$	1500	2243	3000	3732.5	786.0	1180	1575	1970
5	$Stress-ratio$	1.867	1.874	1.863	1.794	1.718	.1.720	1.695	1.695
6	B	14.00	14.02	13.98	13.98	6.750	6.767	6.675	6.680
7	mB	9.100	9.111	9.084	9.084	5.063	5.075	5.006	5.010
8	%THD	31.41	31.41	31.41	31.41	11.98	11.98	11.98	11.98
Table 5.3 continues below									
1	m	0.850	0.850	0.850	0.850	0.950	0.950	0.950	0.950
2	V_{IN}	200.0	300.0	400.0	500.0	200.0	300.0	400.0	500.0
3	V_{DClink}	820.0	1225	1635	2047	590.0	887.0	1183	1480
4	$V_{AC(3\varphi)}$	541.0	812.5	1084	1356	424.8	638.0	850.0	1065

5	Stress – ratio	1.516	1.508	1.508	1.510	1.389	1.390	1.392	1.390
6	B	4.100	4.083	4.088	4.094	2.950	2.956	2.955	2.960
7	mB	3.485	3.471	3.474	3.480	2.803	2.808	2.807	2.812
8	%THD	9.390	9.390	9.390	9.390	9.160	9.160	9.160	9.160

Table 4.15: ZSI vs CB-ZSI (C_p = 1 and 2%) at SBC, CBC and MBC

Parameter	ZSI, SBC	CB-ZSI, SBC, C_p=1%	CB-ZSI, SBC, C_p=2%	ZSI, CBC	CB-ZSI, CBC, C_p=1%	CB-ZSI, CBC, C_p=2%	ZSI, MBC	CB-ZSI, MBC, C_p=1%	CB-ZSI, MBC, C_p=2%
V_{DClink}(V)	644.8	1009	1210	1590	2000	2398	2601	2701	2779
$V_{AC(3\varphi)}$ (V)	216.5	573.6	586.4	888.0	1118	1143	1465	1480	1491
%THD	3.750	3.120	2.760	4.000	2.070	1.87	10.37	31.41	37.32

Table 5.1 – 5.3 show the same relationships between critical parameters in a CB-ZSI that were discovered in table 4.5, 4.7 and 4.10 of a ZSI at SBC, CBC, and MBC respectively, however; with off-sets in this case. Table 5.1, 5.2 and 5.3 verify the prediction of (5.12). They show that inclusion of a shunt capacitance C_p that is 1% of C_1 improves the boost factor of CB-ZSI by more 56% at SBC technique, more than 25% at CBC technique and more than 14% at MBC technique on average. Since the gain factor is a linear function of a boost factor with the proportionality constant being the modulation index, the percentage of improvement of gain factors from ZSI to CB-ZSI remains the same as that of boost factors across SBC, CBC and MBC techniques.

The voltage stress ratio across the switching devices is reduced by more than 40% at MBC technique, more than 5% at CBC control and increased by 1.7% for MBC PWM control technique on average. CB-ZSI also shows improved performance on the %THD for SBC and CBC while it worsens for MBC technique. Figure 5.18 - 5.23 give a graphical comparison between ZSI and CB-ZSI to the boost factor and voltage stress ratio. %THD is reduced by more than 112% for SBC technique, 16.8% for CBC and increased by more than 24% for MBC technique on average.

Table 5.4 shows the response of CB-ZSI at different values of C_p. In this table, the modulation index and input voltage are kept constant at 0.65 and 200V respectively. The table generally shows that the DC-link voltage (and hence all related parameters) and output voltage increases with increase of the shunt capacitance while percentage of total harmonics distortion decrease with increase in shunt capacitance.

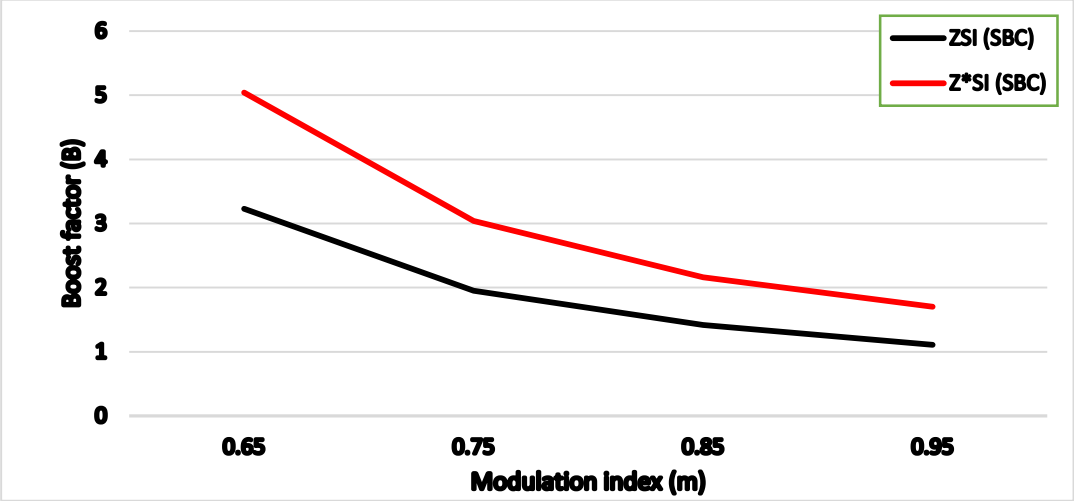


Figure 4.71: Boost factor vs modulation index (ZSI vs CB-ZSI at SBC)

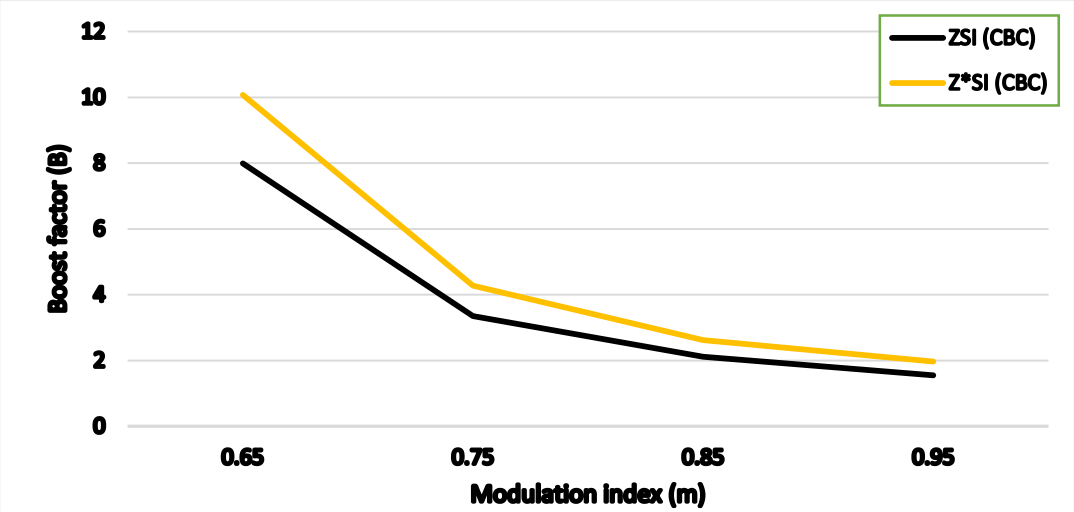


Figure 4.72: Boost factor vs modulation index (ZSI vs CB-ZSI at CBC)

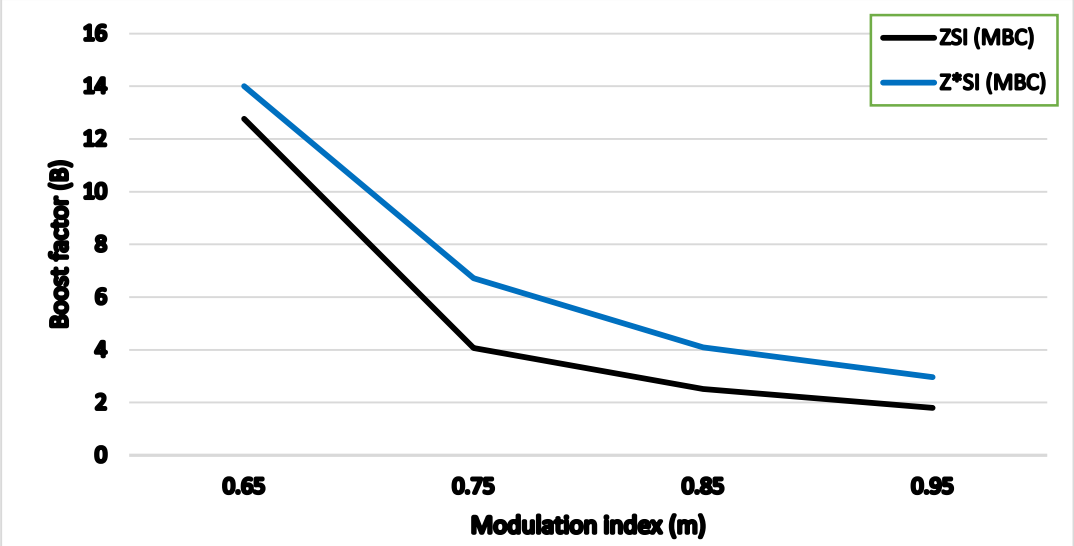


Figure 4.73: Boost factor vs modulation index (ZSI vs CB-ZSI at MBC)

Figure 5.18, 5.19 and 5.20 shows a comparison between boost factors of a ZSI and a CB-ZSI for SBC, CBC and MBC PWM control technique respectively over a range of modulation index. According to (5.12), the boost factor is expected to be higher for a CB-ZSI as compared to a ZSI. As evident in Figure 5.18, 5.19 and 5.20 indeed, the boost factor for a CB-ZSI is always higher than that of a ZSI for a modulation index range specified by (5.1). This holds for all three PWM control techniques investigated in this research study.

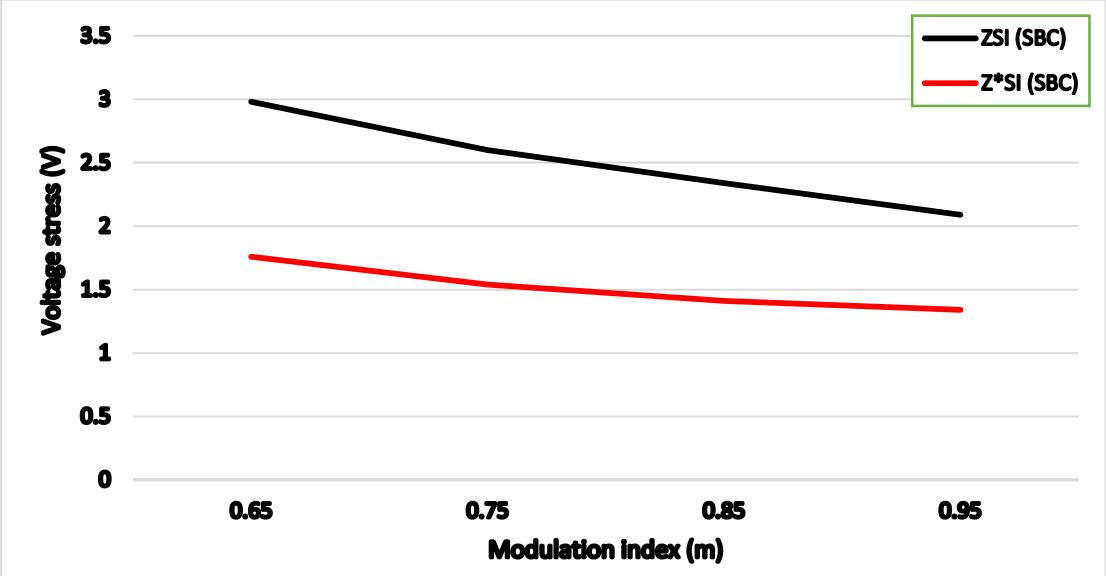


Figure 4.74: Voltage stress vs modulation index (ZSI vs CB-ZSI at SBC)

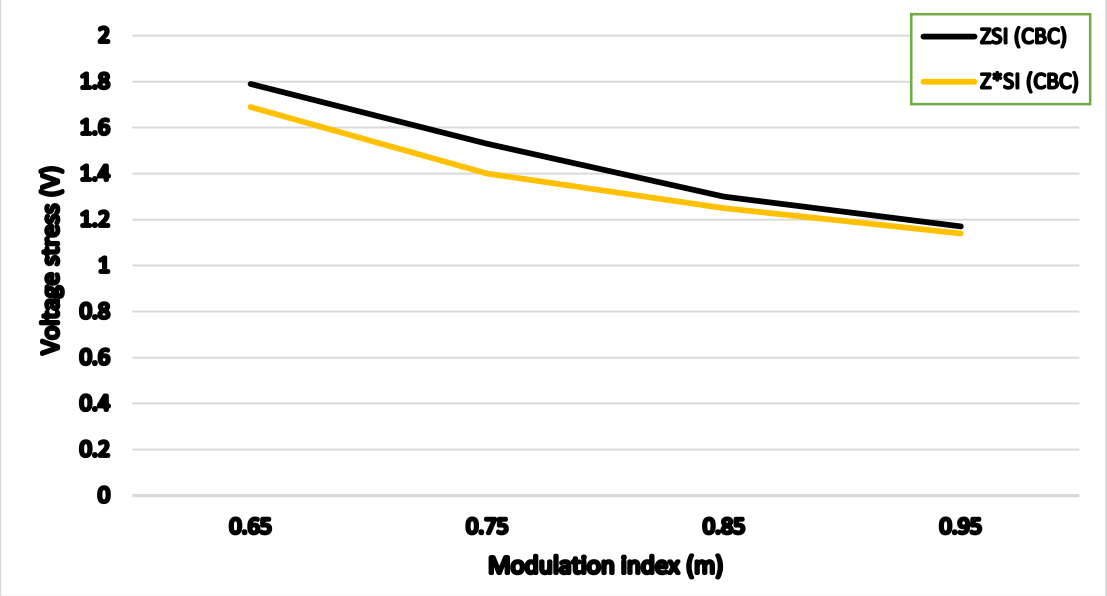


Figure 4.75: Voltage stress vs modulation index (ZSI vs CB-ZSI at CBC)

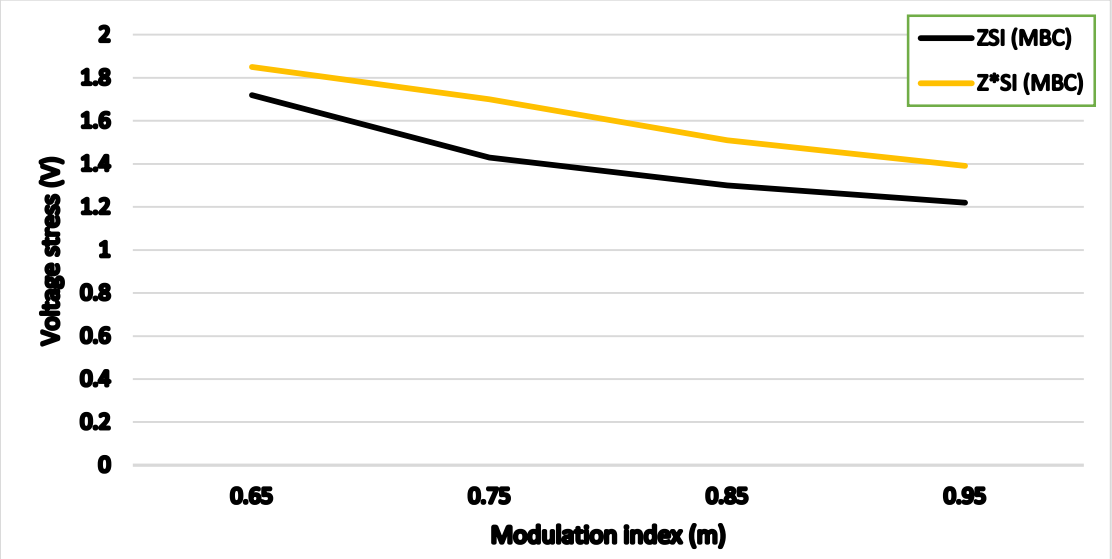


Figure 4.76: Voltage stress vs modulation index (ZSI vs CB-ZSI at MBC)`

Figure 5.21, 5.22 and 5.23 shows a comparison between voltage stresses of a ZSI and a CB-ZSI for SBC, CBC and MBC PWM control technique respectively over a range of modulation index. According to (5.12), the boost factor is expected to be higher for a CB-ZSI as compared to a ZSI for the same modulation index. That implies a lower voltage stress in a CB-ZSI for the same boost factor. As evident in figure 5.21, 5.22 and 5.23 indeed, the voltage stress for a CB-ZSI is always higher than that of a ZSI for a modulation index range specified by (5.1). This holds for all three PWM control techniques investigated in this research study.

5.5. Conclusion

In this chapter, a CB-ZSI was introduced. A mathematical analysis of a CB-ZSI was done which led to the main equation (5.12) which predicted that an inclusion of the shunt capacitances parallel to the inductors of an impedance network would increase a boost factor in CB-ZSI relative to that of a ZSI. This mathematical claim was validated by the simulated results which proved that indeed, a CB-ZSI has a higher boost factor than a classical ZSI for the similar modulation index. The voltage stress for a CB-ZSI is lowered as compared to that of a ZSI for a similar boost factor because a CB-ZSI achieves boost factor similar to that of a ZSI at a much lower modulation index. In general, CB-ZSI shows improved performance relative to a ZSI.

6. CONCLUSION

6.1. Summary and conclusion on the study's objectives

The purpose of this research was to study the behaviour of a ZSI in response to different PWM control technique or rather; the effect of different PWM technique on a ZSI over a range of operation conditions. Furthermore; the knowledge gained from the latter mentioned study was to be carefully utilized to develop an amendment to a classical ZSI in order to improve its response to the PWM control techniques, hence improving power quality of the proposed topology. The proposed topology was termed a Capacitor Boosted-Z-Source Inverter (CB-ZSI) which was formed by inserting shunt capacitors C_{p1} and C_{p2} parallel to L_1 and L_2 respectively.

Three most common PWM control techniques [1], [3], [6], [7], [9], [12], [13] [18], [23] viz. a simple boost control, constant boost control and a maximum boost control PWM technique; were designed and applied to a ZSI. A couple of relationships identified when results were captured in table 4.5, 4.7 and 4.10 for SBC, CBC and MBC technique respectively. The voltage stress across the switching devices, the boost factor (and hence the gain factor) as well as the percentage of total harmonics distortion were exclusively independent of the modulation index and all decrease with the increase in the modulation index. The output voltage as well as the DC-link voltage was dependent on both the input voltage and modulation index. Both the output voltage and the DC-link voltage increase with the increase in either the input voltage or the modulation index; the opposite was also true. The above stated relationships held for all three PWM control techniques however; a proportional offset existed between the results of the three PWM control techniques.

MBC exhibited the highest while SBC exhibited the lowest boost factor for any given modulation index in a range stipulated by (5.1), CBC is sandwiched in between the two extremums. SBC exhibit the highest while MBC exhibit the lowest voltage stress for any given modulation index stipulated by (5.1), CBC is sandwiched in between the two extremums but converges to MBC as the modulation index increases.

Similar relationships to those of ZSI's critical parameters hold for a CB-ZSI, however; the distinction between the two topologies was a relative shift between each and every performance parameter. A CB-ZSI has a higher boost factor (and also a DC-link voltage) than that of a ZSI for any modulation index stipulated by (5.1) across all three different PWM techniques. A CB-ZSI has a lower voltage stress (and also a DC-link voltage) than that of a ZSI for any modulation index stipulated by (5.1) across all three different PWM techniques. A CB-ZSI does not incur adverse changes to the percentage of total harmonic distortions for a SBC and a CBC PWM control method because they remain within the boundary of South African national grid standard

of less than 5% as stipulated by SANS 10142 [5]. However; for a MBC PWM control method, the %THD increase drastically.

Therefore, the main objective of this of this research study was achieved even though more work still need to be done to aid the understanding of the operation of a CB-ZSI and mark its limitations. The boost factor of CB-ZSI was by more 56% at SBC technique, more than 25% at CBC technique and more than 14% at MBC technique on average. Since the gain factor is a linear function of a boost factor with the proportionality constant being the modulation index, the percentage of improvement of gain factors from ZSI to CB-ZSI remains the same as that of boost factors across SBC, CBC and MBC techniques. The voltage stress ratio across the switching devices of a CB-ZSI was reduced by more than 40% at MBC technique, more than 5% at CBC control and increased by 1.7% for MBC PWM control technique on average. %THD for CB-ZSI was reduced by more than 112% for SBC technique, 16.8% for CBC and increased by more than 24% for MBC technique on average.

The above stated figures implies an improved power quality on a CB-ZSI and improved reliability since a CB-ZSI can achieve results without incurring much pressure of the components as it would be for a classical ZSI. This also implies cost reduction when designing a CB-ZSI since a stress that power switching component have to withstand is reduced. There will also be less capacitance and inductive requirement for a CB-Z-impedance network because the whole DB-ZSI does not require a longer shoot-through time interval to achieve large boost factors. Filter passive components' requirements for a CB-ZSI will also decrease for an SBC and CBC technique since the %THD is reduced and will increase for MBC technique for which %THD is increased.

6.2. Future work considerations

More insight is required on the operation of a CB-ZSI. To build on top of the work of this research study, a formula that define the shunt capacitance C_p and correlate it to a specified amount of boost it incurs in a CB-ZSI still needs to be established. The limits of C_p also need to be established. As Cp approaches zero, a CB-ZSI converges to an ZSI; What happens Cp approaches infinity?

The proportional factors k_a and k_b still need to be unpacked. A formula for these factors of a characteristic table which shows ka and kb values for different values of Cp still need to be established to aid easy circuit design of a CB-ZSI.

7. REFERENCES

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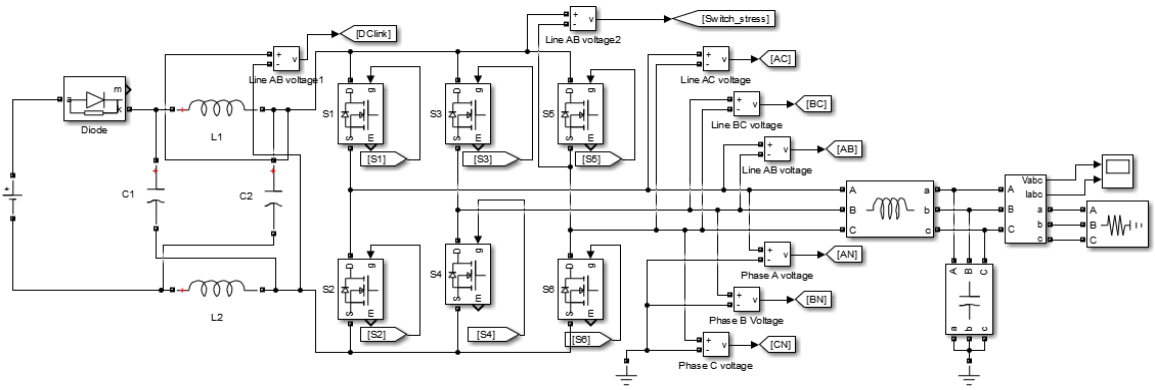
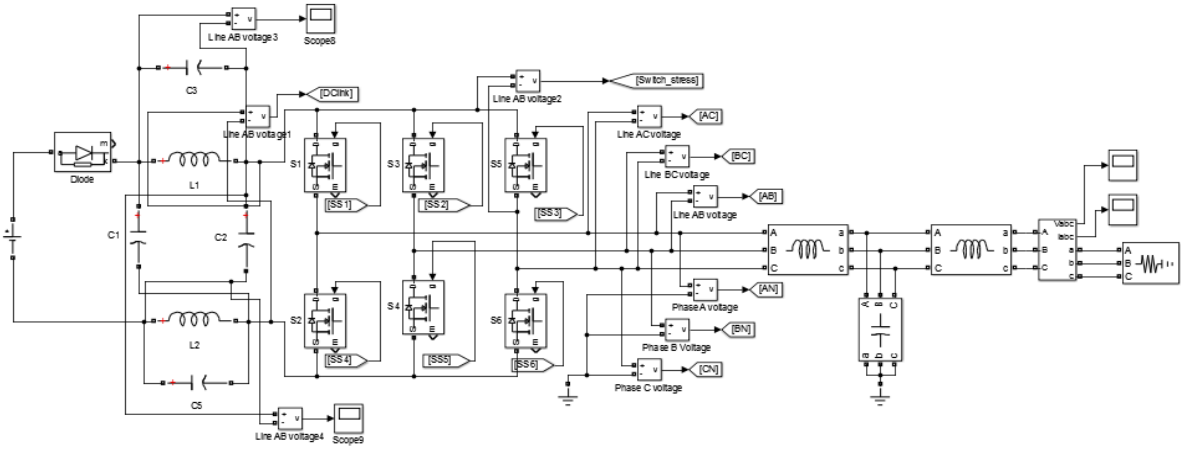
8. APPENDICES

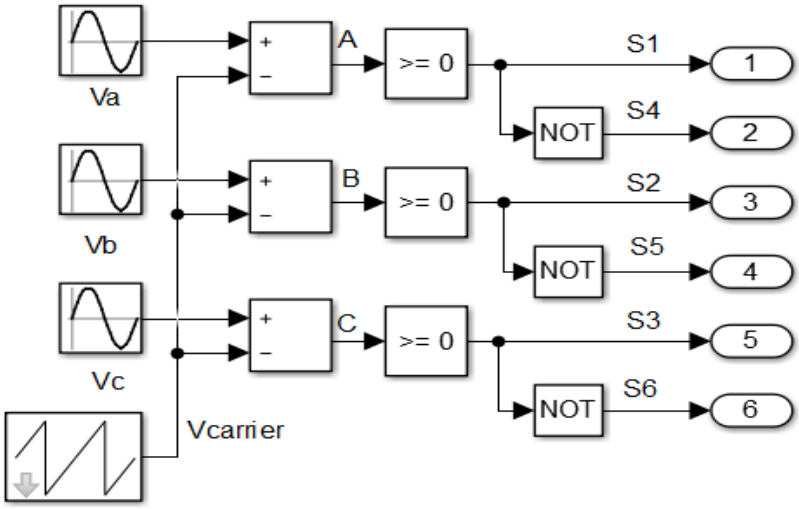
A1. A ZSI circuit (SIMULINK model)



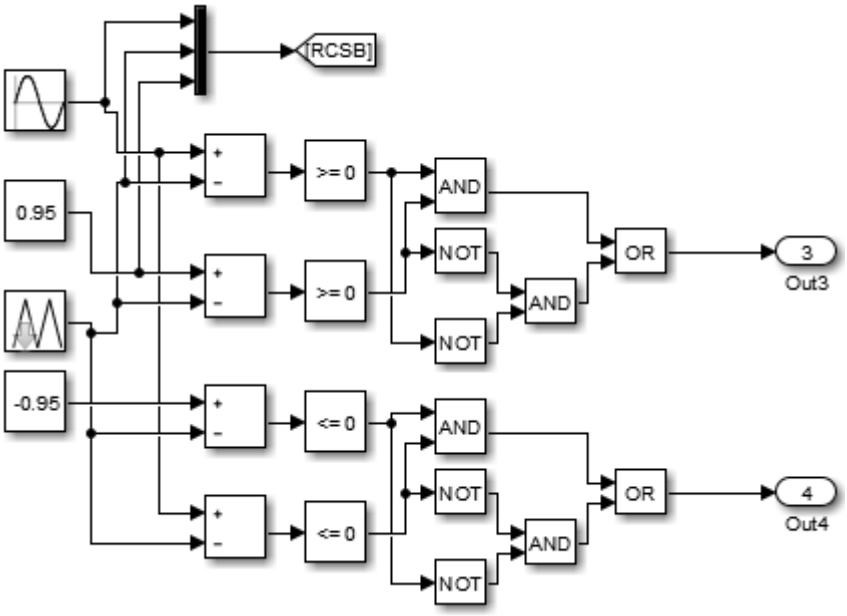
A2. A CB-ZSI circuit (SIMULINK model)



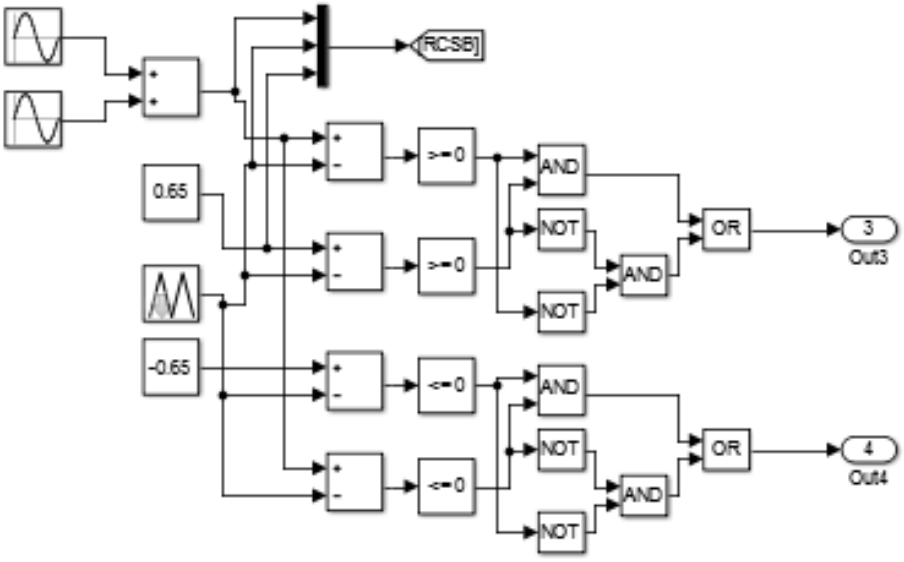
A3. Sine-PWM control technique SIMULINK model



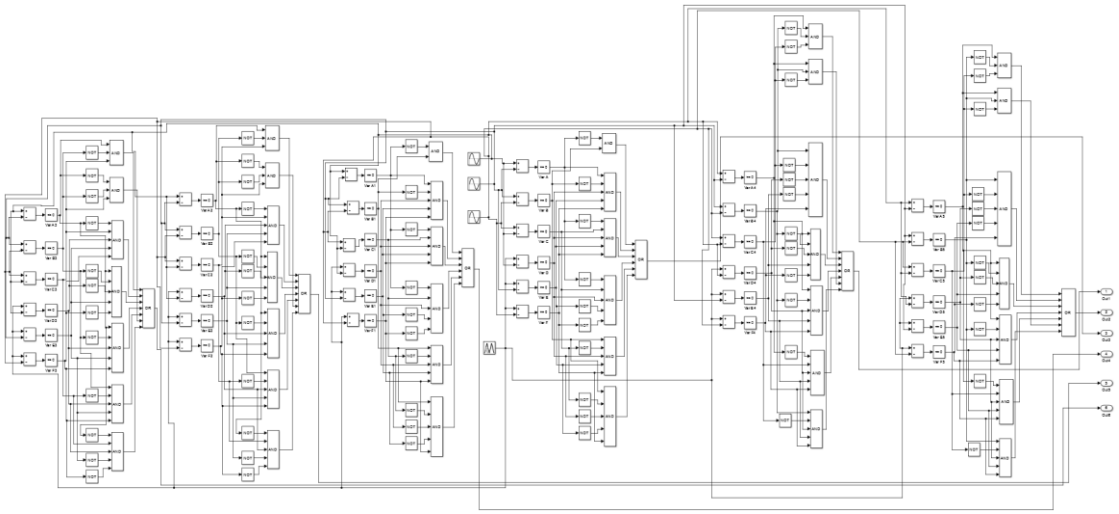
A4. Simple boost PWM control technique SIMULINK model (per phase diagram)



A5. Constant boost PWM control technique SIMULINK model (per phase diagram)



A6. Maximum boost PWM control technique SIMULINK model



A6. Whole design SIMULINK model