TRAVELLING-WAVE FREQUENCY CONVERSION

by

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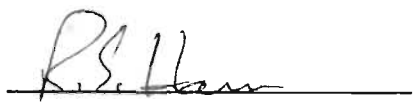
PREFACE

The experimental and theoretical research described in this thesis was carried out by the author in the Electronic Engineering Department of the University of Natal at Durban during the period January 1983 to November 1985 under the supervision of Professor H.L. Nattrass, Head of Department.

These studies represent original work by the author and have not been submitted in any form to another University for any degree. Where use was made of work carried out by others, it has been duly acknowledged in the text.

Signed 

Date 10 Dec 1985

Dedication

To my children, Matthew and Sharon

ACKNOWLEDGMENTS

The author would like to thank the many people who have had an influence on the completion of this thesis, in particular the following:

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ABSTRACT

TRAVELLING-WAVE FREQUENCY CONVERSION

Travelling-wave distributed amplifiers are providing gain over broad frequency ranges for microwave applications. Similar concepts are applicable to distributed mixers and, with the use of controlled feedback, to a multifunction component simultaneously emulating a mixer, amplifier and an oscillator. The concept of this new travelling-wave frequency converter is introduced and data for a discrete component test circuit is presented. To facilitate the converter operation a new three-port travelling-wave mixer is introduced and characterized. Four-port scattering and wave scattering transformations are derived as a method of analysis of the four-port distributed structure. This enables sequential circuit analysis on a small computer.

Practical applications unique to the advanced automatic network analyser, including time domain measurements, are presented to characterize test circuits as well as to develop ancillary equipment such as a transistor test fixture. Automated error corrected transistor measurements and de-embedding are also discussed.

A piecewise linear quantum mechanical method of modelling the conduction channel of a short gate field effect transistor is given to aid the extrapolation of the distributed frequency converter concept to submicron and heterojunction structures.

TABLE OF CONTENTS

LIST OF SYMBOLS AND ABBREVIATIONS

C	Capacitance (Farad)
C_n	Wave scattering matrix of element n
C_{nm}	Element nm of wave scattering matrix
C_T	Total wave scattering matrix
d	Drain
dB	Decibel 10 $\log_{10}$ (power ratio)
dBm	Decibel relative to one milliwatt
ds	Drain-to-Source
e	Amplitude of time variant voltage
E	Voltage
f	Frequency (Hertz)
F	Farad (capacitance)
f_n	Normalized frequency
F_n	Filter (frequency)
FET	Field effect transistor
g	Gate
G	Giga - (multiply by 10^9)
g_m	Transconductance (Siemans)

G_m	Transconductance of element m
gs	Gate-to-Source
h	Planck's constant/2π
H	Henry (inductance)
Hz	Hertz (cycle per second)
i	Current (ampere)
I	Current (ampere)
if, IF	Intermediate frequency
k_n	Mathematical expansion coefficient
l	Loss, voltage ratio
L	Inductance (Henry)
lo, LO	Local oscillator
m	Mass
M	Mega - (multiply by 10^6)
MESFET	Metal Semiconductor FET
PIN	P-intrinsic-N diode
R	Resistance (Ohm)
rf, RF	Radio frequency
s	Laplace operator

S_n	Scattering matrix of element n
S_{nm}	Element nm of scattering matrix
S_T	Total scattering matrix
t	Time (seconds)
v	Time variant voltage
V	Voltage
Z	Impedance
Z_{nm}	Transimpedance
γ	Complex voltage transfer function
Δ	Determinant of a matrix
θ	Phase shift (radians or degrees)
π	Pi (3.14159)
Ψ	Solution to Schrodinger wave equation
ω	Radian frequency (radians/second)
ω_n	Normalized radian frequency
Ω	Ohm (resistance)

CHAPTER 1

INTRODUCTION

This thesis represents a contribution by the author to the design of monolithic microwave integrated circuit functions and reports on the original research leading to the design and implementation of two unique system components. The first component is a three-port travelling-wave mixer, providing separate inputs for the signal and local oscillator. The concept enables a travelling-wave/distributed* amplifier to be operated simultaneously as an amplifier, mixer and oscillator without a significant increase in semiconductor substrate area or circuit complexity. This is done by considering the travelling-wave amplifier as a four-port device and is an extension of the author's work on monolithic receiver front ends for which a patent was received in 1976 (Appendix A, reference claim two). This second device is a TRAVelling-wave Frequency convERTER or a TRAVFERTER.

Travelling-wave amplifiers are inherently broadband devices. Developed in 1936 by Percival [1], the concept was analysed in considerable depth in 1948 [2]. Experimental results were reported in 1950 [3] and it has been utilised to twenty Gigahertz [4-6] in the form of gallium arsenide monolithic microwave integrated circuits (MMIC's) using metal semiconductor field effect transistors (MESFET's). Extensive analysis and test results of distributed amplifiers are contained in the literature [7-13] and one recent paper applies the theory to a two-port travelling-wave broadband mixer [14].

A fundamental advantage of travelling-wave amplifiers over various other broadband gain circuits is the topography that lends itself to integrated circuit implementation. With the maturation of gallium arsenide technology, circuit functions are required that can be used in many applications as system building blocks yet require as little area as possible on the GaAs wafer to optimise the cost per function.

*Little distinction is presently made between travelling-wave and distributed; therefore, these terms will be used interchangeably throughout this thesis.

Monolithic integration of an entire receiver front end by the author in 1976 [15] demonstrated the minimal level of integration necessary to reduce the costs of both production and custom systems. The same concept must now be applied to GaAs MMIC's to meet the performance and cost demands of higher frequency systems.

Extension of the travelling-wave amplifier and mixer theory into simultaneous realisation with controlled level oscillation yields an integratable microwave receiver front end (frequency converter). This front end is capable of very large instantaneous tuning bandwidth (limited primarily by external tuning components) and requires little more GaAs wafer area than a travelling-wave MESFET amplifier alone.

Two-port scattering parameter technique for circuit characterisation and analysis is extended by the author to four-port applications in the thesis. The four-port matrix more completely describes the travelling-wave amplifier. The four-port scattering matrix to wave scattering matrix transformations are derived. This enables circuit analysis of the four-port distributed structure on small computers without resorting to nodal analysis.

Numerous practical applications of the modern automatic network analyser were found. This includes application of time domain analysis to the optimisation of broadband circuits and the automatic measurement of error corrected data under computer control with software de-embedding.

A formalism that can potentially facilitate the modelling of submicron and heterojunction material structures by direct piecewise linear potential barriers is introduced by the author as a viable method for predicting new device performance. The concept suggests implementation of integrated functions as opposed to integrated circuits. A method is presented for the numerical solution of Schrodinger's equation for complex barriers in one dimension.

CHAPTER 2

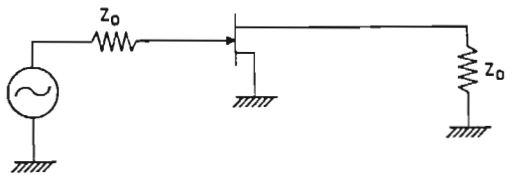
TRAVELLING-WAVE MESFET CIRCUIT FUNCTIONS

The basic travelling-wave circuit function is the amplifier. The distributed concept requires gain devices with relatively large input and output impedances to facilitate periodic loading of transmission line structures that absorb parasitic reactances of the gain device. The original distributed amplifier work applied travelling-wave techniques to vacuum tubes. Vacuum tubes, with extremely high input impedances and relatively high output impedances, are closely approximated in terminal characteristics by the metal semiconductor field effect transistor (MESFET's); therefore, vacuum tube distributed amplifier theory was directly applied to MESFET's.

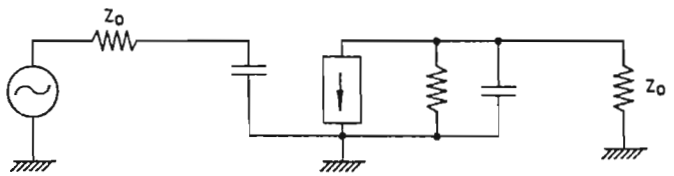
A very basic amplifier can be made by simply connecting a source and a load to a gain device as in Figure 2.1a,b; however, the source is not matched to the amplifier input resulting in reflection of power from the device, and the load is not matched to the output impedance of the device yielding less than optimum power transfer. The device will probably have little gain. The input reflection can be reduced by placing a series inductor between the source and device input to form a low-pass filter section of impedance Z_0 and shunting a resistor of R_0 from the device input to ground as in Figure 2.1c. The device may now be driven from a generator with an output impedance of $Z_0 = R_0$ through any length of transmission line with a characteristic impedance of Z_0 without load reflections. Similar configuration of the output circuit results in a matched output condition; however, as the device impedances are not matched and lossy components have been introduced the gain will be much smaller than the maximum available gain of the device.

To compensate for the low gain of one stage the input and output discrete transmission lines may be extended with additional gain devices as shown in Figure 2.1d. The voltage induced at each node of the input line appears at the gate of a MESFET. The current in the drain of each device splits to the left and right in the output line. If the input and output line have equal phase velocities the components of current travelling to the right sum vectorially at the output. The components

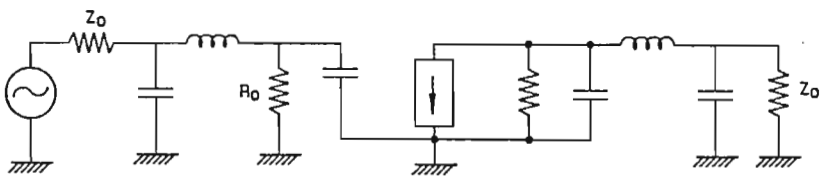
travelling to the left do not add equally and are terminated in the matched load.



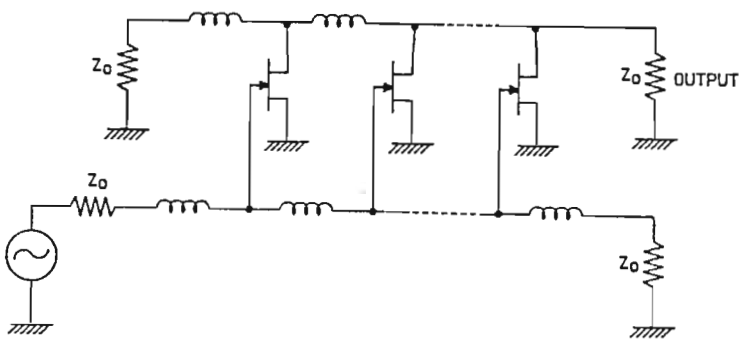
(a) Simple Amplifier



(b) Equivalent Circuit



(c) Lowpass Input/Output Filters



(d) Travelling-Wave Amplifier

Figure 2.1. Travelling-Wave Amplifier Evolution

Ideal gain devices with very large input impedances shunted by a small capacitor and only current sources in the output circuit would result in a distributed amplifier whose gain would increase as stages were added ad infinitum; however, the gain devices are not ideal so the inputs have finite loss and the output current sources are shunted by a moderately low resistance. These resistive losses result in a decreasing wave amplitude along the line as its length is increased. This means that the gain will increase with added stages to a point and will then decrease with added stages after that point. There is an optimum number of stages for a given type of gain device [13].

Distributed amplifiers are topographically simple due to the repetitive and planar (no crossovers) schematic as shown in Figure 2.2; however, because of the large component count the discrete component circuit is generally difficult to fabricate. The development of monolithic microwave integrated circuit technology has practically negated the disadvantage of a large component count. All of the components of a microwave distributed amplifier are small; therefore, circuit complexity becomes largely a lithographic problem and the main problem is then that of reducing the total semiconductor substrate area. Multistage MMIC distributed amplifiers require very little semiconductor area (typically less than three millimeters square).

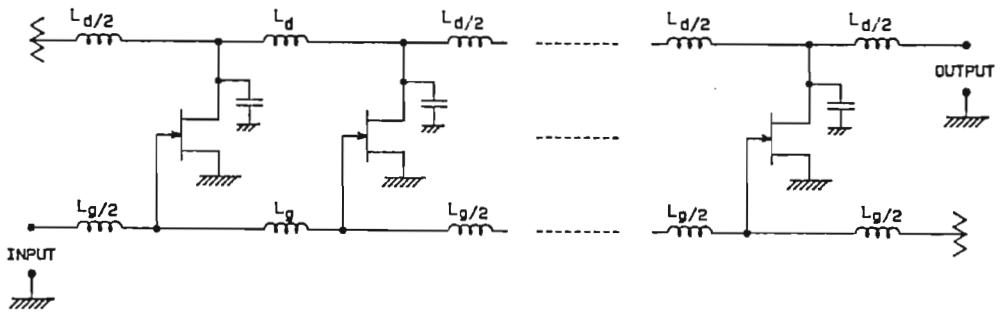


Figure 2.2. Distributed Amplifier Topography

The reduction in substrate area has given the distributed amplifier MMIC a cost advantage as a general system component over various custom or narrow band designs. The same concepts can now be extended to other system components such as mixers and oscillators. The operating mode of the gain device does not change significantly in the travelling-wave

circuit from the mode used in the single device circuit. For a mixer a large local oscillator input is required to drive the device through operating regions where the gain characteristics of the device change with the period of the driving signal. This change nonlinearly modulates a simultaneous input signal resulting in products of the local oscillator and input signal appearing at the output of the circuit. As the impedance levels are well defined at the terminals of the distributed circuit the negative resistance oscillator is relatively difficult to implement; therefore, a feedback oscillator is the best choice for a distributed circuit oscillator. As in a single device oscillator the device output is routed back to the input through a frequency selective component. When the loop gain is greater than unity and there is no phase change in the loop (additive feedback) the circuit will oscillate.

With the usual single gate FET mixer the local oscillator and signal are summed in a coupler before being applied to the gate (or source for a common gate mixer). This is the obvious method of feeding the two signals to a travelling-wave mixer; however, the author has fed the local oscillator to the terminated end of the input line by replacing the line termination with a local oscillator source. This eliminates the external coupler while still applying both signals to all stages in the mixer. The mixer products can now be taken from either end of the output line.

The travelling-wave oscillator is configured by taking either output of the output transmission line and passing it through a frequency selective device and back into the input line at the opposing end of the amplifier. When the oscillator is turned 'on' the oscillations will grow at the frequency of the feedback element bandpass. This growth will continue until the amplifier saturates thus reducing the amplifier gain. The steady state loop conditions will occur when the amplifier has gone far enough into saturation to make the loop gain exactly unity.

Section 2.A. Amplifier

Distributed or travelling-wave amplification with discrete devices utilizes lumped and semi-lumped distributed transmission line techniques to increase the gain-bandwidth product of an amplifier. The input and output capacitances of the two-port gain elements are combined with lumped

inductors (or short high impedance transmission line sections) to form artificial transmission lines going to the input and output ports. Incorporation of the unwanted gain device parasitics into the transmission line facilitates partial summing of transconductances without simultaneous summing of input and output capacitances.

The first distributed amplifiers were implemented with vacuum tubes for video frequency applications [3]; however, with the substitution of the MESFET as the gain element and by fabricating the amplifiers as monolithic microwave integrated circuits to minimize parasitic elements a unique circuit function has evolved. This circuit function has gain over an extremely broad bandwidth and the terminals are already matched to the system characteristic impedance (typically fifty ohms).

A first order design of a distributed amplifier involves computing the artificial transmission line (Figure 2.3) components for the MESFET gate and drain lines. The characteristic impedance of the lines will be [16]

$$Z_0 = \left(\frac{L}{C}\right)^{\frac{1}{2}} \qquad \text{eq.(2.1)}$$

As C_{gs} is larger than C_{ds} and the drain line impedance will generally equal the source line impedance to equalize the phase velocities, the capacitance C is chosen to equal C_{gs}. This defines the inductance L. A drain-to-source capacitance is then added to C_{ds} to equalize the line capacitances and the same inductance is used in the gate and drain. A more involved design considers gate and drain line loss and the tradeoffs of adding stages fed with reduced power [13].

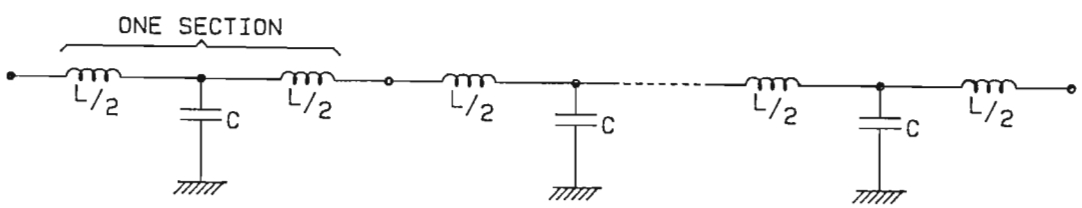


Figure 2.3. Artificial Transmission Line

The cutoff frequency of the artificial transmission line is approximately the rolloff frequency of the amplifier for a small number of amplifier sections. The cutoff frequency of the line is

$$f_c = \frac{1}{\pi(LC)^{1/2}} \qquad \text{eq.(2.2)}$$

A sampling of published literature on integrated travelling-wave amplifiers is presented in the references [7-13]. In all cases the distributed or travelling-wave amplifier is treated as a two-port device as shown in Figure 2.2. Opposing ends of gate and drain lines are terminated in the characteristic impedance of the lines. In actual fact the distributed amplifier is a four-port. As shown in Figure 2.4 a signal at port (1) is amplified at port (2) as in the usual two-port; however, a signal in port (3) is also amplified at port (4). There is some degree of isolation between ports (1) and (4) and ports (3) and (2) but very little isolation between ports (1) and (3) and ports (2) and (4).

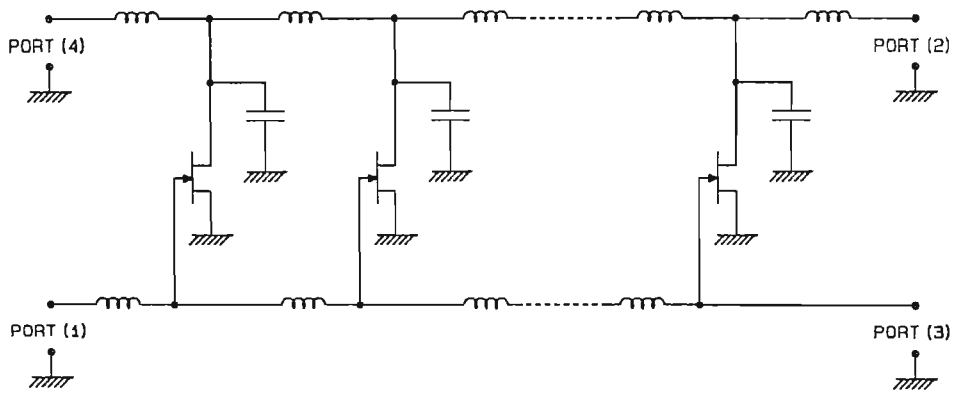


Figure 2.4. Four-Port Travelling-Wave Amplifier

A simplified expression for the gain from input port (1) to output port (2) of the distributed amplifier can be obtained by considering that the current from each drain splits in two directions regardless of the input port, and the phase shifts between all gate nodes and all drain nodes are equal. Figure 2.5 illustrates this by replacing the artificial transmission lines with phase shifts $\theta(f)$ and transconductance gain blocks

G for an n-section amplifier. The current I_2 out of port (2) due to an input $E_1/2$ to port (1) assuming equal splitting of current to the left and to the right at the output of each gain block (that is, light line loading and matched terminations at the ends of the lines) is

$$I_2 = \frac{E_1 G_2}{4} e^{-j(n-1)\,\theta(f)} + \frac{E_1 G_2}{4} e^{-j(n-1)\,\theta(f)} \cdots + \frac{E_1 G_n}{4} e^{-j(n-1)\,\theta(f)}$$

so

$$I_2 = \sum_{m=1}^{n} \frac{E_1 G_m}{4} e^{-j(n-1)\,\theta(f)} \qquad = \frac{nE_1 g}{4} e^{-j(n-1)\,\theta(f)}$$

and

$$G_{21} = \frac{|I_2|^2 R_0}{|E_1|^2/4R_0} = \left(\frac{ngR_0}{2}\right)^2 \qquad \text{eq.(2.3)}$$

where $G_1 = G_2 = \ldots G_n = g$. Note that the gain is not frequency dependent except for transmission line cutoff and device degradation. The equation for forward gain from input port (3) to the output port (4) is identica

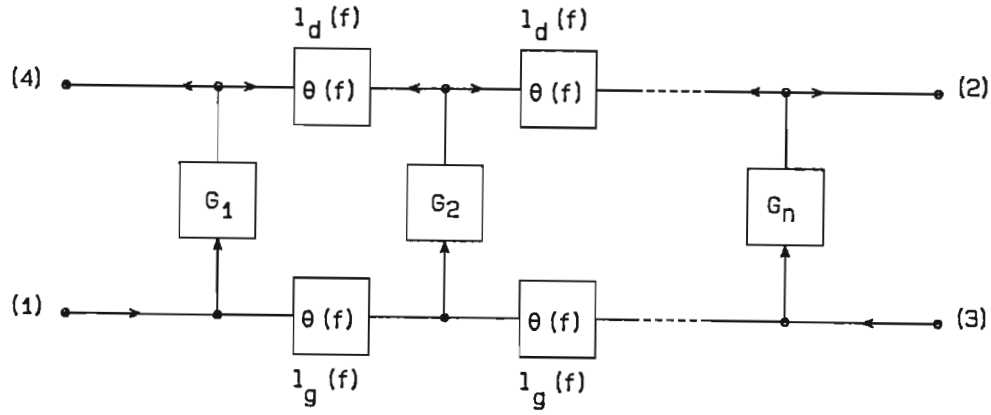


Figure 2.5. n-Section Ideal Distributed Amplifier

Consider now the gain from input port (1) to output port (4). Voltage out of port (4) due to an input to port (1) is

$$I_4 = \frac{E_1 G_1}{4} + \frac{E_1 G_2}{4} e^{-j2\theta(f)} + \ldots \frac{E_1 G_n}{4} e^{-j2(n-1)\theta(f)}$$

so

$$I_4 = \sum_{m=1}^{n} \frac{E_1 G_m}{4} e^{-j2(m-1)\theta(f)}$$

The gain is

$$G_{41} = \frac{|I_4|^2 R_0}{|E_1|^2/4R_0} \qquad \text{where}$$

$$|I_4|^2 = \left(\frac{E_1 g}{4}\right)^2 \sum_{m=1}^{n} e^{-j2(m-1)\theta(f)} \cdot \sum_{m=1}^{n} e^{j2(m-1)\theta(f)}$$

$$G_{41} = \left(\frac{gR_o}{2}\right)^2 \sum_{m=1}^{n} e^{-j2(m-1)\theta(f)} \cdot \sum_{m=1}^{n} e^{j2(m-1)\theta(f)} \qquad \text{eq.(2.4)}$$

The gain then varies between ports (1) and (4) as a function of frequency. The frequency sensitive phase term $\theta(f)$ can be calculated for an artificial transmission line with a cutoff frequency of f_c from the circuit in Figure 2.6.

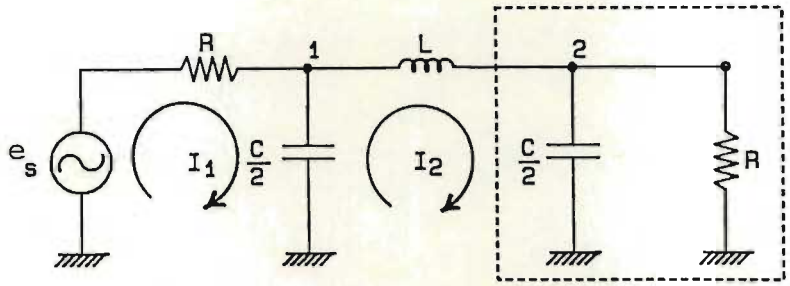


Figure 2.6. Circuit for Calculation of Phase Shift between Terminal Nodes

The loop equations for the circuit are

$$e_s = \left(R_0 + \frac{2}{sC} \right) I_1 - \frac{2}{sC} I_2 \qquad \text{eq.(2.5)}$$

and

$$0 = -\frac{2}{sC} I_1 + \left(\frac{2}{sC} + sL + \frac{2R_0}{2 + R_0 sC} \right) I_2 \qquad \text{eq.(2.6)}$$

This yields

$$I_2 = \frac{e_s \left(\frac{2}{sC} \right)}{\Delta}$$

where Δ is the determinant of the coefficient matrix

and the voltage at node 2 is

$$e_2 = I_2 \left(\frac{2R_0}{2 + R_0 sC} \right) .$$

The forward gain component of the scattering matrix is

$$S_{21} = \frac{e_2}{e_s/2} \quad .$$

Substituting $R_0 = (L/C)^{1/2}$,

$$\omega_c = \frac{2}{(LC)^{1/2}} \quad \text{and} \quad \omega_n = \omega/\omega_c$$

yields

$$S_{21} = \frac{1}{1 - 2\omega_n^3 + j(2\omega_n - \omega_n^3)} \quad . \qquad \text{eq.(2.7)}$$

The phase term to be used in equation 2.4 is then

$$\theta(f) = \tan^{-1}\left(\frac{2\omega_n - \omega_n^3}{1 - 2\omega_n^3}\right) \quad . \qquad \text{eq.(2.8)}$$

Making this substitution and solving for the port (1) to port (4) gain of the distributed amplifier results in the response curve of Figure 2.7 where the gain is normalized to S_{21} of the amplifier.

The nulls in this response are very deep because no attenuation is present in the gate and drain lines. All of the drain signal current then arrives at the terminating loads. In actual fact the gate and drain lines are lossy primarily because of FET gate loss and finite output impedance. The lines must actually be modelled as shown in Figure 2.8.

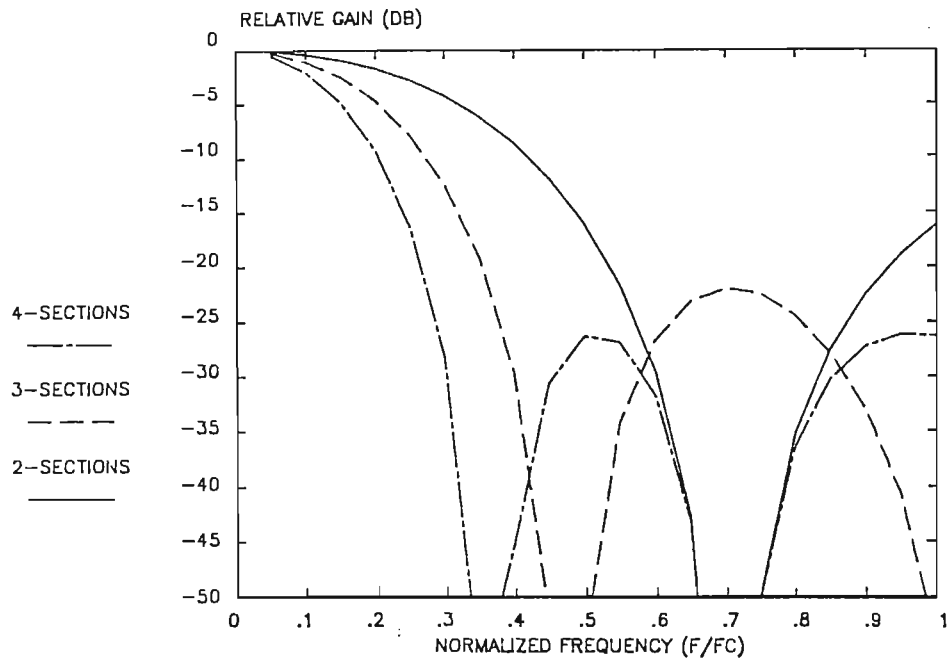
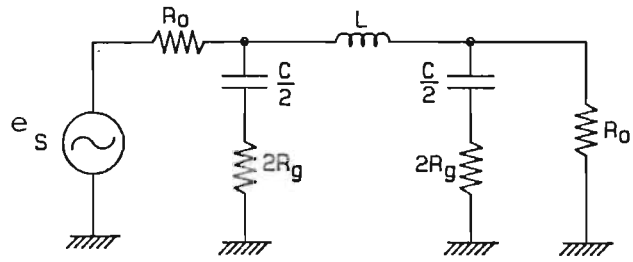
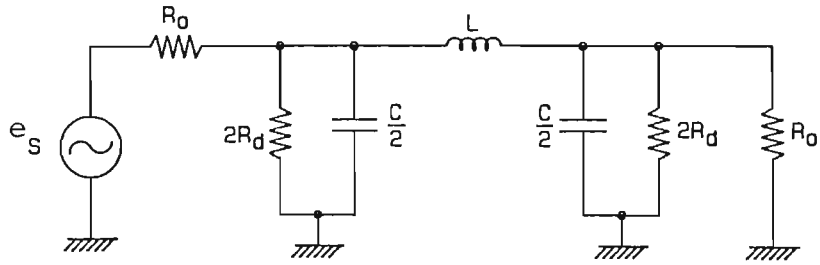


Figure 2.7. Computed Relative Frequency Response (S_{41}/S_{21}) for an Ideal Distributed Amplifier.



(a) Lossy Gate Line



(b) Lossy Drain Line

Figure 2.8. Lossy Lumped Element Transmission Lines

Using similar substitutions for these lines as those used for the lossless line the transfer equation for the gate line is

$$S_{21} = \frac{1 + j\,2\frac{R_g}{R_0}\omega_n}{R_0 - \omega_n^2(R_0 + 2R_g) + j\omega_n(2R_g + R_0)} \cdot B \qquad \text{eq.(2.9)}$$

where $$B = \frac{R_0 + j2R_g\omega_n}{1 + j\left(2\frac{R_g}{R_0} + 1\right)\omega_n}$$

and for the drain line

$$S_{21} = \frac{1}{1 + \frac{R_0}{2R_d} - \omega_n^2\left(\frac{R_0}{R_d} + 2\right) + j\left[\omega_n\left(\frac{R_0}{4R_d} + \frac{R_0}{R_d}\right) + 2 - \omega_n^3\right]} .$$

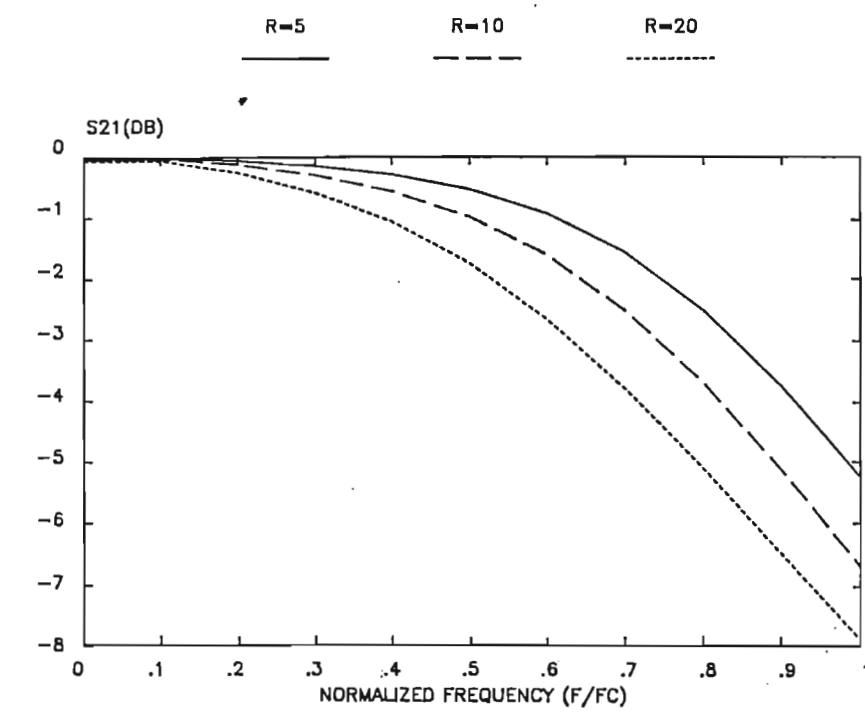
eq.(2.10)

Nominal values for R_g range from five to twenty ohms and for R_d from about two hundred and fifty to one thousand ohms. Plots of S_{21} for the gate and drain lines in Figures 2.9 and 2.10 are split into magnitude and phase.

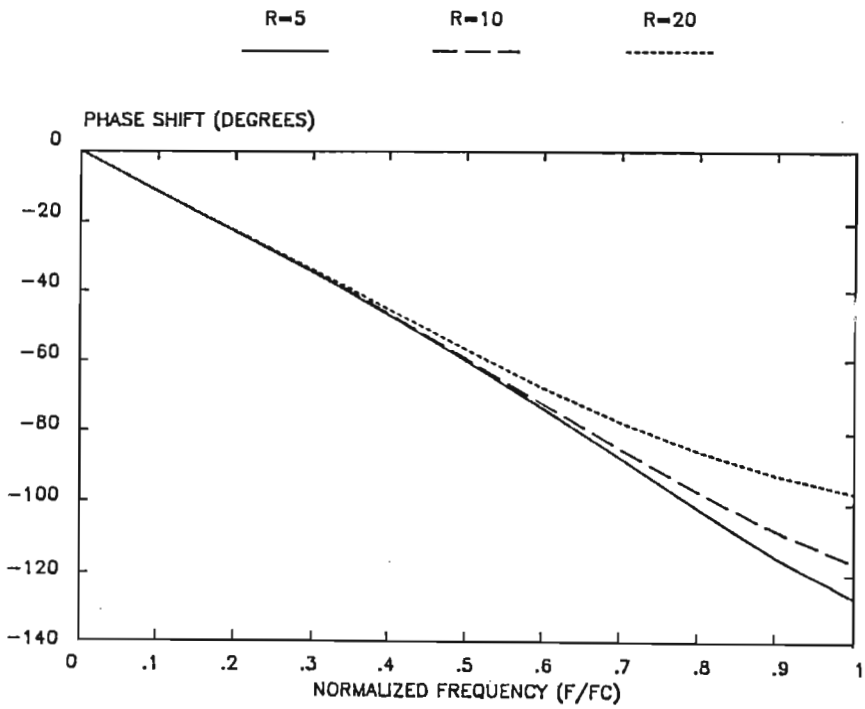
Approximate gain terms for the various amplifier configurations can now be derived by allowing the forward transfer term to equal a loss term 1 times a phase shift term θ

$$S_{21} = 1 \cdot \exp(j\theta).$$

Note that this method will yield a slightly pessimistic result (that is, a gain somewhat smaller than that derived from an exact analysis) as the effects of the reflection coefficients are ignored. Also, gain peaking at or above the cutoff frequency of the transmission lines is not predicted because the interaction of the reflections above cutoff is not considered.

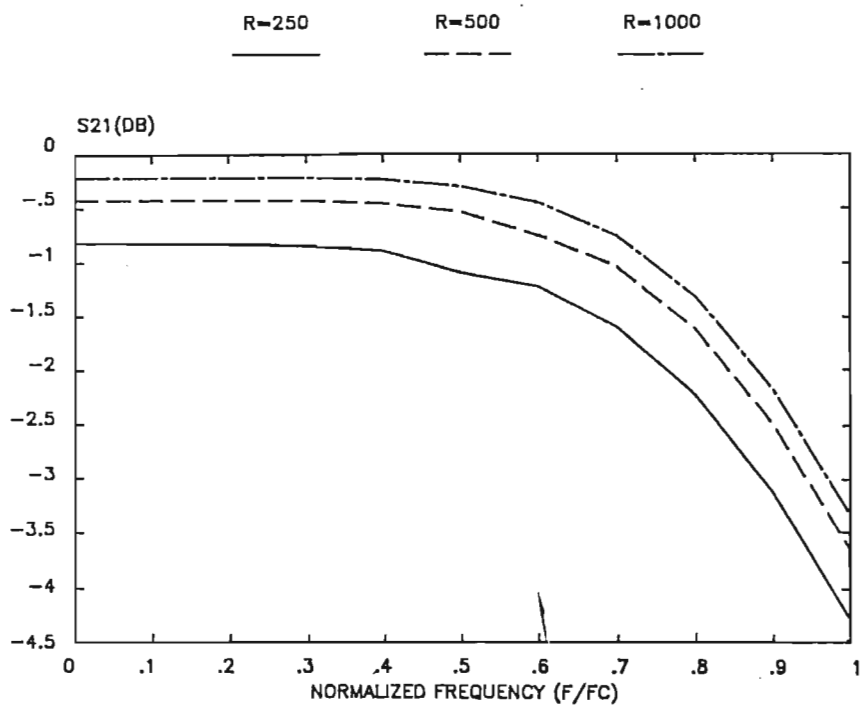


(a) Gate Line Loss/Section

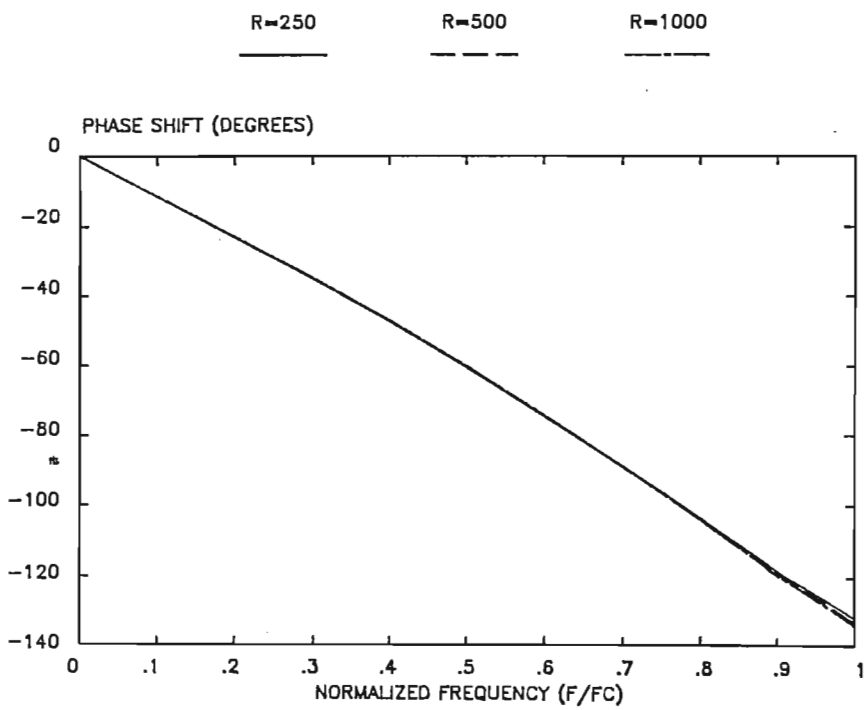


(b) Gate Line Phase Shift/Section

Figure 2.9. Lossy Gate Line



(a) Drain Line Loss/Section



(b) Drain Line Phase Shift/Section

Figure 2.10. Lossy Drain Line

The port (1) to port (2) gain of the distributed amplifier is then (referencing Figure 2.11)

$$\frac{e_0}{e_i} = \frac{R_0}{2} \sum_{m=1}^{n} G_m l_d^{n-m} l_g^{m-1} \exp\left(-j[\theta_d \cdot (n-m) + \theta_g \cdot (m-1)]\right) \qquad \text{eq.(2.11)}$$

and the port (1) to port (4) gain is

$$\frac{e_0}{e_i} = \frac{R_0}{2} \sum_{m=1}^{n} G_m l_d^{m-1} l_g^{m-1} \exp\left(-j[\theta_d \cdot (m-1) + \theta_g \cdot (m-1)]\right) \qquad \text{eq.(2.12)}$$

These gains normalized to $(nGR_0/2)^2$ at zero frequency and

for $G = G_1 = G_2 = \ldots G_n$

are plotted in Figure 2.12 for $R_g = 0\Omega$ and $R_d = 10M\Omega$ and in Figures 2.13 and 2.14 for $R_g = 15\Omega$ and $R_d = 200\Omega$. Note that the addition of circuit losses has a marked effect with an increase in the number of stages in Figures 2.12 and 2.13. Nulls in the S_{41} response are reduced as will be seen by comparing Figure 2.14 with Figure 2.7.

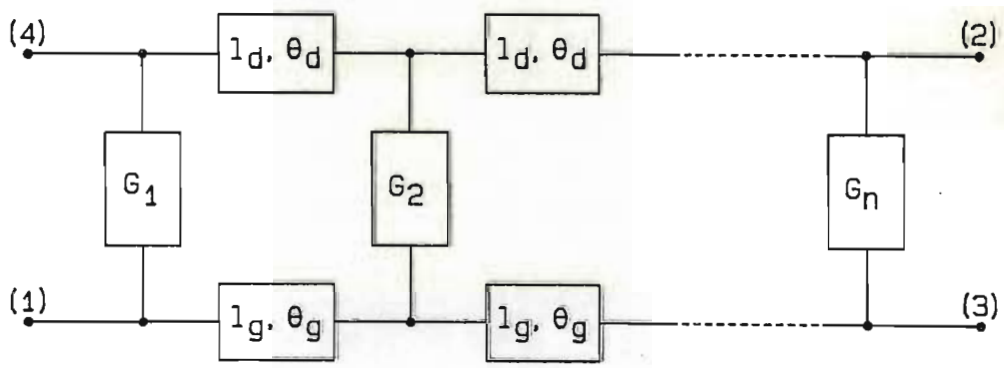


Figure 2.11. Generalized Distributed Amplifier with Lossy Lines

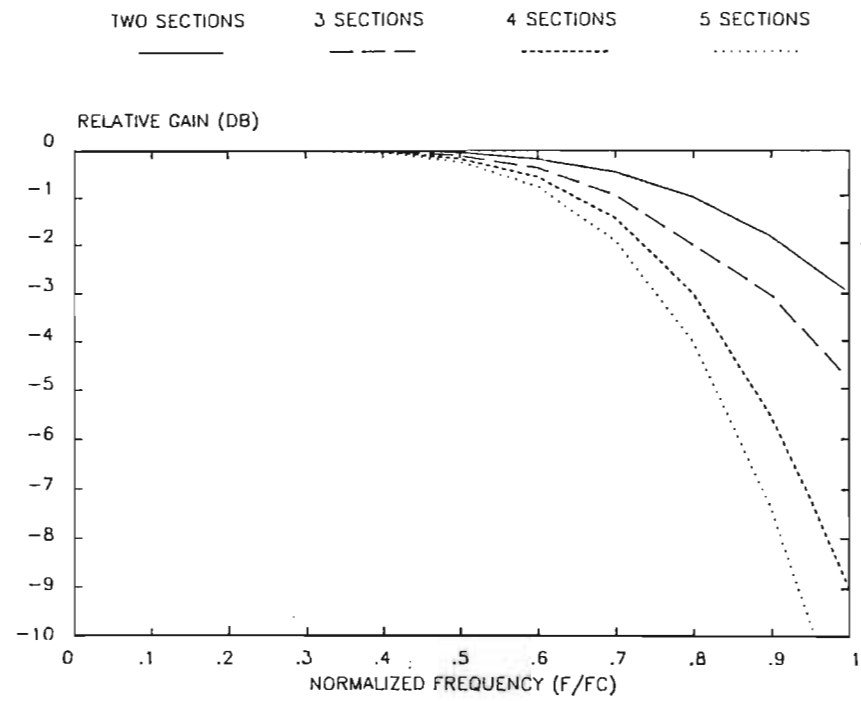


Figure 2.12. $|S_{21}|$ versus Normalized Frequency for $R_g = 0\Omega$ and $R_d = 10M\Omega$.

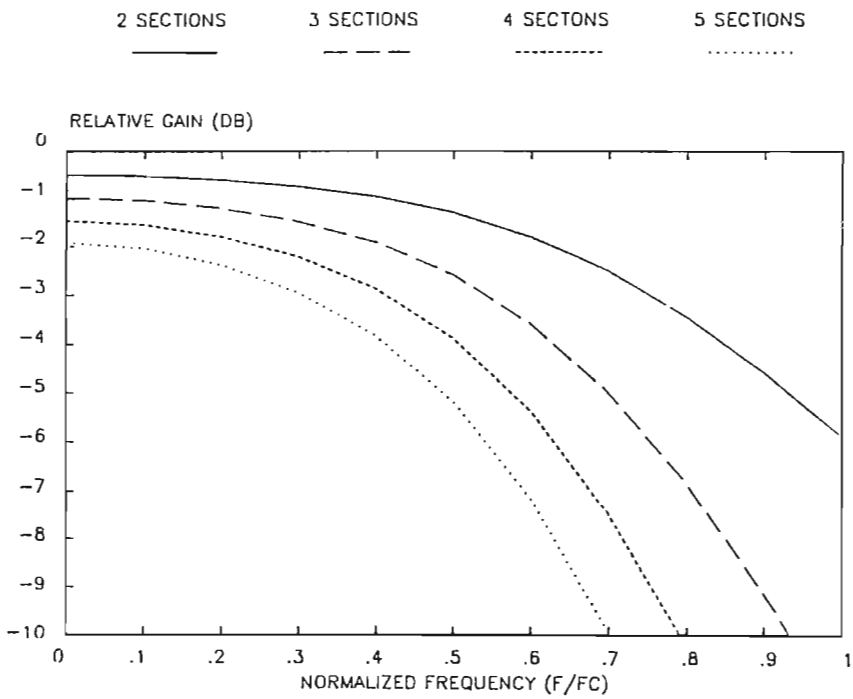


Figure 2.13. $|S_{21}|$ versus Normalized Frequency for $R_g = 15\Omega$ and $R_d = 200\Omega$.

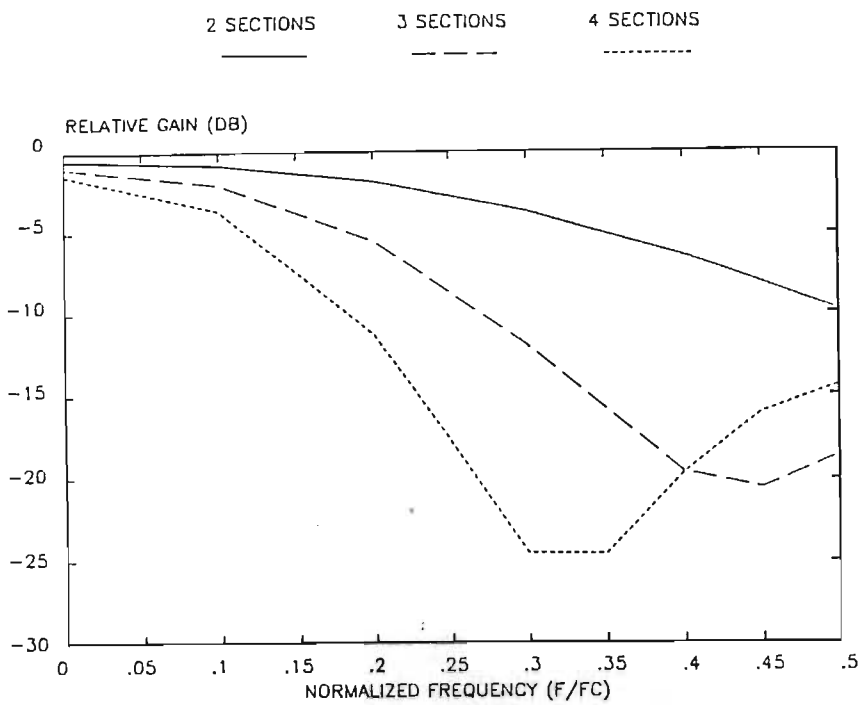


Figure 2.14. $|S_{41}|$ versus Normalized Frequency for $R_g = 15\Omega$ and $R_d = 200\Omega$.

The travelling-wave amplifier can be designed and exactly analysed using a four-port scattering matrix and its associated four-port wave scattering matrix. For example, given a catalog of four-port elements as shown in Figure 2.15, a travelling-wave amplifier, Figure 2.16, can be configured. If the wave scattering matrix (also called a chain scattering matrix) of each component is $[\Phi_n]$ and a transform of matrix $[\Phi_n]$ is $[S_n]$ (the scattering matrix of each component) denoted

$$\Phi_n = \text{transform}[S_n] = T[S_n] \quad \text{and} \quad S_n = T[\Phi_n]$$

then

$$\Phi t = \prod_{m=1}^{n} \Phi m$$

and

$$S_t = T[\Phi_t] .$$

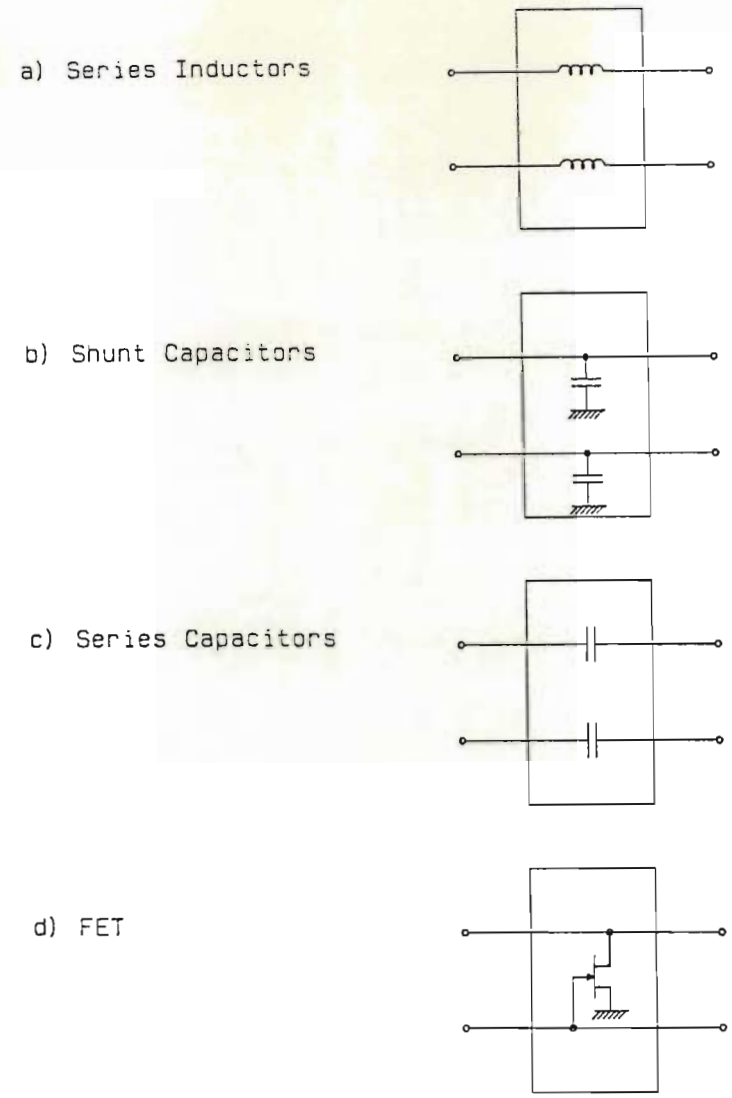


Figure 2.15. Definition of Some Four-Port Elements

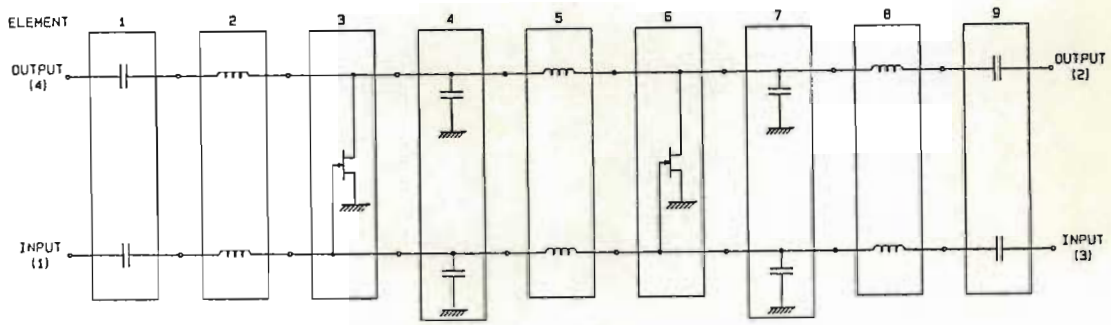


Figure 2.16. Two Section Distributed Amplifier Configured from Four-Port Elements.

The transform pairs are derived in Appendix B. Also included in the appendix is the flowchart of the computer program for calculating S_n for each component, C_n for each S_n, multiplying the matrices and computing S_t from C_t.

Section 2.B. Mixer

Non-linear components of multiple time variant voltages will be generated by a MESFET under particular bias and drive conditions. By appropriate assignment of source and load impedances and a non-linear model of the active element the gain of the various input and output components can be approximated [16-20].

A non-linear model of a MESFET, Figure 2.17, has components C_{gs}, R_d and g_m that will vary with d.c. bias and signal amplitude. If one component of the input is considerably larger than the other input and the d.c. bias remains constant, the non-linear model elements will vary more with the period of the large input than with the period of the small input. C_{gs}, R_d and g_m will then become functions of time $C_{gs}(t)$, $R_d(t)$ and $g_m(t)$ where the time dependence is upon the large (local oscillator) input. Numerous investigations [14,17] and the author's measurements indicate that the largest contributor to mixing is the transconductance $g_m(t)$. The capacitance $C_{gs}(t)$ and source drain resistance $R_d(t)$ values can be taken as the time average components C_{gs} and R_d.

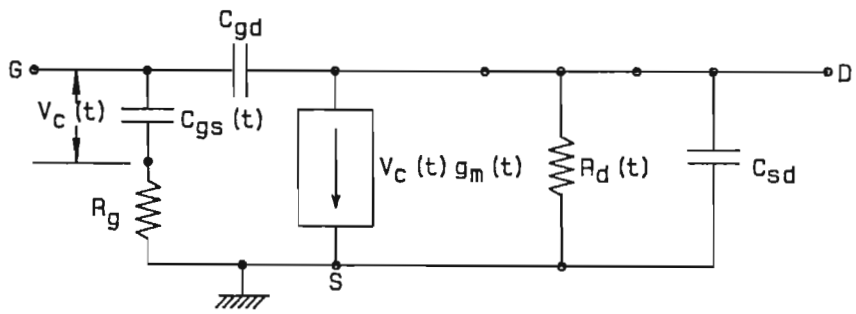


Figure 2.17. MESFET Mixer Model

By applying a constant gate to source bias and a large local oscillator (LO) input superimposed on a lower level signal voltage, intermodulation current components that are a function of the nonlinear transconductance are generated in the source-drain circuit.

Assume the instantaneous value of the time dependent transconductance has the form

$$G(t) = k_0 + k_1\, e(t) + k_2\, e^2(t) \qquad \text{eq.(2.13)}$$

where

$$e(t) = V_{gs} + e_{lo} \sin \omega_{lo} t.$$

Expanding

$$G_m(t) = k_0 + k_1 V_{gs} + k_1 e_{lo} \sin \omega_{lo} t + k_2 V_{gs}^2 + 2k_2\, V_{gs}\, e_{lo} \sin \omega_{lo} t + k_2 e_{lo}^2 \sin^2 \omega_{lo} t \qquad \text{eq.(2.14)}$$

where the terms

$$G_{amp} = k_0 + k_1 V_{gs} + k_2 V_{gs}^2 \qquad \text{eq.(2.15)}$$

result in amplifier gain and the terms

$$G_{mix} = k_1 e_{lo} \sin \omega_{lo} t + 2k_2 V_{gs} e_{lo} \sin \omega_{lo} t$$

hence

$$G_{mix} = (k_1 e_{lo} + 2k_2 V_{gs} e_{lo}) \sin \omega_{lo} t \qquad \text{eq.(2.16)}$$

result in mixer gain. The second order term $k_2 e_{lo}^2 \sin^2 \omega_{lo} t$ indicates that the device can be used as a second harmonic mixer.

The mixer output terms due to a signal input $e_{rf} \cos \omega_{rf} t$ are

$$I_{mix} = G_{mix} \cdot e_{rf} \cos \omega_{rf} t$$

so

$$I_{mix} = (k_1 e_{lo} e_{rf} + 2k_2 V_{gs} e_{lo} e_{rf}) \left(\frac{\sin(\omega_{lo} + \omega_{rf})t}{2} + \frac{\sin(\omega_{lo} - \omega_{rf})t}{2} \right). \qquad \text{eq.(2.17)}$$

The output current due to difference terms is

$$I_{if} = \left(\frac{k_1}{2} + k_2 V_{gs} \right) \cdot e_{lo} e_{rf} \sin (\omega_{lo} - \omega_{rf})t \qquad \text{eq.(2.18)}$$

Pucel et al [17] define a method of analysis for single device MESFET mixers where all input and output frequency components can be terminated in the appropriate impedance to calculate mixer gain. For the non-linear MESFET model an analysis circuit considering linear and squared signal plus LO terms is shown in Figure 2.18. The impedances Z_m are coupled to the input and output by ideal filters F_m to feed or terminate signals at one specific frequency. Note that as the time dependence of the mixer is already considered in g_m there is no need to retain the LO source and termination in this circuit so only Z_1 to Z_6 impedances are retained in the analysis. This is not to say that the proper termination of the LO out of the mixer is not important.

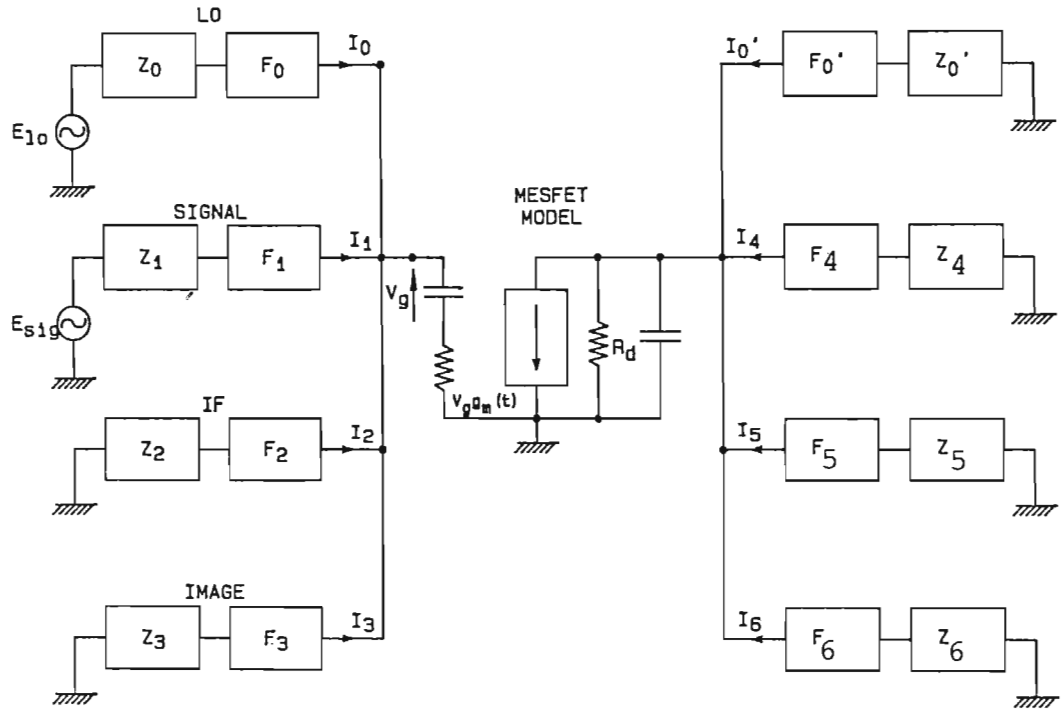


Figure 2.18. MESFET Mixer Analysis Circuit

The circuit voltages and currents are related by

$$V_k = E_k - I_k Z_k \quad (k = 1,2...6) \qquad \text{eq.(2.19)}$$

where $E_k = 0$ for $k \neq 1$.

Also $V_k = [Z_{kl}]\,[I_k]$

where Z_{kl} is the set of six-port circuit impedance parameters describing the transimpedances and mutual impedances of the MESFET. In matrix notation this can be written as

$$[E] = [V] + [Z_t]\,[I]$$

$$= [Z_m]\,[I] + [Z_t]\,[I] \qquad \text{eq.(2.20)}$$

where

$$[E] = \begin{bmatrix} E_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad [V] = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix}$$

and

$$[I] = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix}.$$

$[Z_m]$ and $[Z_t]$ represent the mixer and the mixer terminations respectively.

These matrices are

$$[Z_m] = \begin{bmatrix} Z_{11} & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_{22} & 0 & 0 & 0 & 0 \\ 0 & 0 & Z_{33} & 0 & 0 & 0 \\ Z_{41} & 0 & Z_{43} & Z_{44} & 0 & 0 \\ Z_{51} & Z_{52} & Z_{53} & 0 & Z_{55} & 0 \\ Z_{61} & Z_{62} & Z_{63} & 0 & 0 & Z_{66} \end{bmatrix}$$

and

$$[Z_T] = \begin{bmatrix} Z_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & Z_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & Z_4 & 0 & 0 \\ 0 & 0 & 0 & 0 & Z_5 & 0 \\ 0 & 0 & 0 & 0 & 0 & Z_6 \end{bmatrix}.$$

Replacing the non-linear MESFET model in Figure 2.18 with an ideal non-linear travelling-wave amplifier section model, Figure 2.19, and neglecting all gain terms except $g_0 = G_{amp}$ and $g_1 = G_{mix}$ the matrix elements are

$$Z_{kk} = R_0$$

$$Z_{41} = -g_0 R_0^2$$

$$Z_{51} = -g_1 R_0^2$$

$$Z_{61} = -g_1 R_0^2$$

$$Z_{52} = -g_0 R_0^2$$

$$Z_{62} = -g_1 R_0^2$$

$$Z_{63} = -g_0 R_0^2$$

$$Z_{43} = Z_{53} = -g_1 R_0^2$$

and $Z_l = R_0$ for $l = 1$ to 6.

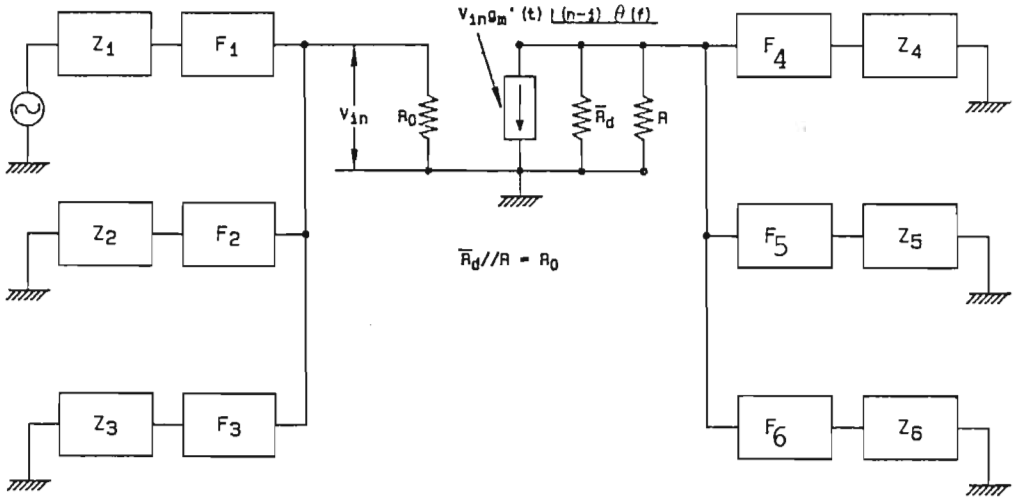


Figure 2.19. Two-Port Travelling-Wave Mixer Section Analysis Circuit

The set of equations for the simplified two-port travelling-wave mixer are then

$$\begin{bmatrix} E_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = R_0 \cdot \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ -g_0R_0 & 0 & -g_1R_0 & 1 & 0 & 0 \\ -g_1R_0 & -g_0R_0 & -g_1R_0 & 0 & 1 & 0 \\ -g_1R_0 & -g_1R_0 & -g_0R_0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix}$$

$$+ R_0 \cdot \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix}$$

eq.(2.21)

The conversion gain is the ratio of the IF power out of port (5) to the RF power into port (1) or

$$G_{conv} = \frac{\text{IF power(5)}}{\text{RF power(1)}} = \frac{|I_5|^2 R_0}{|E_1|^2/4R_0} = 4R_0^2 \frac{|I_5|^2}{|E_1|^2} \quad . \qquad \text{eq.(2.22)}$$

Solving equation 2.21 yields

$$I_1 = \frac{E_1}{2R_0} \; , \; I_2 = 0, \; I_3 = 0, \; I_4 = -\frac{g_0 E_1}{4} \; , \; I_5 = -\frac{g_1 E_1}{4}$$

and $I_6 = -\frac{g_1 E_1}{4}$.

The conversion gain of a travelling-wave mixer section is then

$$G_{conv} = \frac{g_1^2 R_0^2}{4} \qquad \text{eq.(2.23)}$$

The transfer function for the two terminal travelling-wave mixer actually contains phase (θ) and loss (Γ) terms that are a funct frequency as in the amplifier. The simplified travelling-wave mixer equivalent circuit in Figure 2.20 can be further reduced to the block equivalent in Figure 2.21 where $\gamma = \Gamma \cdot \exp[j\theta(f)]$.

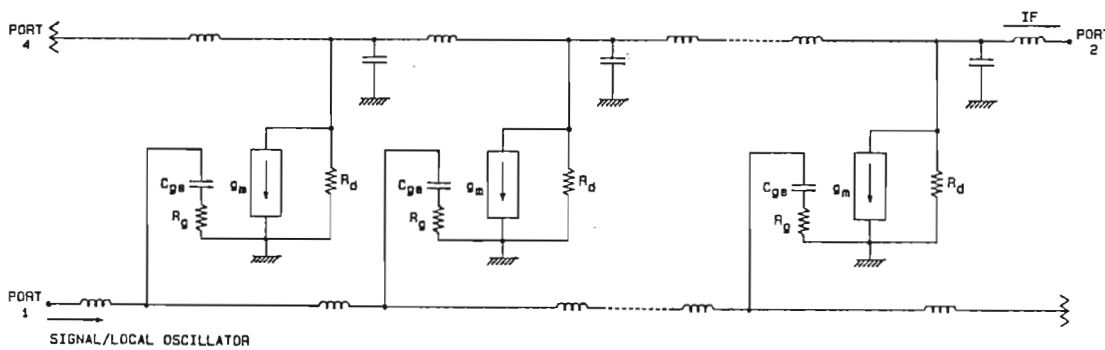


Figure 2.20. Simplified Travelling-Wave Mixer Equivalent Circuit

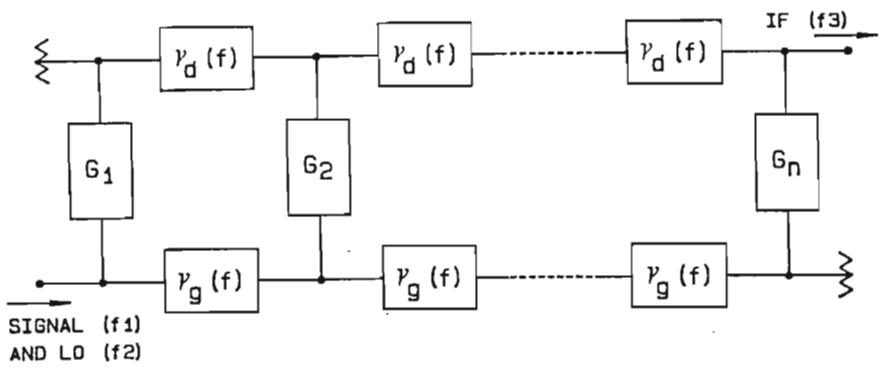


Figure 2.21. Block Equivalent Circuit of a Two-Port Travelling-Wave Mixer

Consider each gain element G_m as a conversion transconductance, let $l = 1$ and retain only nonlinear terms for first order mixing so that

$$G_m = [k_1(m) + 2k_2(m)\ V_{gs}]\ v_{lo}(t)$$

where $v_{lo}(t) = e_{lo} \cos \omega_{lo} t$.

The signal and local oscillator voltages into each gain block are shifted in phase from the input by $(m-1)\theta_g(f)$ where m is the stage number and $\theta_g(f)$ is the frequency dependent phase shift between stage inputs. The inputs to each G_m then contain phase components

$$p\ \theta_g(lo) + q\ \theta_g(rf).$$

where $p = 0$ to $m-1$ and $q = m-1$ to 0.

The output current from each G_m is

$$i_m = (k_1 + 2k_2V_{gs}) \cdot v_{lo}(t) \cdot v_{rf}(t)$$

so

$$i_m = G_m \cdot v_{rf}(t)$$

where $v_{rf}(t) = e_{rf} \cos \omega_{rf} t$.

For a fixed bias V_{gs} the current i_m is proportional to $v_{lo}(t) \cdot v_{rf}(t)$ or

$$i_m \alpha e_{lo} \cos [\omega_{lo}t + p\ \theta_g(lo)] \cdot e_{rf} \cos [\omega_{rf}t + q\ \theta_g(rf)]$$

so

$$i_m \alpha e_{lo} \cos A \cdot e_{rf} \cos B.$$

Using exponential notation to separate the frequency components the current is

$$i_m = G_m\, e_{lo}\, e_{rf}\, \frac{e^{jA} + e^{-jA}}{2} \cdot \frac{e^{jB} + e^{-jB}}{2}$$

so

$$i_m = G_m\, e_{lo}\, e_{rf}\, \frac{e^{j(A+B)} + e^{j(A-B)} + e^{j(B-A)} + e^{-j(A+B)}}{4} \qquad \text{eq.(2.24)}$$

Evaluating the product terms individually

$$A + B = (\omega_{lo} + \omega_{rf})t + p\ \theta_g(lo) + q\ \theta_g(rf) \qquad \text{eq.(2.25a)}$$

$$A - B = (\omega_{lo} - \omega_{rf})t + p\ \theta_g(lo) - q\ \theta_g(rf) \qquad \text{eq.(2.25b)}$$

$$B - A = (\omega_{rf} - \omega_{lo})t - p\ \theta_g(lo) + q\ \theta_g(rf) \qquad \text{eq.(2.25c)}$$

and

$$-(A+B) = -(\omega_{lo} + \omega_{rf})t - p\ \theta_g(lo) - q\theta_g(rf); \qquad \text{eq.(2.25d)}$$

therefore, to evaluate the magnitude and phase of the output current at each product frequency the phase shift terms from gate line input to device input must be adjusted according to the frequency term being evaluated. The sum frequency term $(\omega_{lo} + \omega_{rf})$ out of G_m is then

$$i_m = \frac{G_m e_{lo} e_{rf}}{2} \exp\left\{j[p\theta_g(lo) + q\theta_g(rf)]\right\} \exp[j(\omega_{lo}+\omega_{rf})t]\ . \qquad \text{eq.(2.26)}$$

The $(\omega_{lo} - \omega_{rf})$ term for $\omega_{lo} > \omega_{rf}$ is

$$i_m = \frac{G_m e_{lo} e_{rf}}{2} \exp\left\{j[p\theta_g(lo) - q\theta_g(rf)]\right\} \exp[j(\omega_{lo} - \omega_{rf})t] \quad \text{eq.(2.27)}$$

and the $(\omega_{rf} - \omega_{lo})$ term for $\omega_{rf} > \omega_{lo}$ is

$$i_m = \frac{G_m e_{lo} e_{rf}}{2} \exp\left\{j[-p\theta_g(lo) + q\theta_g(rf)]\right\} \exp[j(\omega_{rf} - \omega_{lo})t] \quad \text{eq.(2.28)}$$

The amplitude and relative phase components of the sum and difference terms can be generalised by the equation

$$i_m = i_{om} \exp j[kp \cdot \theta_g(lo) + hq \cdot \theta_g(rf)] \quad \text{eq.(2.29)}$$

where $$i_{om} = \frac{G_m e_{lo} e_{rf}}{2} \quad \text{eq.(2.30)}$$

and h and k are defined in Table 2.1.

IF	$(\omega_{lo} + \omega_{rf})$	$\omega_{lo} > \omega_{rf}$ $(\omega_{lo} - \omega_{rf})$	$\omega_{rf} > \omega_{lo}$ $(\omega_{rf} - \omega_{lo})$
k	+1	+1	-1
h	+1	-1	+1

Table 2.1. Definition of Phase Term Signs for Mixer Element Output

The intermediate frequency output current terms are then shifted in phase by the drain line sections by the amount $W \cdot \theta_d(if)$ where W is the number of phase shift sections between the mixer element output and the line termination.

It must be reiterated that these gains are computed within a region of operation of the MESFET where the pinchoff voltage $V_p < v_{gs}(t) < 0$ and where the conversion gain is a direct function of local oscillator drive level.

Assuming the output current from the mixer elements split equally to the left and the right in the output transmission line (reference Section 2.A) the G_1 current into the output termination will be

$$I_1 = \frac{i_{o1}}{2} \exp[j(n - 1)\, \theta_d(if)]$$

were n is the total number of stages.

The current out due to G_2 is

$$I_2 = \frac{i_{o2}}{2} \exp\left\{j[k\cdot\theta_g(lo)+h\cdot\theta_g(rf) + (n-2)\theta_d(if)]\right\}.$$

The current out due to G_n is

$$I_n = \frac{i_{on}}{2} \exp\left\{j[k\cdot(n-1)\, \theta_g(lo) + h\cdot(n-1)\, \theta_g(rf)]\right\}.$$

The total current into the output termination is

$$I_T = \sum_{m=1}^{n} \frac{i_{om}}{2} \exp\left\{j[k\cdot(m-1)\, \theta_g(lo) + h\cdot(m-1)\, \theta_g(rf)+(n-m)\, \theta_d(if)]\right\}. \qquad \text{eq.(2.31)}$$

Assume the input and output lines to be below cutoff so the phase can be approximated by $\theta\,(f)$ = constant · frequency = cf. Also let $\theta_g = \theta_d$ and $i_{o1} = i_{o2} = \cdots\cdots i_{on} = i_o$. For the sum intermediate frequency the current I_T into the line terminating resistor is

$$I_T = \frac{ni_o}{2} \exp[j(n-1)cf(IF)] \qquad \text{eq.(2.32)}$$

This current magnitude does not change with frequency; therefore, there is no variation in this mixer configuration for sum frequency mixing in conversion gain with frequency relative to the gain as an amplifier. The conversion gain is a direct function of the local oscillator level. Identical terms are obtained for difference frequency mixing. The relative conversion gain for ideal lossless gate and drain transmission lines is plotted in Figure 2.22. The relative conversion gain is defined as

$$CG_R = 20 \cdot \log_{10} \frac{I_T}{ni_{o/2}} \quad . \qquad \text{eq.(2.33)}$$

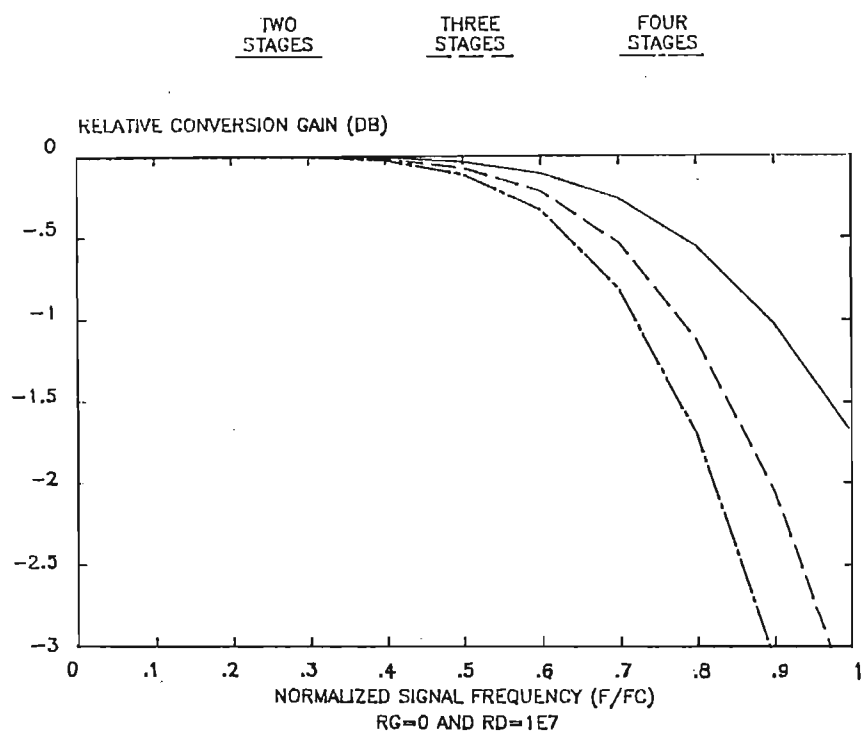


Figure 2.22. Computed Two-Port Relative Conversion Gain as a Function of Signal Frequency with Lossless Transmission Lines: ω_n(LO) = 0.3, ω_n(IF) = difference frequency.

Consider the travelling-wave mixer as a three port device with the signal and local oscillator applied to opposing ends of the gate transmission line as shown in Figure 2.23. Figure 2.24 is the block equivalent circuit for the 3-port mixer. The signal is fed into the left hand gate port and the local oscillator is fed to the right hand gate port. The output is taken from the right hand drain port.

Again using ideal transconductances for the gain blocks and letting l = 1 the current out of G_1 travelling to the output is

$$I_1 = \frac{i_{o1}}{2} \exp\left\{j[k \cdot (n-1)\, \theta_g(lo) + (n-1)\, \theta_d(if)]\right\}.$$

The outputs from the other conversion gain blocks are

$$I_2 = \frac{i_{o2}}{2} \exp\left\{j[k \cdot (n-2)\, \theta_g(lo) + h \cdot \theta_g(rf) + (n-2)\theta_d(if)]\right\}$$

and

$$I_n = \frac{i_{on}}{2} \exp\left\{j[h \cdot (n-1) \cdot \theta_g(rf)]\right\}.$$

The total output current is then

$$I_T = \sum_{m=2}^{n} \frac{i_{om}}{2} \exp\left\{j[k \cdot (n-m)\, \theta_g(lo) + h \cdot (m-1)\theta_g(rf) + (n-m)\theta_d(if)]\right\}. \qquad \text{eq.(2.34)}$$

Again letting $i_{o1} = i_{o2} = \ldots\ i_{on} = i_o$, $\theta_d = \theta_g$ and assuming $\theta(f) = cf$ the output current sum frequency component is

$$I_T = \frac{i_o}{2} \exp\left\{j[\, 2ncf(lo) + (n-1)cf(rf)]\right\} \sum_{m=1}^{n} \exp\,[-j2mcf(lo)]\ . \qquad \text{eq.(2.35)}$$

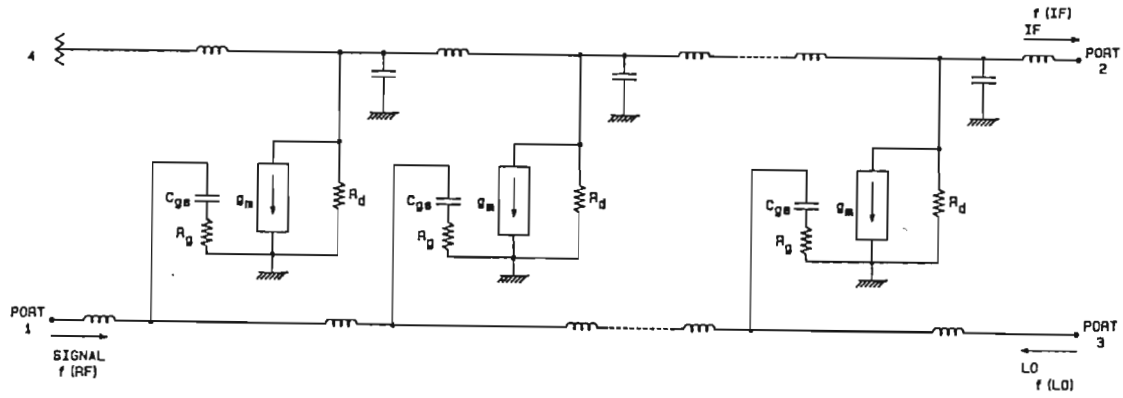


Figure 2.23. Simplified Three-Port Travelling-Wave Mixer Equivalent Circuit

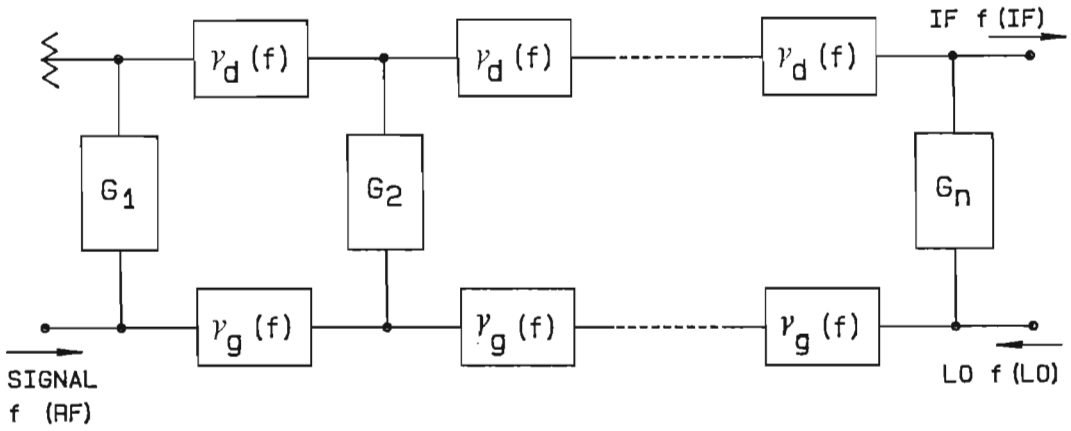


Figure 2.24. Block Equivalent Circuit of a Three-Port Travelling-Wave Mixer

The output current amplitude is then a function of the local oscillator frequency. The relative conversion gain for lossless gate and drain lines is plotted in Figures 2.25 and 2.26 for various numbers of sections as a function of signal and oscillator frequencies. Note that the gain versus frequency curve is the same as the gain curve for the port (1) to port (4) gain of the amplifier with $\theta_d = \theta_g$.

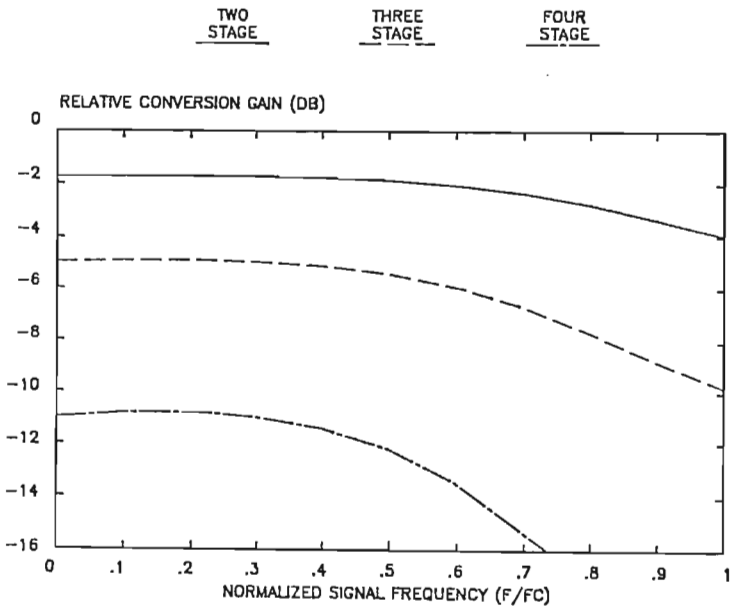


Figure 2.25. Computed Relative Conversion Gain as a Function of Normalized Signal Frequency for a Three-Port Mixer: ω_n(lo) = 0.3 and ω_n(if) = difference frequency.

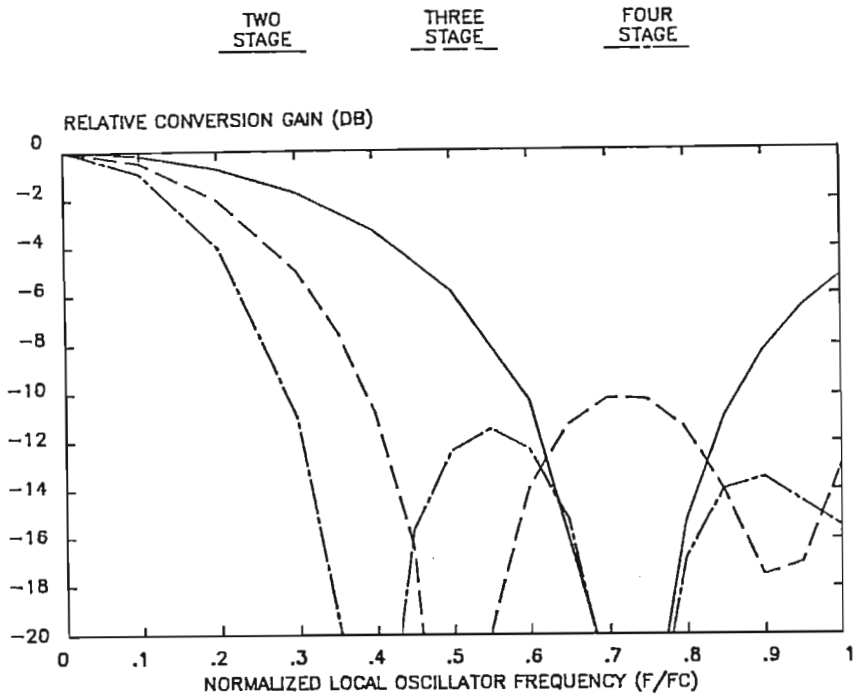


Figure 2.26. Computed Relative Conversion Gain as a Function of Normalized Local Oscillator frequency for a Three-Port Mixer: $\omega_n(rf) = 0.3$ and $\omega_n(if)$ = difference frequency.

The difference frequency current component with f(lo) > f(rf) is

$$I_T = \frac{i_o}{2} \exp\{j[2ncf(lo) - (n-1)cf(rf)]\} \sum_{m=1}^{n} \exp[-j2mcf(lo)] \qquad \text{eq.(2.36)}$$

and with f(rf) > f(lo)

$$I_T = \frac{i_o}{2} \exp\{j[-2ncf(lo) + (n-1)cf(rf)]\} \sum_{m=1}^{n} \exp[j2mcf(lo)] \qquad \text{eq.(2.37)}$$

Note that in both cases the magnitude of the current will be the same as in the sum frequency case and will change as a function only of the local oscillator frequency within the bounds that the signal and intermediate frequencies are well below the cutoff frequency of the gate and drain lines.

Section 2.B.1. Two-Port Distributed Mixer with Lossy Lines

The analysis of the mixer with gate and drain losses is complicated by the fact that the individual conversion transconductances are different because the local oscillator drive levels are different at each device; however, if all of the devices are driven within the bounds of zero volts V_{gs} and V_p the transconductance varies proportionately to the local oscillator drive as expressed in equation 2.16. The transconductance of a device is then reduced by the amount of gate line loss between the LO input and the device gate.

Considering losses and referencing Figure 2.24 where $\gamma = 1 \cdot \exp(j\theta)$ the current output due to G_1 from port (2) with LO and RF inputs to port (1) is

$$I_1 = \frac{i_{o1}}{2} \; 1_d(if)^{n-1} \cdot \exp[j\theta_d(if)].$$

For the second device

$$I_2 = \frac{i_{o1}}{2} \; 1_g(lo) \cdot 1_g(rf) \cdot 1_d(if)^{n-2} \cdot A$$

where

$$A = \exp\{j[k\cdot\theta_g(lo) + h\cdot\theta_g(rf) + (n-2)\cdot\theta_d(if)]\}$$

and for the n^{th} device

$$I_n = \frac{i_{on}}{2} \; 1_g(lo)^{n-1} \cdot 1_g(rf)^{n-1} \cdot B$$

where

$$B = \exp\{j[k\cdot\theta_g(lo)\cdot(n-1) + h\cdot\theta_g(rf)\cdot(n-1)]\} .$$

The total output current is then

$$I_T = \sum_{m=0}^{n} \frac{i_{om}}{2} \cdot l_g(lo)^{m-1} \cdot l_g(rf)^{m-1} \cdot l_d(if)^{n-m} \cdot D$$

where

$$D = \exp\{j[k \cdot \theta_g(lo) \cdot (m-1) + h \cdot \theta_g(rf) \cdot (m-1) + \theta_d(if) \cdot (n-m)]\}.$$

eq.(2.38)

Letting $\omega_n(lo) = 0.3$ and varying $\omega_n(rf)$ from 0.3 to 0.6 varies the difference term $\omega_n(if)$ from 0 to 0.3. The relative conversion gain for $i_{o1} = i_{o2} = \cdots i_{on}$, $R_g = 10\Omega$ and $R_d = 300\Omega$ is plotted against RF frequency in Figure 2.27.

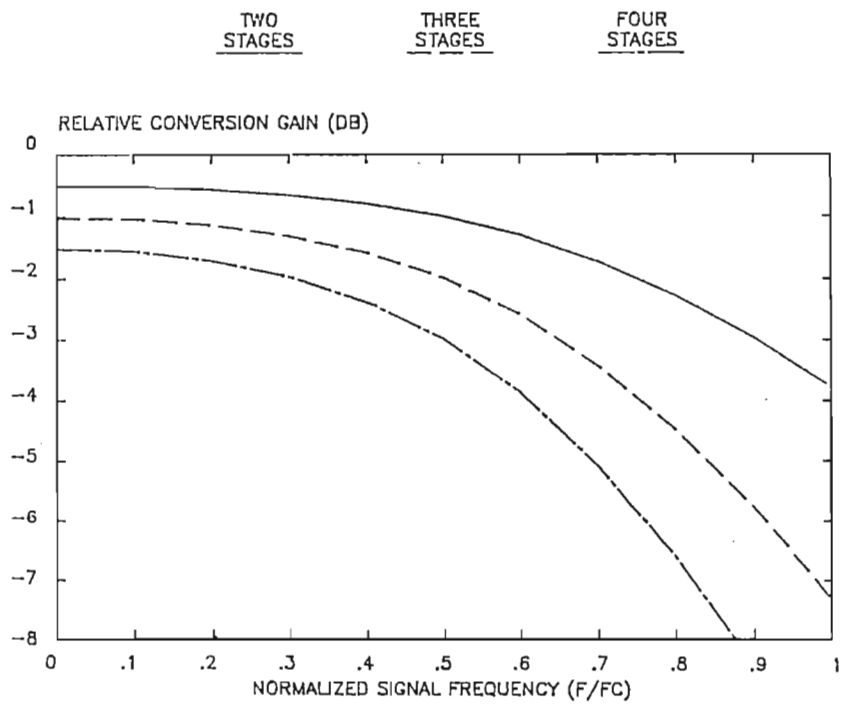


Figure 2.27. Computed Relative Two-Port Conversion Gain Versus Normalized Signal (RF) Frequency for $R_g = 10\Omega$ and $R_d = 300\Omega$, $\omega_n(lo) = 0.3$, $\omega_n(if)$ = Difference frequency.

Section 2.B.2. Three-Port Distributed Mixer with Lossy Lines

The three-port mixer with the RF fed into port (1), the LO into port (2) and the IF taken from port (3) has an output current component due to G_1 of

$$I_1 = \frac{i_{o1}}{2} l_g(lo)^{n-1} \cdot l_d(if)^{n-1} \cdot A$$

where

$$A = \exp\{j[k \cdot \theta_g(lo) \cdot (n-1) + \theta_d(if) \cdot (n-1)]\}.$$

The output current from G_2 is

$$I_2 = \frac{i_{o2}}{2} l_g(lo)^{n-2} \cdot l_g(rf) \cdot l_d(if)^{n-2} \cdot B$$

where

$$B = \exp\{j[k \cdot \theta_g(lo) \cdot (n-2) + h \cdot \theta_g(rf) + \theta_d(if) \cdot (n-2)]\}.$$

and that due to G_n is

$$I_n = \frac{i_{on}}{2} l_g(rf) \cdot \exp[j\, h \cdot \theta_g(rf)].$$

The total current is

$$I_T = \sum_{m=1}^{n} \frac{i_{om}}{2} l_g(lo)^{n-m} \cdot l_g(rf)^{m-1} \cdot l_d(if)^{n-m} \cdot D$$

where

$$D = \exp\{j[k \cdot \theta_g(lo) \cdot (n-m) + h \cdot \theta_g(rf) \cdot (m-1) + \theta_d(if) \cdot (n-m)]\}.$$

eq.(2.39)

The relative conversion gain with $R_g = 10\Omega$ and $R_d = 200\Omega$ is plotted in Figure 2.28 for a down converting mixer with $\omega_n(rf)$ from 0.3 to 0.6. In Figure 2.29 the same transmission line parameters are used but the local oscillator is varied from 0 to 1.0.

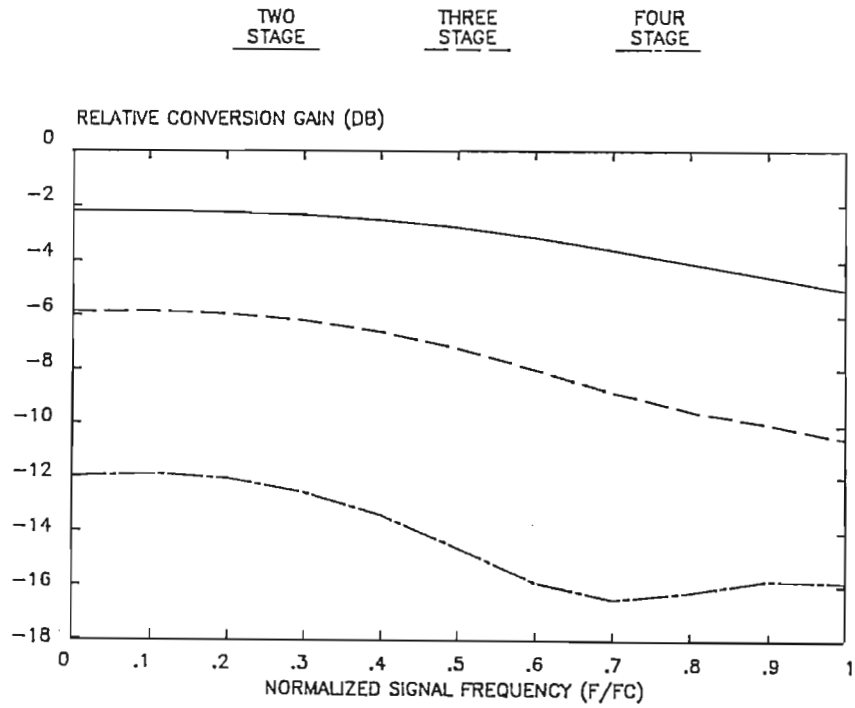


Figure 2.28. Computed Relative Conversion Gain of a Three-Port Mixer as a Function of Normalized Signal (RF) Frequency, $\omega_n(lo) = 0.3$, $R_g = 10\Omega$, $R_d = 300\Omega$, $\omega_n(if)$ = difference frequency.

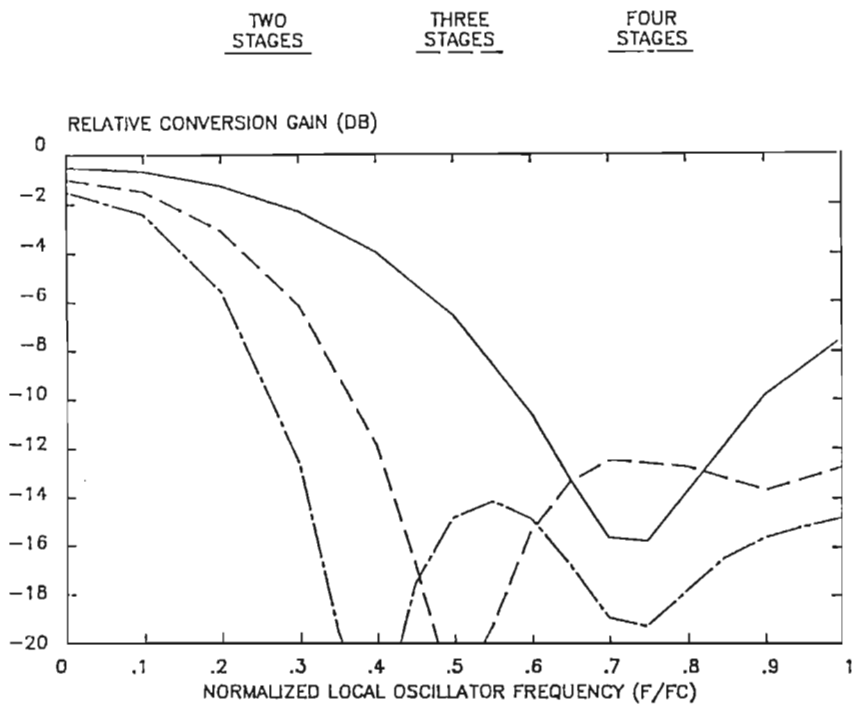


Figure 2.29. Relative Conversion Gain of a Three-Port Mixer as a Function of Normalized Local Oscillator Frequency, R_g = 10Ω, R_d = 300Ω, f(if) = difference frequency.

Section 2.C. Feedback Oscillator

The travelling-wave amplifier can be made into an oscillator by placing a frequency selective circuit between the input and the output [21,22].

The feedback circuit can be represented by the block diagram in Figure 2.30 where

$$G_{23} = \frac{V3}{V2} \quad , \quad G_{34} = \frac{V4}{V3}$$

and V2=V1+V4. Defining G_{13} as V3/V1 and substituting

$$G_{13} = \frac{G_{23}\ V2}{V1} = \frac{G_{23}\ V2}{V2-V4} = \frac{G_{23}}{1-G_{23}G_{34}} \qquad \text{eq.(2.40)}$$

the circuit is then an oscillator when $G_{23}G_{34}=1$.

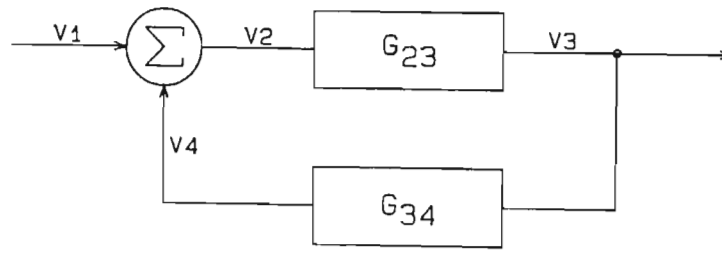


Figure 2.30. Feedback Circuit

Let the feedback component be an LC series tuned circuit with loss component R (Figure 2.31) so that in the complex frequency plane

$$Z(s) = \frac{1}{sC} + sL + R$$

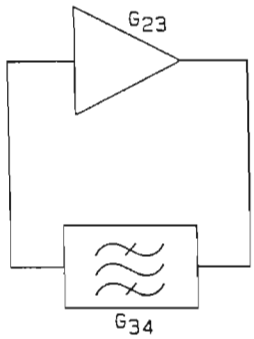


Figure 2.31. Simple Oscillator

The voltage ratio from the input to output terminal of the feedback section is then

$$G_{34} = \frac{R_L}{Z(s) + R_L} = \frac{sCR_L}{s^2LC + sRC + sR_LC + 1} \qquad \text{eq.(2.41)}$$

where R_L is the loading on the output of the G_{34} circuit. If $G_{23} = K$ then

$$G_{13} = \frac{K}{1 - \dfrac{ksCR_L}{s^2 LC + sRC + sR_LC + 1}} \qquad \text{eq.(2.42)}$$

.

For steady state oscillation the poles of G_{13} must lie at $\pm j\omega$

$$\text{so} \quad s^2 + \frac{sC(R+R_L) - sKCR_L + 1}{LC} = s^2 + \omega^2 \qquad \text{eq.(2.43)}$$

Equating like powers of s yields $\dfrac{C(R+R_L) - KCR_L}{LC} = 0$

and $\omega^2 = \dfrac{1}{LC}$

then $(R+R_L) = KR_L$ so $K = \dfrac{R+R_L}{R_L} = 1 + \dfrac{R}{R_L}$.

The circuit will then oscillate when losses within the circuit are overcome by the gain of the amplifier. Upon startup the poles of G_{13} will lie well into the right hand plane. As the level of the oscillation increases the amplifier will begin to saturate thus reducing the gain until a steady state condition with the poles on the j-axis has been reached.

This condition causes the amplifier to swing into very nonlinear regions of operation. The author has included a limiter in the feedback loop as shown in Figure 2.32. This reduces the loop gain as oscillations build but does not allow the amplifier to swing into extremely nonlinear regions.

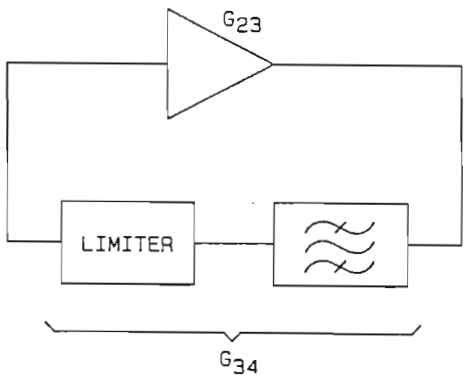


Figure 2.32. Oscillator with Non-Saturating Amplifier

An oscillator has now been made from the distributed amplifier (Figure 2.33). A local oscillator voltage is effectively applied to the gate line by the oscillator feedback path. Two ports remain unused for the introduction of a signal and the extraction of the mixer products.

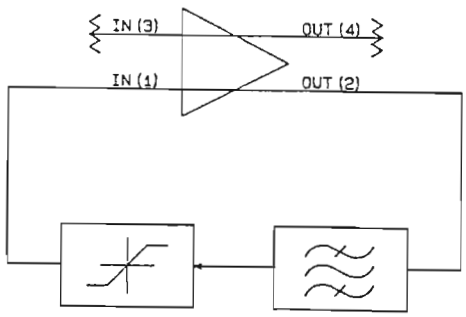


Figure 2.33. Non-Saturating Travelling-Wave Distributed Oscillator

Section 2.D. Travelling-Wave Frequency Conversion

The travelling-wave amplifier can be made to oscillate in a controlled manner such that an optimum local oscillator level is returned to the gate line along with a signal frequency from the opposite end of the gate line causing an intermediate frequency signal to be generated in the drain line. Comparable narrow band circuits have been implemented with single devices [23-25]. By controlling the level of the oscillation feedback component returned to the amplifier it is not driven into extreme nonlinear regions where the linear gain component is minimized [26].

An oscillator is made from a distributed amplifier by placing the feedback circuit between a drain output port and a gate input port as shown in Figure 2.34. Referencing Section 2.B, if the operating region of all active devices is maintained between the pinch off voltage and forward gate diode conduction the linear transconductance is

$$G_{amp} = k_0 + k_1 v_{gs} + k_2 v_{gs}^2 \qquad \text{eq.(2.44)}$$

and results in linear amplifier gain. The second order term

$$G_{mix} = (k_1 + 2 k_2 v_{gs}) e_{lo} \qquad \text{eq.(2.45)}$$

results in mixing of the local oscillator and signal frequencies. The bias and drive conditions establish the magnitude of amplifier and mixer gain.

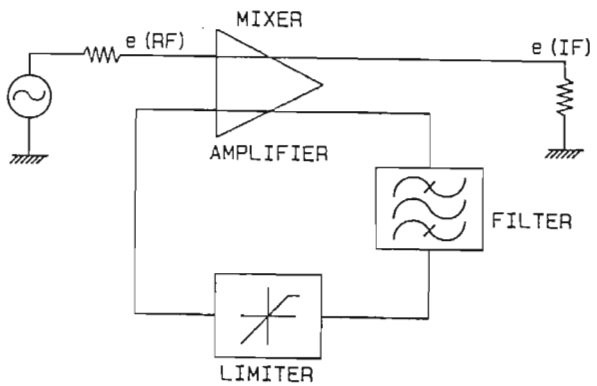


Figure 2.34. Non-Saturating Travelling-Wave Frequency Converter

The amplifier gain is a maximum at $V_{gs} = 0$ and a minimum at $V_{gs} = V_p$. The derivative of the mixer gain with respect to V_{gs} indicates a conversion minimum somewhere between $V_{gs} = 0$ and $V_{gs} = V_p$ with positive k_1 and k_2. The conversion maximum for this specific case ($k_2 > k_1$) occurs at approximately $V_{gs} = V_p$.

Maximum mixer conversion gain requires the maximum local oscillator drive level as G_{mix} is directly proportional to e_{lo}. With $k_2 > k_1 > 0$ maximum conversion gain occurs at V_p; however, allowance must be made for e_{lo} increasing the absolute peak value of V_{gs}. Linear transconductance G_{amp} must be reconciled with the bias point to establish if there is sufficient gain to allow oscillation with the feedback components to be used.

The limiting level of the feedback limiter will establish the local oscillator excitation. Separate setting of V_{gs} sets the operating point. If the optimum conversion transconductance bias point does not yield suitable linear gain then V_{gs} will have to be increased (less negative) and the local oscillator level decreased to prevent forward gate conduction.

For matched impedance RF input and IF output ports and flat frequency response diplexing filters are required at the oscillator end of the gate and drain lines to properly terminate the signal (RF input) and the IF output respectively. If this is not done the feedback filter reflects all incident waves not in the passband. If the gate and drain lines are considered lossless then twice the normal voltage can appear on the gate (resulting in a 6 dB increase) and all IF current on the drain can be reflected to the IF load where it can sum in phase. This circumstance can cause up to an apparent 12 dB increase in conversion gain. Conversely, if the voltages all interfere destructively, the conversion gain can go to zero. If the loading is not done through frequency selective elements the feedback filter is also loaded, increasing the loss in the feedback loop. This requires more gain to be added by the amplifier. This is done by increasing the gate voltage and thus generally decreases the

transconductance nonlinearity. Figure 2.35 is a block diagram for a travelling-wave frequency converter with gate and drain diplex filters.

The reflection of the signal (RF) back into the gate line modifies Equation 2.39 by the factor

$$\text{RF correction} = \rho(rf)\ \exp[2(n-m)\ \theta_d(lo) + \phi_R(rf)] + 1 \qquad \text{eq.(2.46)}$$

where $\rho(rf)$ is the magnitude of the reflection coefficient and $\phi_R(rf)$ is the phase of the reflection. The reflection of the IF voltage back into the drain line modifies the same equation by

$$\text{IF correction} = \rho(if)\ \exp[2(m-1)\ \theta_R(if) + \phi_R(if)] + 1 \qquad \text{eq.(II.D-4)}$$

where $\rho(if)$ and $\phi_R(if)$ are the magnitude and phase respectively of the reflection at port (4).

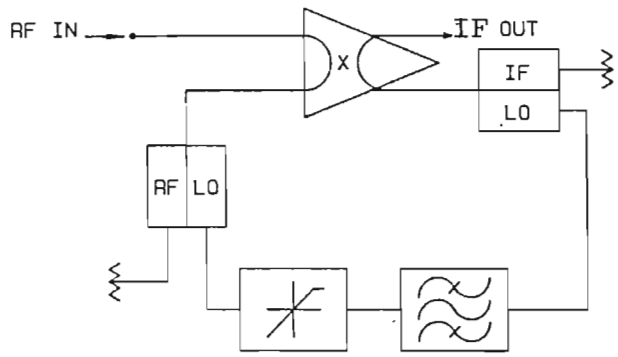


Figure 2.35. Travelling-Wave Frequency Converter with Gate and Drain Line Diplex Filters

The gate line losses present yet another problem. Assuming identical devices throughout the amplifier/mixer, as the signal progresses down the lossy gate line the LO excitation at each gate is reduced, thereby causing a rapid decrease in conversion gain with gate loss. This LO gradient can be compensated to some extent by increasing dG_{mix}/dv_{gs} of all devices [27] as the local oscillator voltage drops; however, this change in device characteristics will probably have to be accompanied by an increase in V_{gs} and this will complicate the bias circuit design.

CHAPTER 3

CIRCUIT DESIGN, FABRICATION AND TESTING

Design of a travelling wave frequency converter was undertaken to prove the concept that a readily integrable circuit can be configured to amplify, oscillate and mix simultaneously thereby ultimately reducing the size and cost of the functional block. This design was undertaken with discrete components realizing that the circuit performance would not be as good as that obtainable from an MMIC due to stray and parasitic elements. Fabrication was in soft board microstrip and strip bar.

Super-Compact* running on an HP9000 series 5000 was used extensively for transmission line computations as the subprogram "TRL" has both closed form and Bryant-Weiss [28] analysis capability. Touchstone** running on an HP9836C with a floating point processor was used for circuit analysis and optimisation after initial circuit analysis by the four-port program. The four-port program was originally run in C-Basic on a Z-80 based microcomputer to demonstrate that a complex circuit can be handled by the program on a small computer. The program was then moved to the HP9836C in HP-Basic for convenience. It was noted that a four stage distributed amplifier with parasitics could be analysed on the microcomputer (with 64K bytes total memory) but was too complex to be analysed on Touchstone with 1.9M bytes total memory. This is because the sequential analysis of cascaded circuits does not require the history or future of the analysis to be retained as the running wave-scattering matrix is continually updated.

Artwork was generated in any of three different ways:

(1) handcut rubylith on a manual coordinatograph
(2) laid out and photoplotted on a Gerber system
(3) rubylith cut on a standard Hewlett Packard plotter with a carbide tip "pen" driven from a Series 200 computer plot file.

* Trademark of Compact Software, Inc.
** Trademark of EESof, Inc.

Software to produce pattern generator files for the Hewlett Packard system was written by the author. Artwork photographic reduction was done on a 10X microelectronics reduction camera (375mm X 375mm working field) or a 5X MIC reduction camera (300mm X 500mm working field). The reduction was onto high resolution plastic negative processed lithographic film.

Rogers RT Duroid (relative dielectric constant of 2.2) was used for the microstrip circuits. Kodak KPR negative photoresist was used for circuit definition. The boards were spray etched in ferric chloride.

The HP8510 Automatic Network Analyzer was used extensively for both frequency and time domain analysis (reference Appendix E for Automatic Network Analyzer description). This instrument in the time domain mode was invaluable in locating unwanted discontinuties in the transistor test fixture (Appendix C) and in the PIN limiter (Section 3.C.1). Real time error corrected measurements in the frequency domain facilitated rapid dielectric resonator filter measurements (Section 3.C.2).

The HP8566 Spectrum Analyzer was used for mixer, oscillator and converter tests. A large spurious free dynamic range enabled accurate measurement of mixer products and oscillator spectra.

The following sections discuss the testing and correlation of test data to theory of a travelling-wave amplifier, oscillator, two-port mixer and three-port mixer. Also, the design and testing of components required to implement the TRAvelling-wave Frequency convERTER (filter and limiter) are covered. Finally, all the components are interfaced to yield the TRAVFERTER in Section 3.D.

Section 3.A. Amplifier

A three stage distributed amplifier was selected to demonstrate the travelling-wave frequency converter concept for two reasons. First, because of package parasitics the artificial transmission lines must have a lower cutoff frequency than would be required if the unpackaged transistor chips were used. Three stages then result in sufficient gain to demonstrate three-port mixing and non-saturating feedback oscillation. Secondly, with a constant impedance artificial line (required for maximum bandwidth) the signal voltage at the gate of successive stages is reduced by inductor and transistor gate losses. A point is reached where increasing the number of stages actually decreases gain.

The amplifier was designed before the transistor test fixture was completed; therefore, because of the differences between the manufacturer's data (averaged over many devices) and the data measured on a device from the same lot as used in the amplifier, there was some difference between the design performance and the actual performance.

The gate capacitance is about 0.6 pF. This results in a series inductor of [16]

$$L = Z_0^2 C = 1.5 \text{ nH} \qquad \text{eq.(3.1)}$$

for $Z_0 = 50\Omega$ in the gate and drain lines. This line has a cutoff frequency of

$$f_c = \frac{1}{\pi (LC)^{1/2}} \qquad \text{eq.(3.2)}$$

The inductors were made with one hundred ohm transmission lines (width of 0.7 mm on 0.787 mm RT Duroid). From Beyer et al [13] the length of the line is

$$l = \frac{Lc}{E_{eff} Z_0} \qquad \text{eq.(3.3)}$$

where c is the velocity of light and E_{eff} is the effective dielectric constant (about 1.88 for a 100Ω line on RT Duroid). The length of line

required is then 3.35 mm. The distributed capacitance of the transmission line is simulated as a lumped capacitance at each end of the line where

$$C = \frac{l\, E_{eff}}{2Z_0\, c} = 0.075 \text{ pF}.$$

This capacitance adds to the gate capacitance so an iteration is made to recalculate the inductance required after increasing the gate capacitance by 2 X 0.075 pF. The new inductance is 1.9 nH or 4.2 mm of 100Ω line. The line end capacitance is then 0.1 pF. The equivalent circuit for the three stage distributed amplifier is shown in Figure 3.1. The frequency response for this amplifier analysed with manufacturer's data is shown in Figure 3.2. The calculated response with the data from the device lot actually used is shown in Figure 3.3.

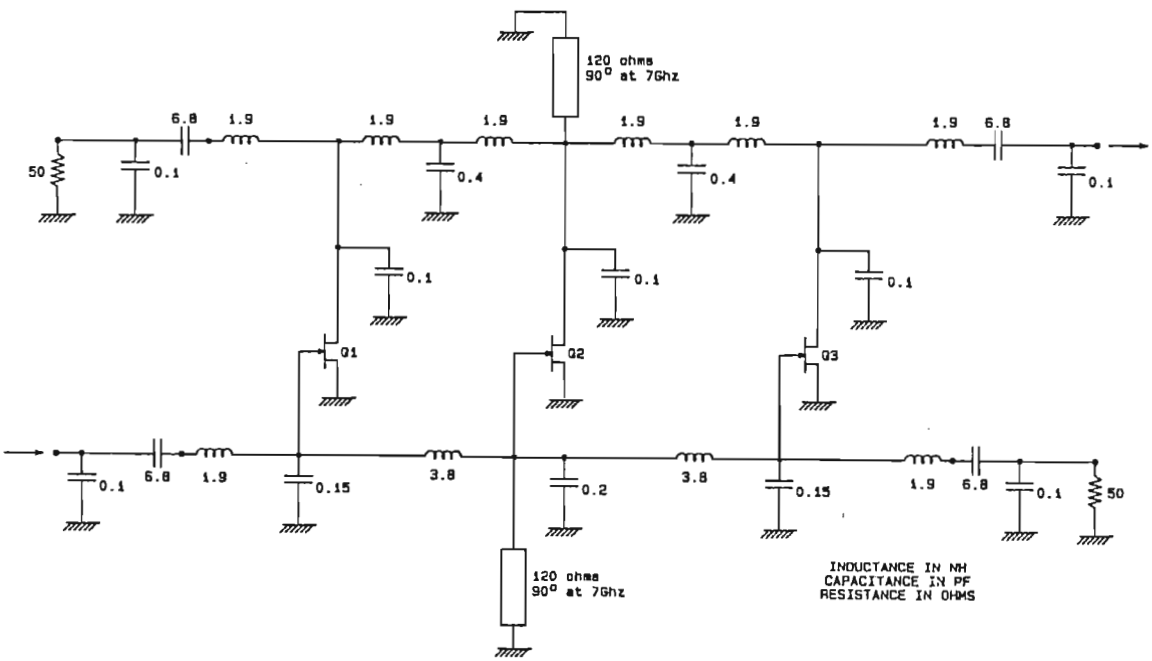


Figure 3.1. Three Stage Distributed Amplifier Equivalent Circuit

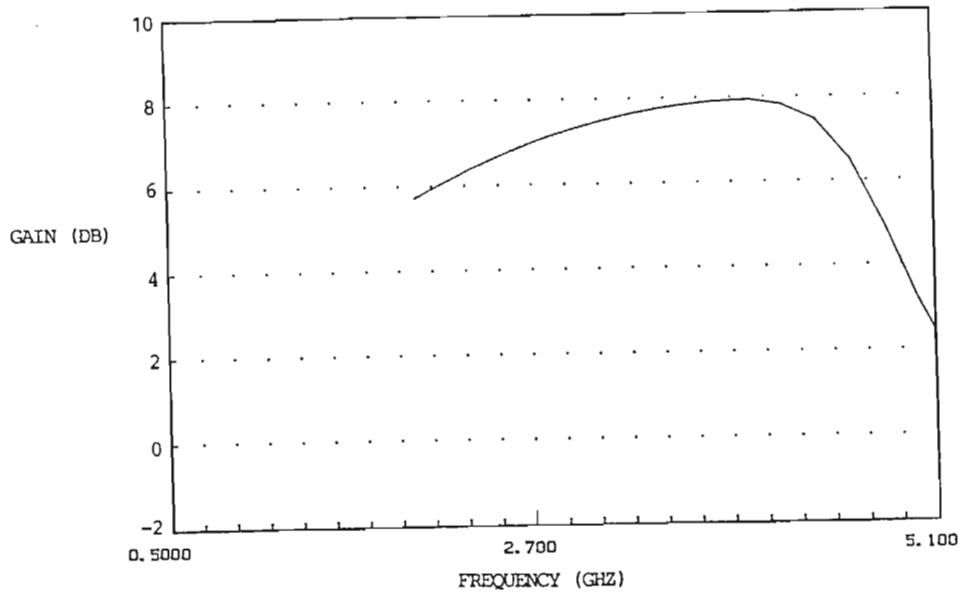


Figure 3.2. Amplifier Analysed with Manufacturer's Data (supplied from 2 to 12 GHz.)

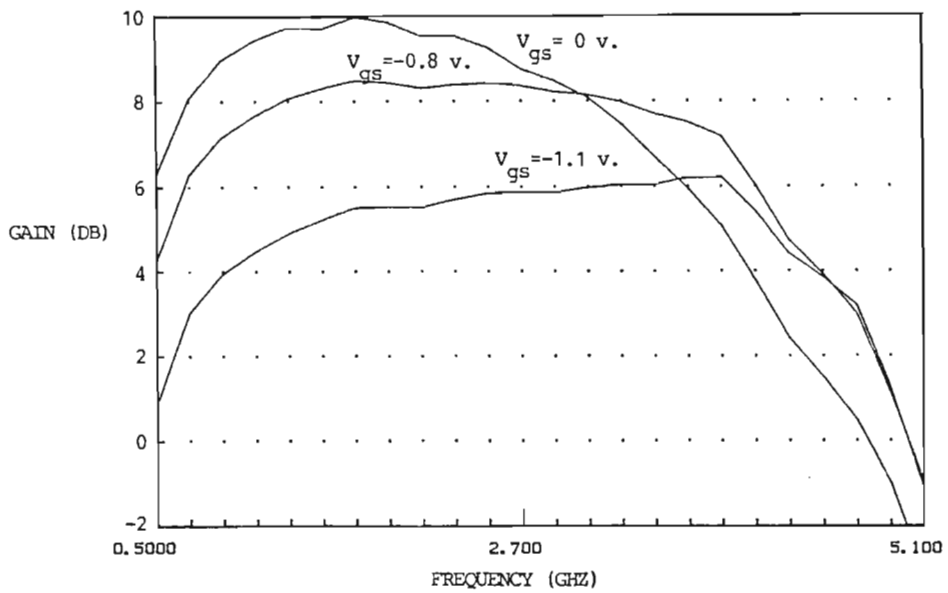


Figure 3.3. Calculated Response using Measured Data on the Device (measured device from same lot used to make the amplifier)

An optimum design for the measured data would have 2.75 nH inductors in the gate and drain because the gate capacitance is actually 1.1 pF. The computed frequency response for this amplifier is plotted in Figure 3.4. Note that there is not a considerable difference and, for the intended purpose, the amplifier will suffice.

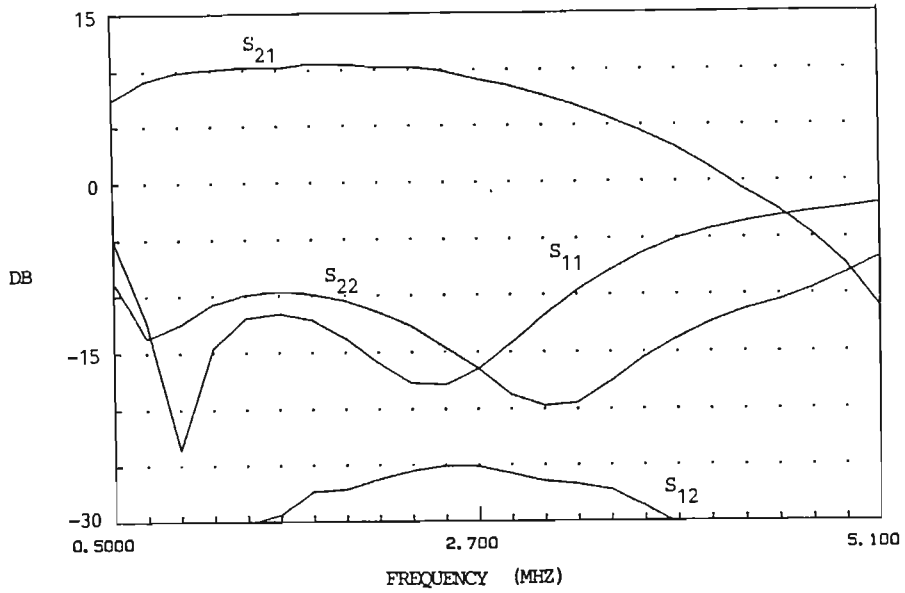


Figure 3.4. Calculated Response for Circuit Optimised to Measured Device Data

The amplifier was constructed on 0.254 mm (0.010 inch) RT Duroid. Initially quarter wave lines at 7 GHz were used for bias isolation; however, they were changed to quarter wave lengths of 40 gauge wire at 2 GHz to lower the low frequency cutoff of the amplifier. The input and output coupling is through chip capacitors. The amplifier was mounted in an aluminium package with SMA connectors and capacitive bias feed throughs as shown in Plate 3.1.

The computed response for the amplifier is plotted in Figure 3.5 for both port (1) to port (2) gain and port (1) to port (4) gain. The measured response for the same gains is in Figure 3.6.

The measured and computed gains correlate closely, especially in that the difference between S_{21} and S_{41} is almost identical at approximately ten dB at mid band. This indicates that the amplifier gate and drain lines are consistent and the transistors are reasonably well matched. The amplifier displays the expected gain characteristics of a three-port travelling-wave amplifier.

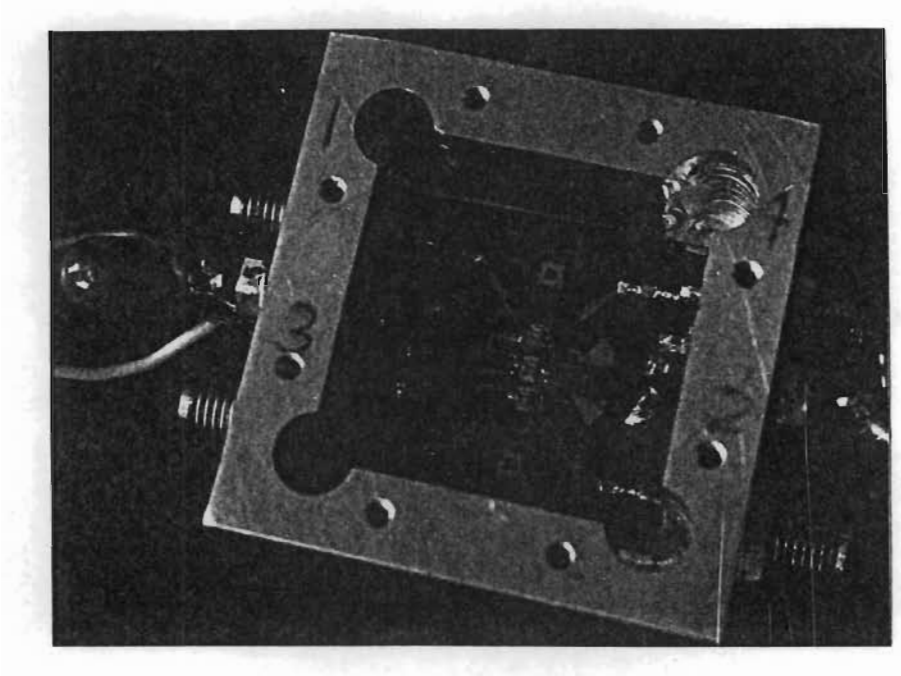


Plate 3.1. Three Stage Travelling-Wave Amplifier

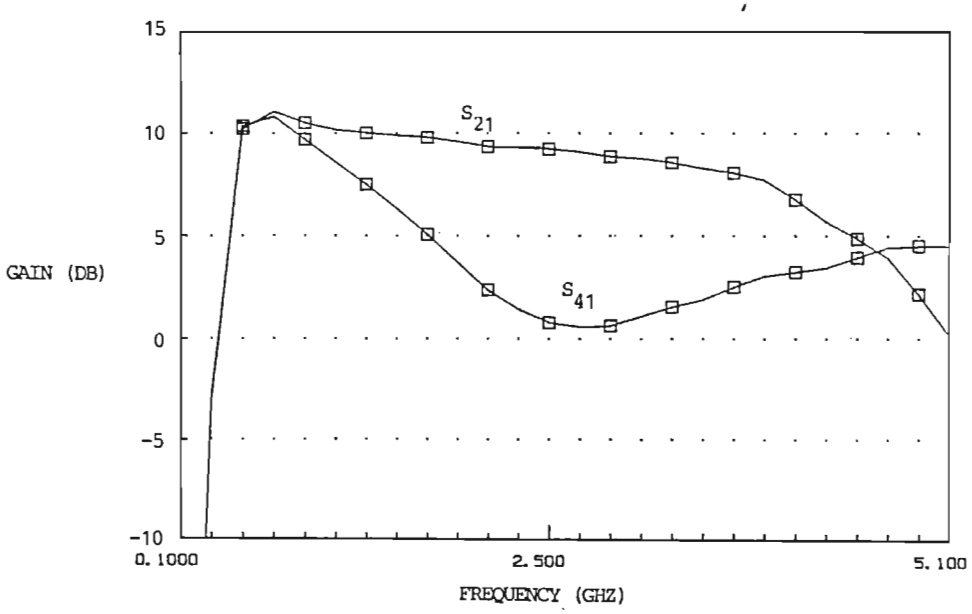


Figure 3.5. Computed Frequency Response for Three Stage Travelling-Wave Amplifier

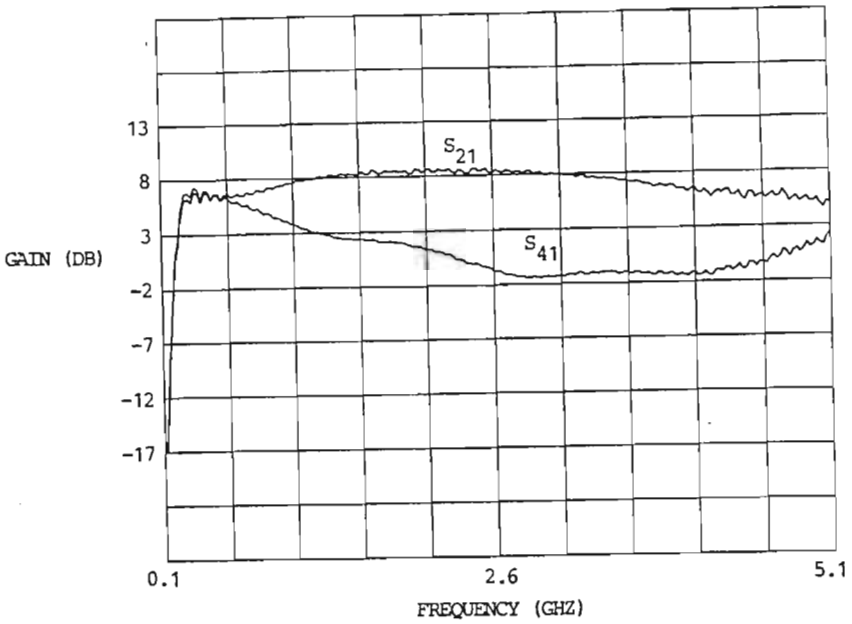


Figure 3.6. Measured Frequency Response for Three Stage Travelling-Wave Amplifier

As the ultimate goal is to operate the amplifier as a non-saturating oscillator in which the greatest gain is at $V_{gs} = 0$ and the best mixer performance is at $V_{gs} = V_p$ it is necessary to know the saturation and gain characteristics of the amplifier. The data for these parameters measured at two GHz are in Figures 3.7 and 3.8 respectively.

Even when operating at 2.5 volts V_{ds} the one dB compression point is 14 dBm output with $V_{gs} = -1.1$ volt. The measurement was made at -1.1 volt V_{gs} because, as indicated by the gain reduction curve, the amplifier still has a gain of almost five dB. It is anticipated that mixer loss will be acceptable at this bias with a few dBm of feedback (local oscillator) power in the converter.

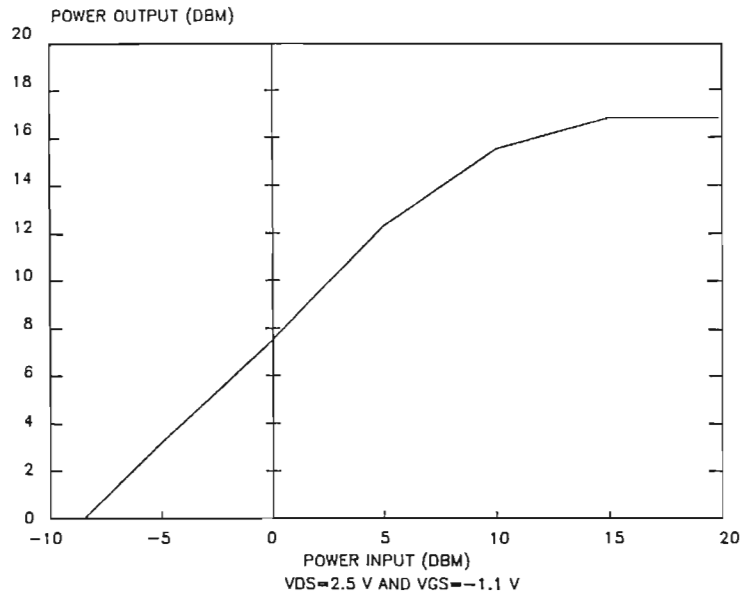


Figure 3.7. Measured Three Stage Travelling-Wave Amplifier Saturation Characteristic

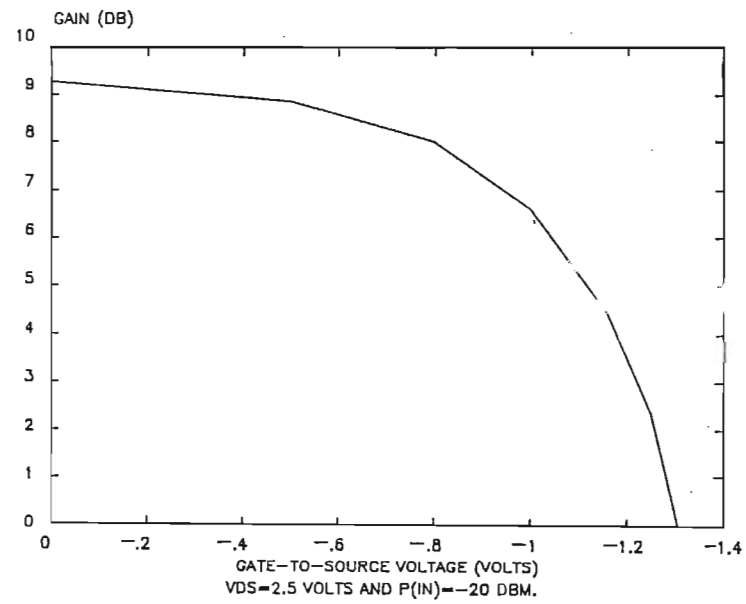


Figure 3.8 Measured Gain Reduction with Decreasing Gate-to-Source Voltage

Section 3.B. Mixer

The travelling-wave mixer is an amplifier with both a signal and a local oscillator voltage applied to the active devices. The primary difference between amplifier and mixer design is derived from changes in the FET parameters due to optimisation of bias voltages. Large amplifier gains are obtained with little negative bias on the FET gates; however, this is not a desirable bias point for mixer operation as it restricts the amplitude of the local oscillator voltage.

The design value of gate bias must be chosen to give moderate gain without allowing positive peaks of the local oscillator voltage to forward bias the gate diode. This premise will result in a maximum bias of about -0.3 to -0.6 volts for one to four milliwatts of local oscillator drive. Higher levels of local oscillator signal will result in greater non-linear products being generated in the individual devices; however, forward biasing the FET gates will cause excessive loss in the gate artificial transmission line thereby greatly reducing the amplifier and conversion gain. This is definitely not desirable if the amplifier/mixer is to be used at the same time as an oscillator. Decreasing the value of V_{gs} will also increase the level of nonlinear products and letting V_{gs} equal V_p will maximize conversion gain but the linear gain component will be reduced to the extent that simultaneous operation as an oscillator will not be possible.

The conversion gain was calculated using the measured FET data in Appendix C. The transconductance values were fitted to a third order curve

$$g_m\ (V_{gs}) = \sum_{m=0}^{3} k_m\ (V_{gs})^m \qquad \text{eq.(3.4)}$$

yielding $k_0 = 0.070$ S, $k_1 = 0.0369$ S/volt, $k_2 = 0.0315$ S/volt^2 and $k_3 = 0.0282$ S/volt^3. Referencing equation 2.32 the output voltage from an ideal two port mixer will be

$$e_n = n \cdot I_{IF} R_0/2.$$

The conversion gain for this case is

$$G_{conv} = 20 \cdot \log_{10}[n(k_1/2 + k_2 v_{gs}) \cdot e_{lo} \cdot R_0/2]. \qquad \text{eq.(3.5)}$$

This equation is plotted in Figure 3.9 for $R_0 = 50\Omega$, $e_{lo} = 0.32$ volts RMS (3 dBm into 50Ω) and n = 3.

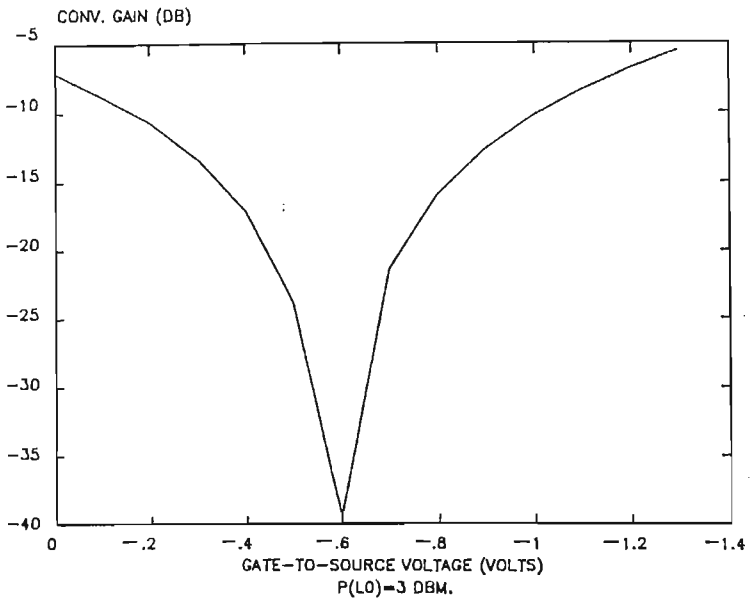


Figure 3.9 Calculated Two-Port Conversion Gain as a Function of Gate-to-Source Voltage, V_{VS}

Note that as the local oscillator drive is 0.45 volts zero-to-peak and V_p is -1.45 volts the curve is strictly correct only between -0.45 and -1.0 volts as other nonlinear effects influence conversion gain outside these limits; however, in the case of V_{gs} approaching V_p the increase in nonlinear effects is desirable as long as the linear gain can be maintained high enough to allow the converter to oscillate.

The primary importance of this graph is to stress salient points in the relationship between device nonlinear response and conversion efficiency. A conversion loss maximum occurs about 0.6 volts indicating maximum device linearity about that point. From this minimum point less conversion loss occurs as gate-to-source bias is reduced. At -1.2 volts equation 3.5 indicates a conversion loss of -7 dB. Both loss maximum and loss at -1.2 volts correspond reasonably with the measured results in

Figure 3.10 where the maxima occurs around -0.6 volt and -1.2 volt loss is about 4 dB. The reduction in conversion loss is due to nonlinear components other than transconductance (R_{ds}, C_{gs} and R_g) and especially to driving the gate beyond pinchoff. The general characteristics of the measured curve closely approximate the calculated values.

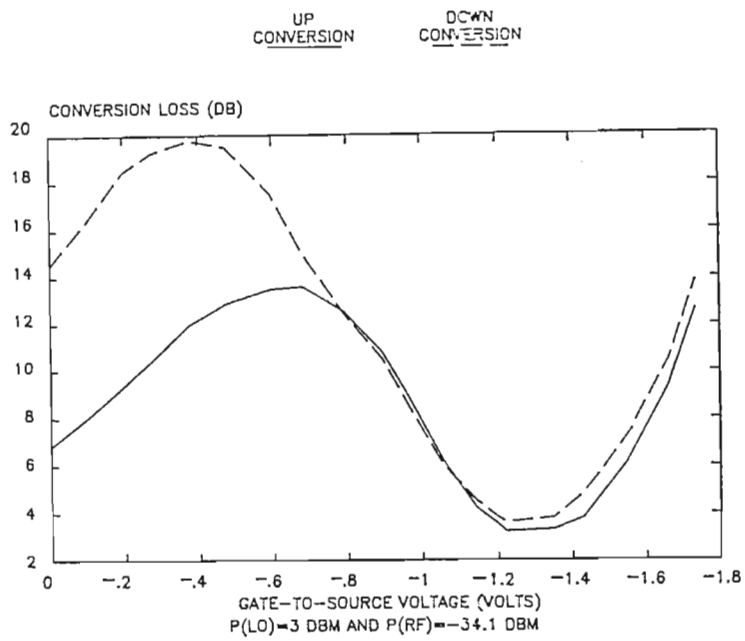


Figure 3.10. Measured Conversion Loss as a Function of Gate-to-Source Voltage for the Two-Port Mixer (local oscillator frequency = 2 GHz)

Conversion loss as a function of V_{gs} was also measured for the three-port mixer and is plotted in Figure 3.11. The data was measured at 2 GHz. That represents an ω_n of approximately 0.35. Referring to Figure 2.26 for a three stage mixer the conversion gain should be about 8 dB less than the conversion gain of a two-port mixer under similar operating conditions. The actual difference is 9 dB. Again, agreement with theory is very close.

Conversion loss varies with the level of the local oscillator. This relationship holds while the gate-to-source is within the bounds stated above. The gate was biased at -1.2 volts and the local oscillator power was varied. This is plotted against conversion loss for the two-port mixer in Figure 3.12. Under these conditions there is a straight line variation until the local oscillator power is about 0.25 volt zero-

to-peak voltage reducing the gate bias to -1.45 volts on negative voltage peaks; that is, conversion loss is reduced by increasing local oscillator power until the negative peak equals the pinchoff voltage. After that point is reached, little reduction in loss is possible unless the bias point is changed. The three-port mixer conversion loss follows the same pattern as shown in Figure 3.13.

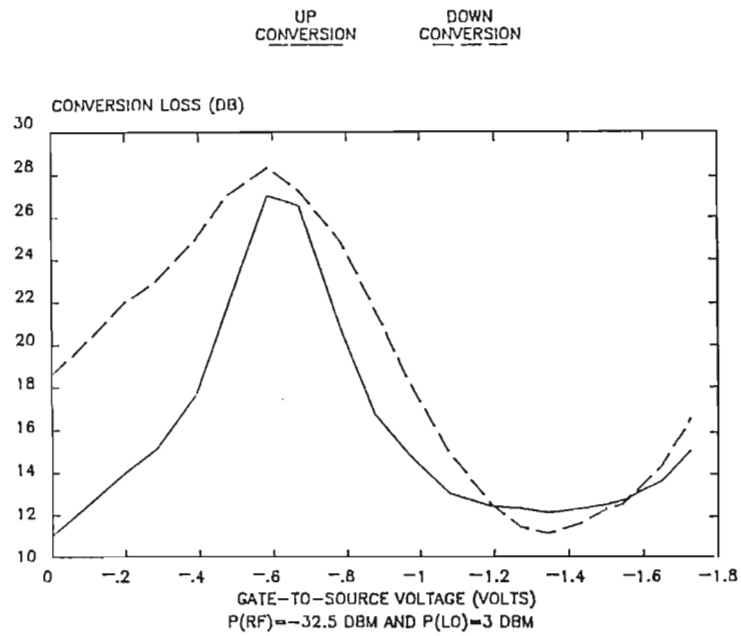


Figure 3.11. Measured Conversion Loss as a Function of Gate-to-Source Voltage for the Three-Port Mixer (local oscillator frequency = 2 GHz)

The primary difference between the two-port and three-port mixers as indicated by equations 2.32 and 2.35 to 3.37 is that the three-port mixer conversion loss is a function of local oscillator frequency. The three-port conversion loss was measured at various local oscillator frequencies with a low side RF signal and difference frequency IF. The result is plotted in Figure 3.14 where 2.6 GHz corresponds to approximately $\omega_n = 0.45$. Comparison of this curve with the three stage computed data in Figure 2.29 shows good agreement between the experimental data and theory.

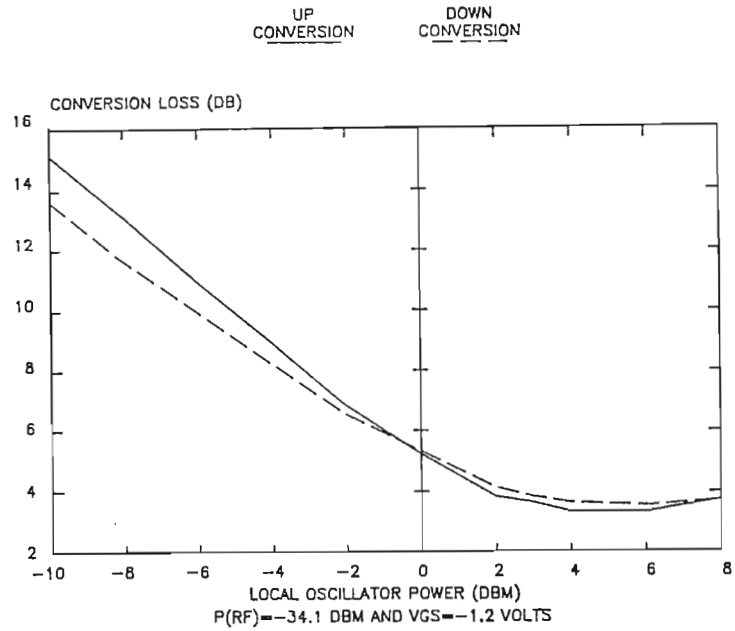


Figure 3.12. Measured Conversion Loss as a Function of Local Oscillator Power for the Two-Port Mixer (local oscillator frequency = 2 GHz.)

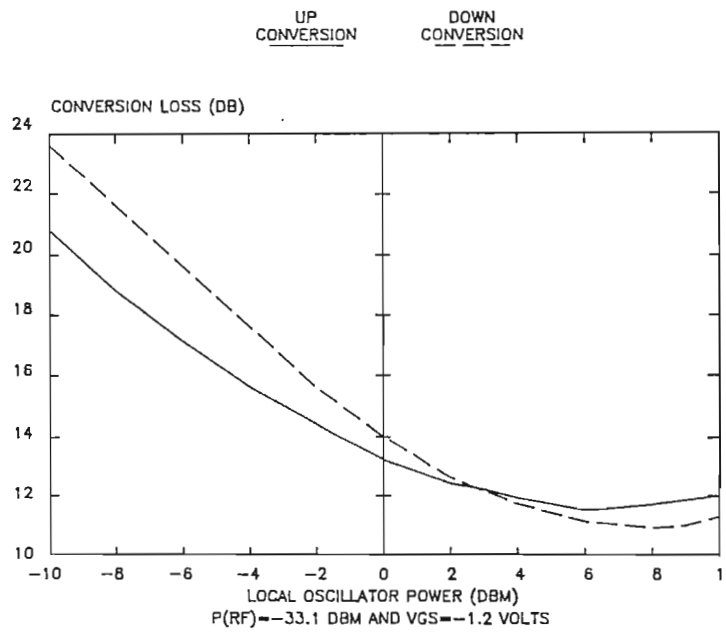


Figure 3.13. Measured Conversion Loss as a Function of Local Oscillator Power for the Three-Port Mixer (local oscillator frequency = 2 GHz.)

The computed conversion gain relative to a two port mixer is -1.5 dB at zero local oscillator frequency indicating an expected 5.5 dB conversion loss. This compares favorably with the 7 dB in Figure 3.14. The remainder of the measured curve also fits the theory.

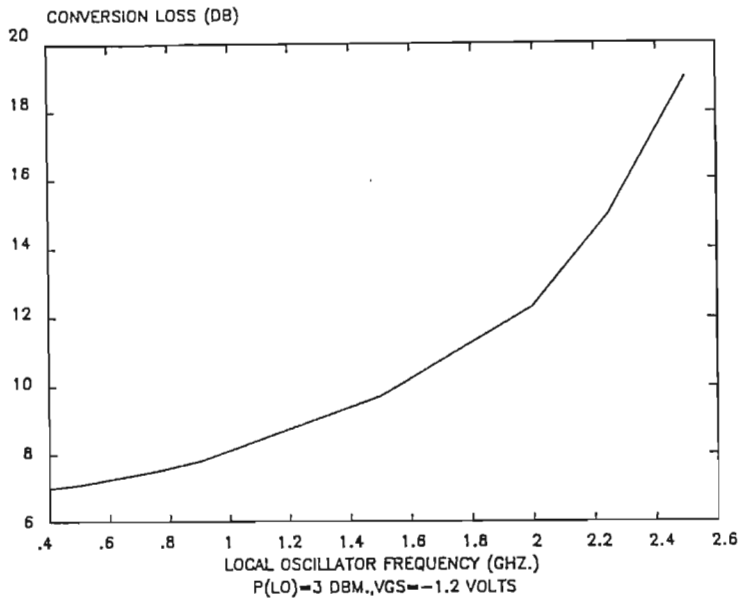


Figure 3.14. Measured Conversion Loss as a Function of Local Oscillator Frequency for the Three-Port Mixer

Conversion gain as a function of RF signal frequency was measured for fixed IF frequencies. In Figure 3.15 the data for a local oscillator frequency of 900 MHz is plotted against an RF signal input of 1 to 3.2 GHz. This indicates IF frequencies of 1.9 to 4.1 GHz for up conversion and 300 MHz to 2.3 GHz for down conversion. Note that as the IF approaches low frequency cutoff for the mixer (about 300 MHz) the conversion gain decreases and as the IF approaches the high frequency cutoff the gain also decreases. A nominal value of 8 dB of conversion loss is obtained at a 900 MHz local oscillator frequency with -1.2 volts of gate bias and 3 dBm of local oscillator power. Similar results are obtained at a local oscillator frequency of 1.5 GHz (Figure 3.16) where a nominal value of conversion loss of 11 dB is measured. The data is in good agreement with the theory.

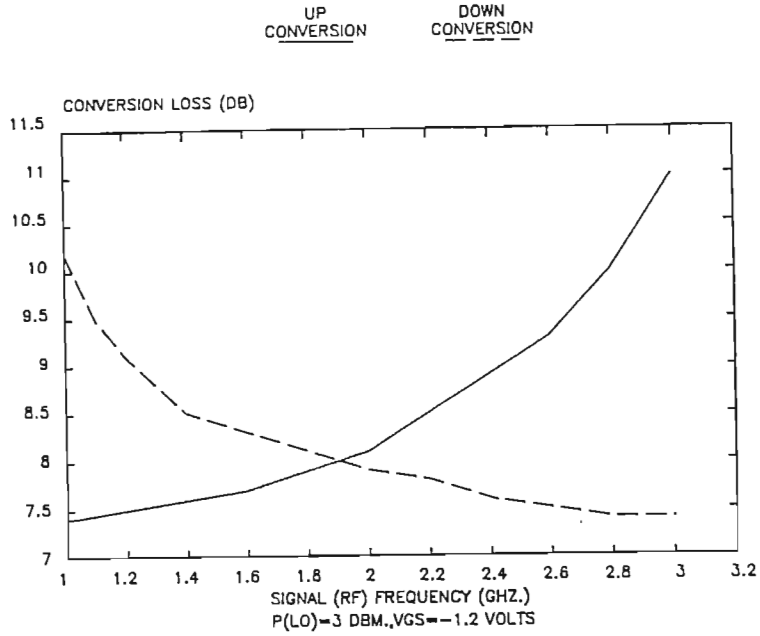


Figure 3.15. Measured Conversion Loss of a Three-Port Mixer as a Function of Signal (RF) Frequency at a Local Oscillator Frequency of 0.9 GHz

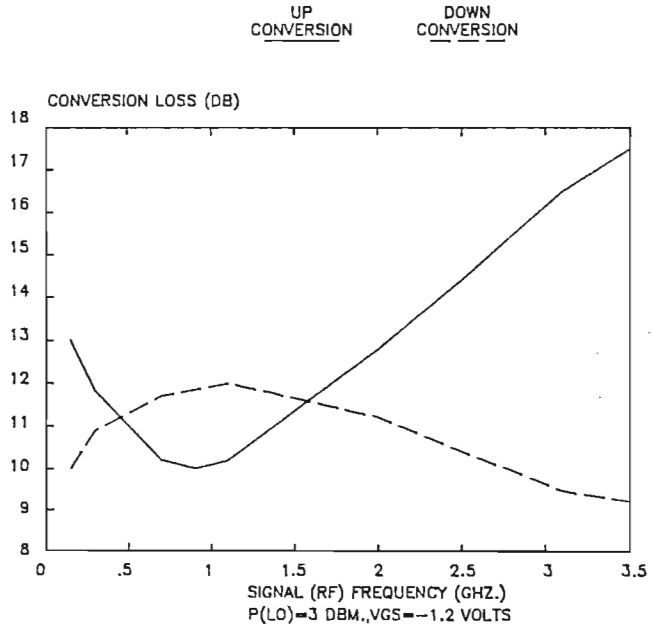


Figure 3.16. Measured Conversion Loss of a Three-Port Mixer as a Function of Signal (RF) Frequency at a Local Oscillator Frequency of 1.5 GHz.

Section 3.C. Feedback Oscillator

Design of the oscillator consisted of specifying and designing feedback components compatible with the amplifier/mixer. These feedback components were to provide frequency selectivity with only a moderate loss and to limit the power fed back into the amplifier/mixer input to a level yielding good mixing. The feedback components are then a filter and a power limiter.

Section 3.C.1. Limiter

A power limiter is required to provide the gain versus power reduction in the feedback loop of the oscillator to prevent the amplifier from being driven into extremely nonlinear operating regions. These regions are (1) extremely negative gate bias so that loop and amplifier gain is excessively reduced and (2) forward biasing the gate diode.

Two types of power limiting were considered. These were diode clipping and PIN diode limiting. Diode clipping (Figure 3.17) limits average power on a cycle-to-cycle basis. As any voltage across the diode exceeds the built-in potential the diode conducts, hence reflecting the excess voltage. This method is very fast but introduces considerable nonlinearity into the circuit. This can cause problems in the mixer mode when both signal and local oscillator voltages appear across a diode and generate products that can then sum vectorally with products from the mixer.

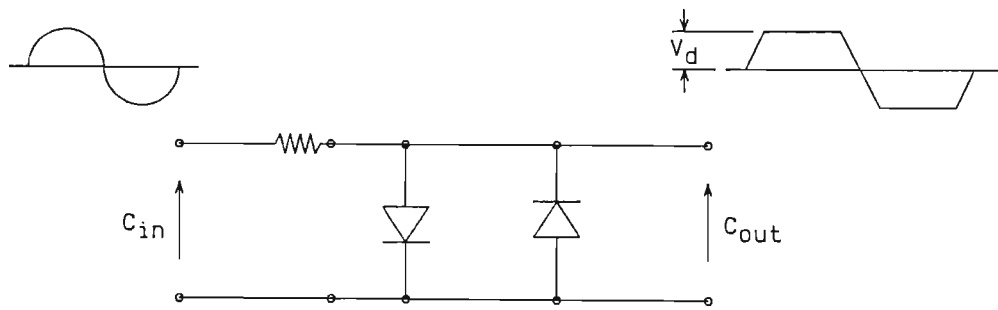


Figure 3.17. Schottky Diode Clipper

Reflective PIN limiting (Figure 3.18) attacks rapidly as the initial mode of operation is as a diode. Current i_d flows in the diode from an overvoltage $v_f > v_d$ thus lowering the resistance. This is where the similarity to a diode clipper ends. As the potential is reversed the PIN diode retains a low resistance as the carriers previously generated cannot be quickly removed because they have a very long life time in the intrinsic region. The impedance measured across the PIN diode as a function of current is resistive. This type of limiter will then limit current without introducing excessive higher order products or reactive mistuning.

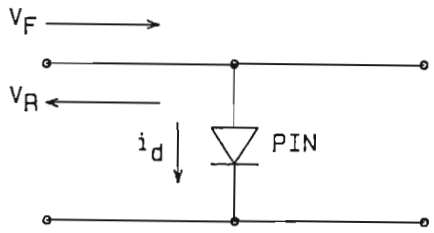
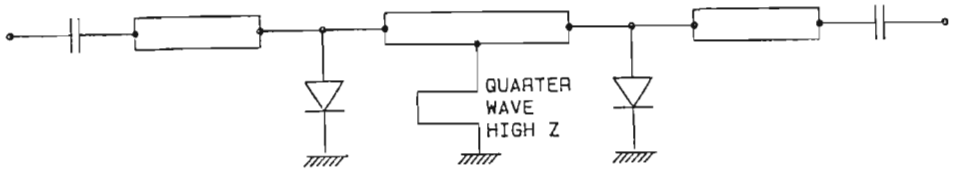


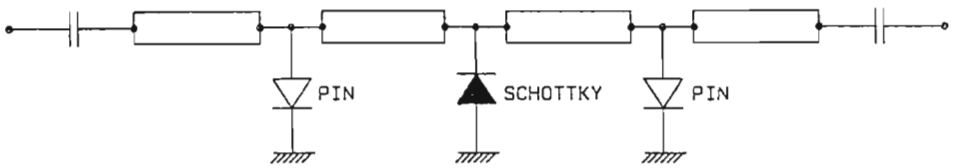
Figure 3.18. Reflective PIN Diode Limiter

Two types of PIN limiter were constructed. The first was the shunt diode limiter operating from its own bias generated from overvoltage rectification. This is shown in Figure 3.19a. The second type, Figure 3.19b, utilizes a Schottky barrier diode to rectify some of the overvoltage and the current then passes through the PIN diode to cause an increase in reflected power. The Schottky diode is not pushed far enough into conduction to cause excessive mixing products. This limiter operates at a much lower level than the straight PIN limiter as the Schottky barrier potential is less than the PIN barrier potential.

The limiter was constructed in strip bar (Plate 3.2) because radial lead glass packaged diodes were used. The packages were 3.8 mm (0.15 inches) long so the transmission line was constructed 3.8 mm above the ground plane. The transmission line material was 0.25 mm. copper sheet. The line was first constructed without the diodes inserted and checked on the HP8510 automatic network analyser in the time domain mode. This graphically illustrated the discontinuities at the SMA connector to strip bar transitions.



(a) Self Bias



(b) Schottky Diode Detector Bias

Figure 3.19. Transmission Line PIN Diode Limiters

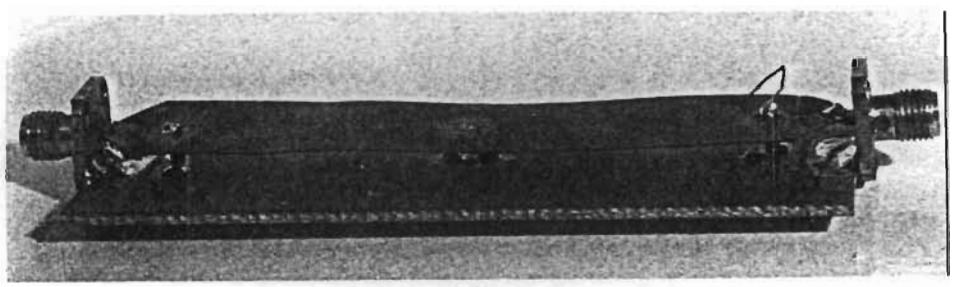


Plate 3.2. Strip Bar PIN Limiter

The result of the time domain measurement is shown in Figure 3.20 The two peaks are reflections from the connector-to-line discontinuities. The magnitudes of the reflections are 0.08 and 0.10 relative to a normalised incident step function. Figure 3.21 is the frequency response of the strip bar transmission line. The S_{11} curve indicates a return loss of only 11 dB at 2 GHz with a transmission loss S_{21} of 0.71 dB.

The diodes were then mounted between the strip bar and the ground plane close to the connectors. This increased the reflections. The bars were shaped at the connector transitions to reduce the local capacitance and increase the inductance depending upon the PIN diode to introduce compensating capacitance. The resulting inductance and lumped shunt capacitance results in a low pass filter section. The tuning was done while observing the results on the HP8510.

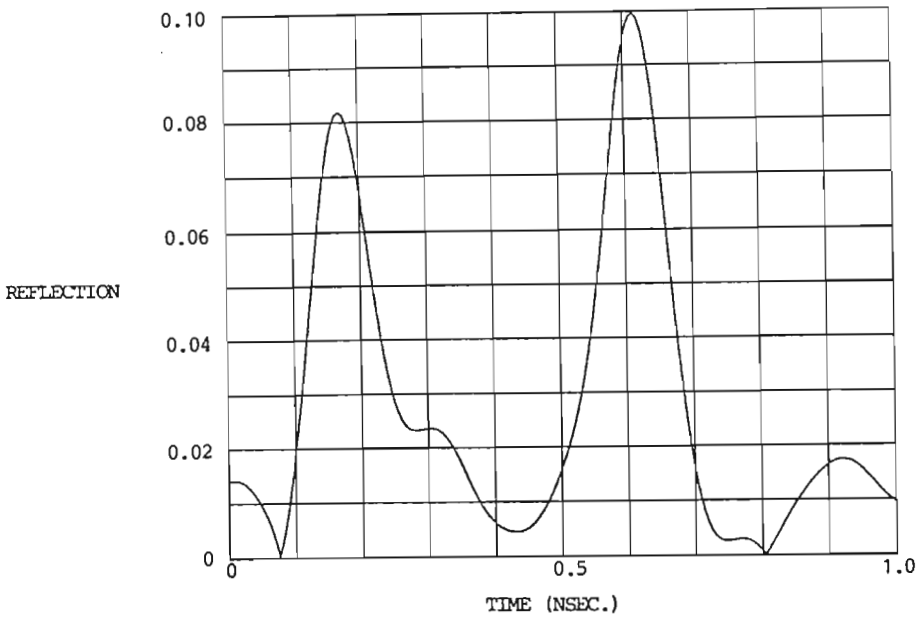


Figure 3.20. Measured Time Domain Reflection Response of Strip Bar Transmission Line Before Tuning

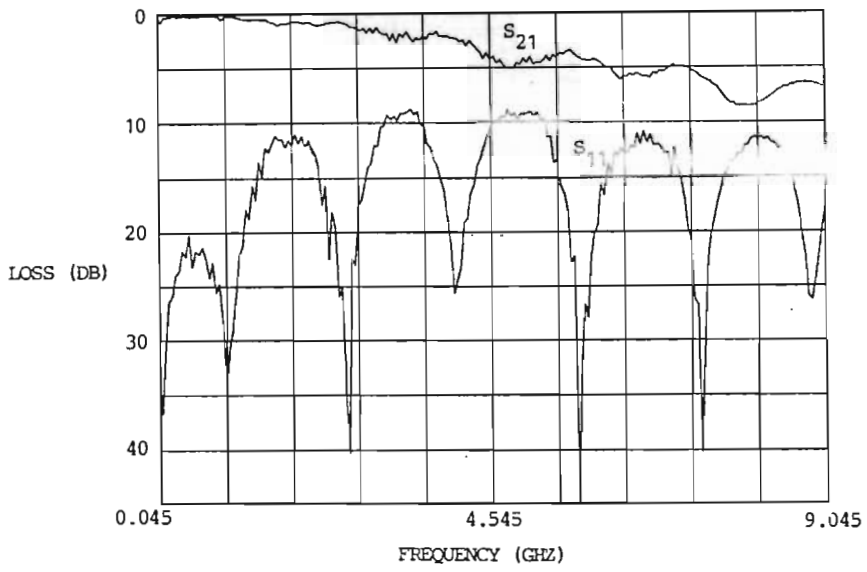


Figure 3.21. Measured Frequency Domain Transmission and Reflection Response of Strip Bar Transmission Line Before Tuning

The result of the final adjustment is shown in Figure 3.22. The large return (4.5 percent of the incident amplitude) is due to the first low pass section reflecting the majority of the incident high frequency power above the cutoff frequency and is entirely acceptable. The standing

wave ratio S_{11} from the limiter as shown in Figure 3.23 is less than 1.2 up to about 3 GHz. This represents a reasonable return loss of less than -20 dB. Figure 3.24 shows that the transmission loss even with the diodes mounted is less than the reduction of the mismatch loss.

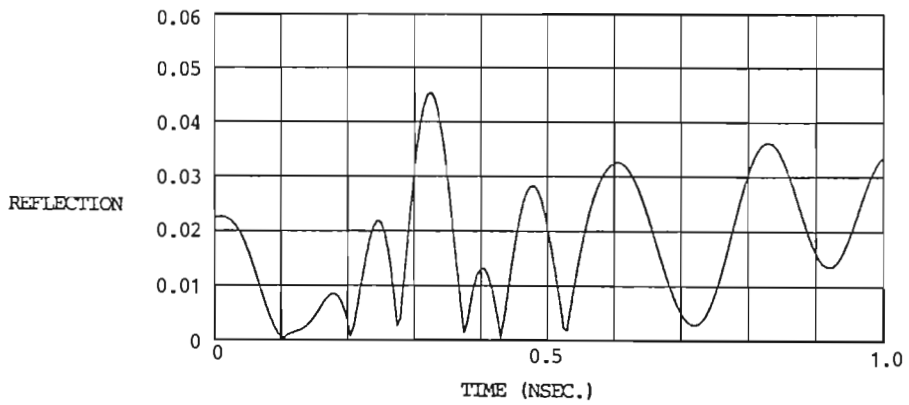


Figure 3.22. Measured Time domain Reflection Response of PIN Diode Limiter After Tuning

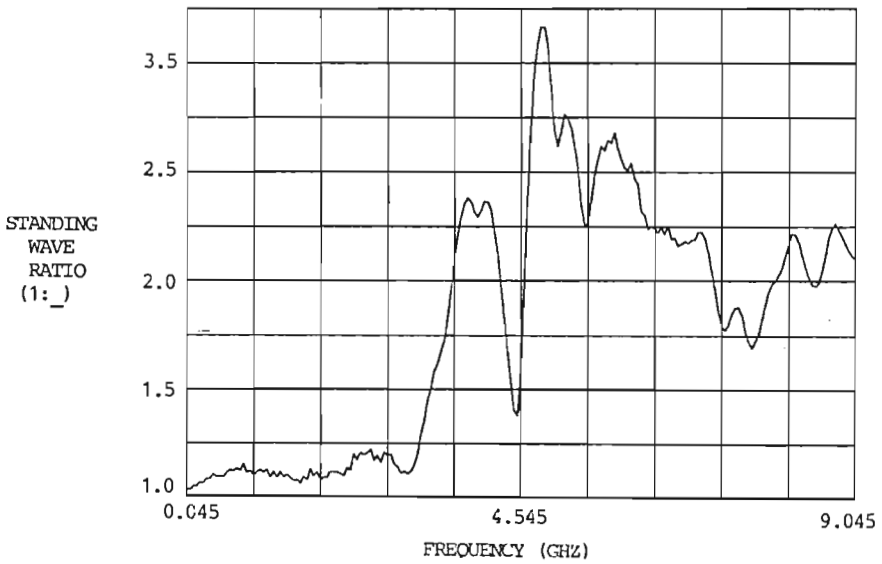


Figure 3.23. Measured Standing Wave Ratio of PIN Diode Limiter After Tuning

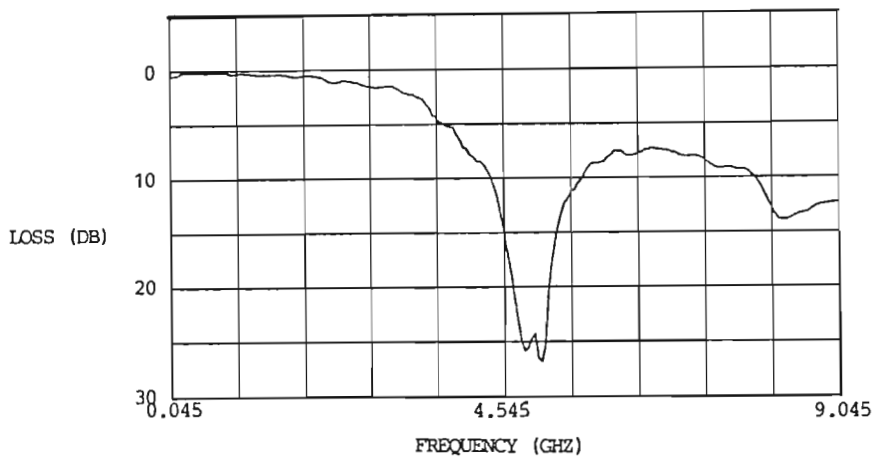


Figure 3.24. Measured Transmission Frequency Response for PIN Diode Limiter After Tuning

Time domain reflectometry (TDR) with the HP8510 is unique when compared with conventional TDR in that level sensitive components such as the PIN limiter can be tested without introduction of relatively large test signal levels. As the HP8510 computes the time response from discrete frequency measurement of amplitude and phase responses, large dynamic range measurements are made while never applying more than a -10 dBm (in this case) signal to the device under test. A conventional TDR test set would apply a very short rise time pulse with voltages large enough to affect the diodes if sufficient high frequency energy is to be introduced to obtain reasonable temporal resolution.

The output power as a function of input power of the limiter measured at 2 GHz is shown in Figure 3.25. The effective limiting level is just over 4 dBm and it displays a gain reduction of 5 dB for a 10 dBm input. Hard limiting is obtained above about 8 dBm input.

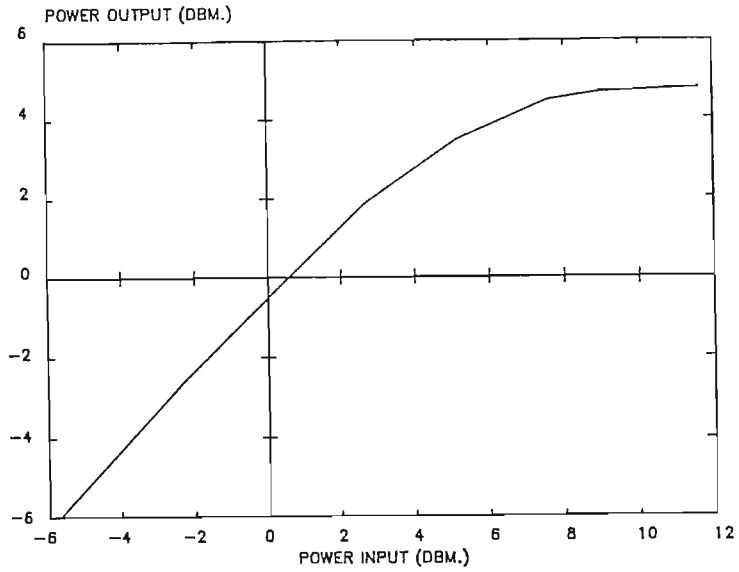


Figure 3.25. Measured Limiter Power Transfer Characteristic

Section 3.C.2. Filter

Virtually any two-port frequency selective device will work as an oscillator filter. The required specifications are that the insertion loss be low enough to allow all loop components to have a total gain greater than one and the selectivity be great enough to define the oscillation frequency. The stability must be compatible with the application.

A two gigahertz dielectric resonator was used for the feedback filter [29]. A microstrip fixture with orthogonal fifty ohm transmission lines was constructed in 0.062 mm (1.57 inches) Duroid with SMA connectors. A photograph of the fixture is shown in Plate 3.3. The fixture was configured to allow each line to be terminated in fifty ohms so that off resonance a proper termination is seen at each port. After testing of the dielectric resonator and finding the desired resonator position on the fixture the lines were open circuited a quarter of a wavelength away from the tangent point of a concentric circle about the center of the resonator puck. The measured frequency and phase response of the filter are shown in Figure 3.26. The filter has a nominal insertion loss of 1.5 dB and a 3 dB bandwidth of 15 MHz representing a loaded Q of well over one hundred. By carefully cutting the stubs and tuning, an insertion loss of 0.7 dB was measured.

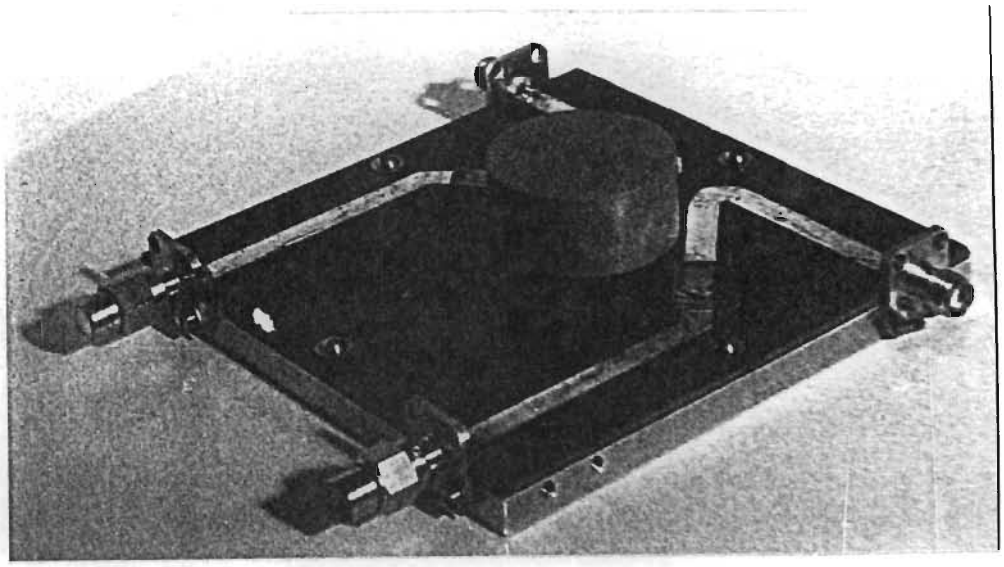


Plate 3.3. Dielectric Resonator Filter

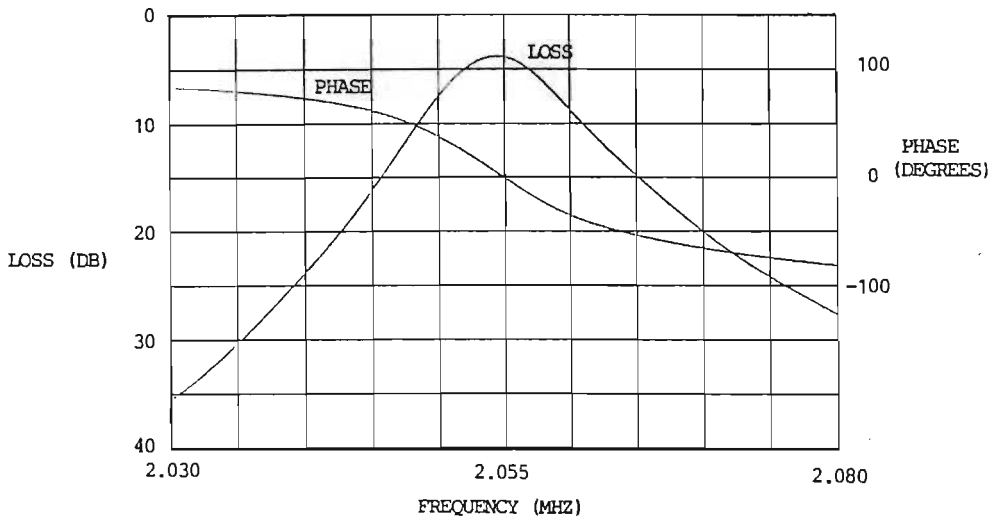


Figure 3.26. Measured Frequency Response of Dielectric Resonator Filter

Section 3.C.3. Oscillator

The components of the oscillator were interconnected with semi-rigid coaxial cable as shown in Figure 3.27. A 10 dB directional coupler was inserted within the loop to provide a sample of the oscillation for power measurement and spectral analysis. The coupler was placed at the input of the amplifier as the signal level at that point determines if the amplifier will be in saturation.

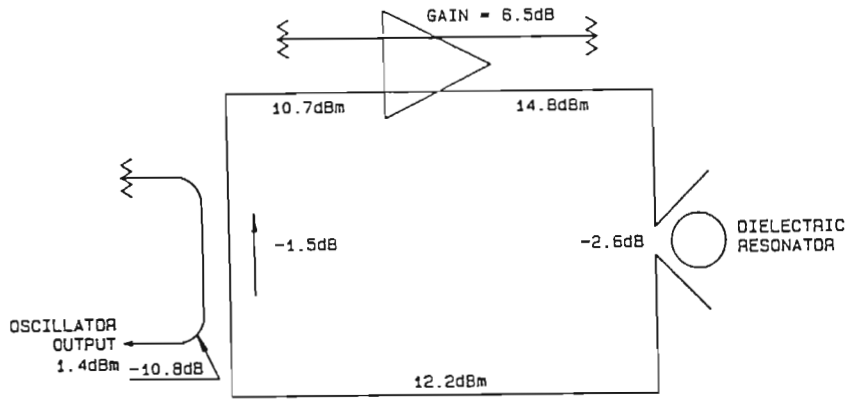


Figure 3.27. Travelling-Wave Feedback Oscillator (without limiter)

The oscillator was first connected without the limiter to simulate a normal oscillator configuration (Figure 3.27). The gate-to-source voltage was set at -1 volt to ensure that the gate inputs would not approach V_p or forward bias. Gain and saturation data for this bias point are contained in Figures 3.7 and 3.8. Non-saturating amplifier gain at this bias is nominally 6.5 dB. Just prior to oscillator testing, the filter loss was measured to be 2.6 dB as the dielectric resonator had been moved and the filter retuned since the measurements in Section 3.C.2 had been made. The output power and spectrum were measured on a spectrum analyser. The analyser display is shown in Figure 3.28. Power levels within the loop are shown in Figure 3.27. The 1.4 dBm out of the coupler measured by the spectrum analyser indicates that the amplifier output level is 14.8 dBm and the input level is 10.7 dBm. Referring to the amplifier gain saturation characteristic in Figure 3.7 these power levels represent approximately a 2.5 dB amplifier gain reduction due to saturation. The product of gains and losses within the loop is unity.

The oscillator was then connected as shown in Figure 3.29 with the PIN diode limiter in the loop. The level measured out of the coupler as indicated in Figure 3.30 was -8.1 dBm. The amplifier input level is then 1.2 dBm and, again referencing Figure 3.7, the amplifier is operating in the linear region.

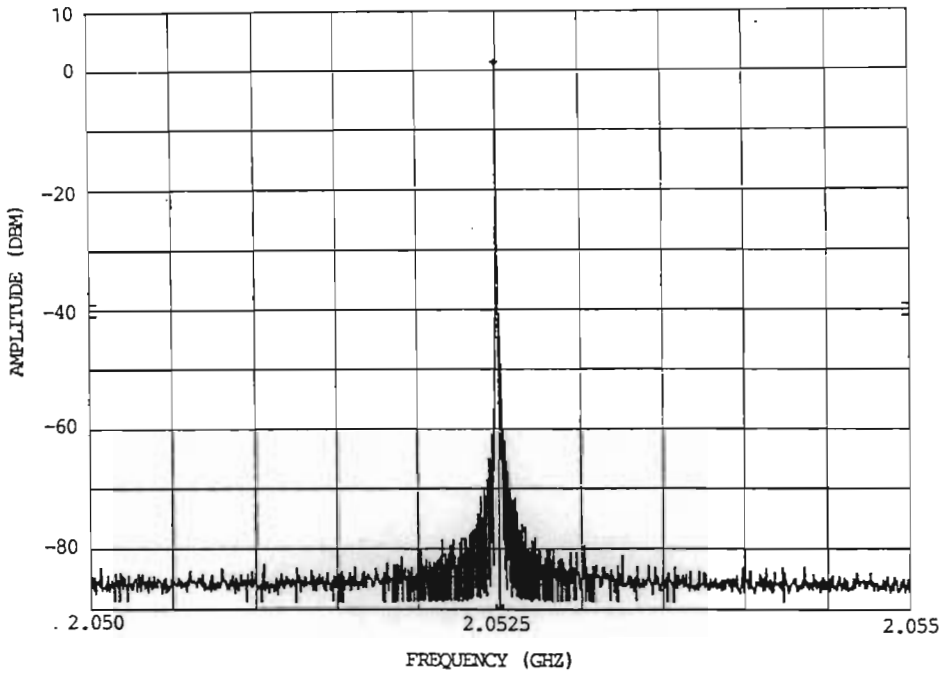


Figure 3.28. Measured Output of Travelling-Wave Feedback Oscillator (no limiter in feedback circuit)

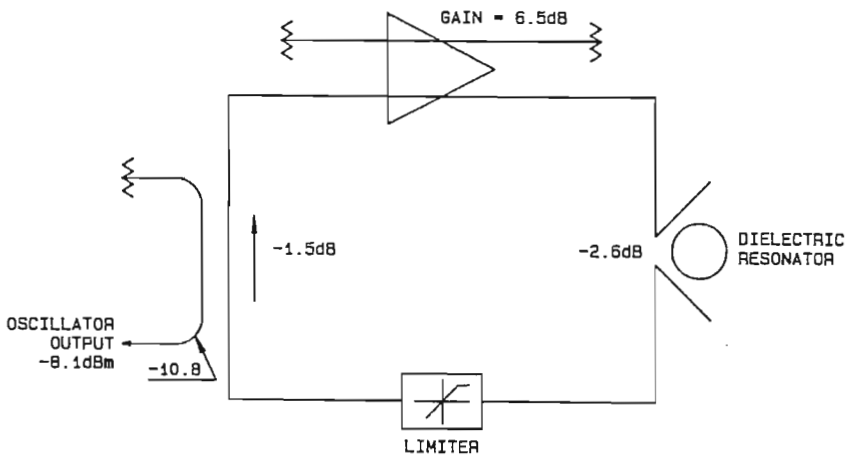


Figure 3.29. Travelling Wave Feedback Oscillator (with limiter)

The amplifier output is 7.7 dBm. In order for the loop gain to drop to unity the limiter must supply 2.4 dB of loss. Referring to Figure 3.25, a 5.1 dBm limiter input results in approximately a 2.5 dBm output or 2.6 dB of loss. All gains and losses within the loop are accounted for.

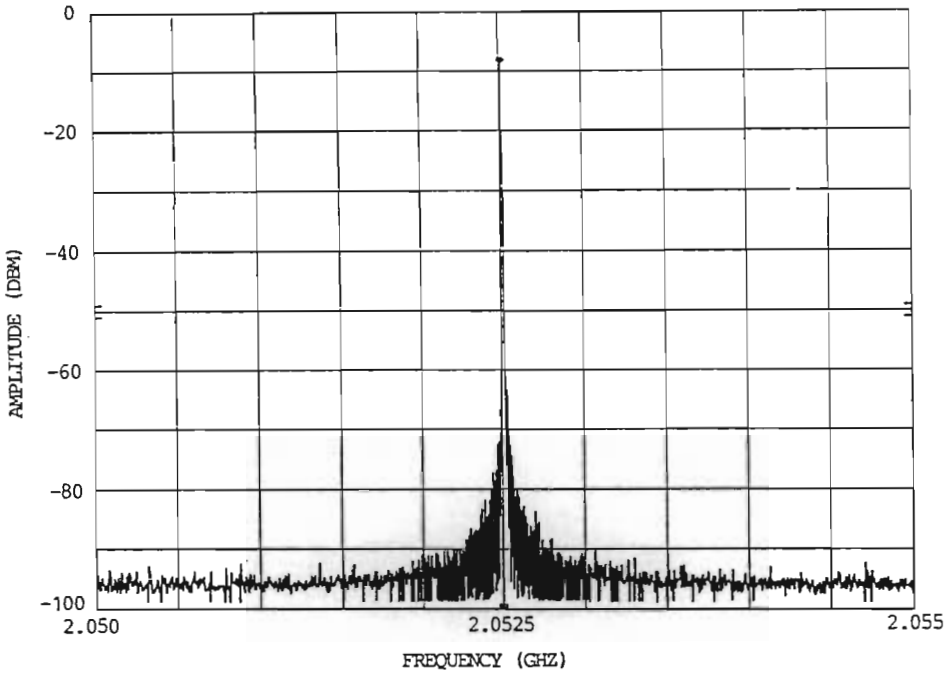


Figure 3.30. Measured Output Of Travelling-Wave Feedback Oscillator (with limiter in feedback loop)

As will be noted from Figures 3.28 and 3.30 the close-in spectrum is very clean. The output was examined from 500 MHz to 13 GHz and no spurious responses were found.

Section 3.D. Frequency Converter

The travelling-wave frequency converter consists of a limiting feedback oscillator with a signal fed into the unused input port and the desired product removed from the unused output port. Figure 3.31 is a block diagram of the converter. With the coupler removed all of the loop gain reduction must come from the limiter (assuming the amplifier gain is not reduced to the point where the loop gain is less than unity).

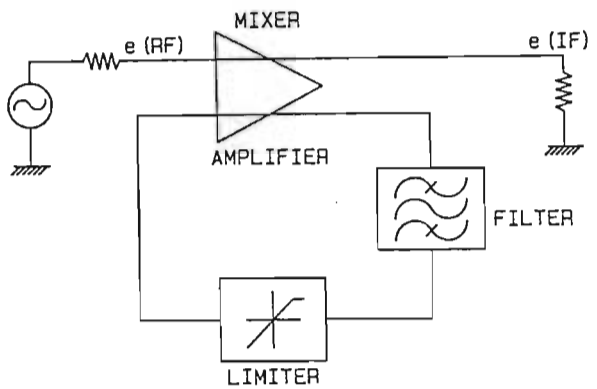


Figure 3.31. Travelling-Wave Frequency Converter

The circuit will oscillate until the gate bias reduces gain to just less than the sum of the loop losses. The filter loss was measured to be 2.6 dB just after testing the converter. The limiter insertion loss is 0.7 dB and connecting cable and connectors contribute another one dB of loss; therefore, the amplifier gain can be reduced to about 5 dB. Referring to Figure 3.8, the amplifier has 5 dB of gain at a gate bias of about -1.1 volts.

An RF signal was fed to the converter in Figure 3.31 while observing the difference frequency from the IF output. The gate bias was varied to peak the IF output. Maximum IF output was obtained at -0.95 volts gate bias. This corresponds to 6.25 dB of amplifier gain indicating that the limiter was well into its nonlinear region having to reduce the loop gain by 2 dB. This occurs at a limiter input level of 6.2 dBm with an output of 4.2 dBm. The effective local oscillator level is then 4.2 dBm.

Referring to Figure 3.13, the expected conversion loss with 4.2 dBm of local oscillator power at 2 GHz is about 12 dB. The measured conversion loss as a function of signal (RF) frequency varied from 14 to 40 dB due to gate and drain line mismatches as described in Section 2.D. The nominal conversion loss for a typical frequency segment is shown in Figure 3.32 normalised to the minimum conversion loss at an RF frequency of 630 MHz. Note the cyclical variation due to line mismatches. The conversion loss at 630 MHz input was 14 dB.

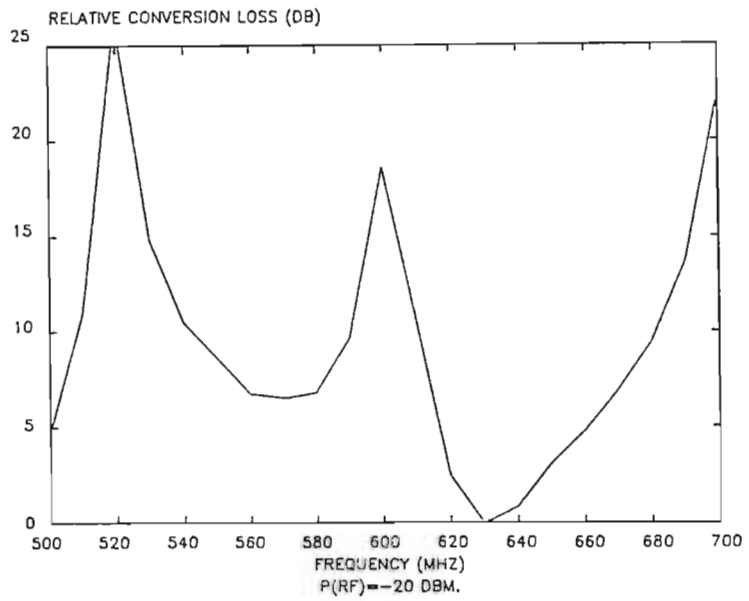


Figure 3.32. Measured Converter Relative Conversion Gain without Diplexers

There is a minima of conversion loss because the filter input is approximately a short circuit at this frequency and the connecting cable is approximately a quarter of a wave length. The impedance seen at port (4) is then an open circuit and the power is reflected back to port (2). Computer evaluation of equation 2.39 modified by equation 2.46 and 2.47 to satisfy these circumstances was in good agreement with the measured results predicting a zero dB difference at the peak. Mathematical simulation was complicated by the multiple reflections back into the gate line because of the non-infinite mismatch presented by the limiter and mismatches from the filter of power passed by the limiter. This multiple reflection causes the rapid variation in conversion loss over narrow frequency ranges observed in Figures 3.32.

Fine grain variation was minimised by placing a 3 dB attenuator between the converter gate line and the limiter. The reduction in loop gain necessitated operating the gate at greater than -0.5 volts to obtain oscillation and mixing. The loss at -.25 volts was 25 dB. Considering loss due to reduced LO power and referencing Figure 3.11, the conversion loss should be 23.5 dB. The correction factor computed by inclusion of $\rho(RF) = 0.5$ and a low IF frequency (in this case 400 MHz) predicts an increase in loss of 4 dB. Therefore, the calculated loss is 27.5 dB. Again, the measurements and theory are in reasonable agreement.

CHAPTER 4

EXTENDING OPERATING FREQUENCY

The highest operating frequency of the MESFET travelling-wave device is established primarily by the FET. In general, narrow gate devices will have higher gain and even with gain roll-off the high frequency gain will be improved. Realization of higher frequency devices requires not only advanced fabrication techniques but also methods of modelling the operating mechanisms [30-40] so that the devices can be analysed and hence optimised.

The upper frequency limit of MESFET circuits, including travelling wave devices, is constantly being increased by new technological developments. The advances in molecular beam epitaxy (MBE) [41] and metalorganic chemical vapor deposition (MO-CVD) [42] have enabled the fabrication of heterojunction structures [43] with fine structure measured in lattice constants. A direct and basic formalism is required to analyse carrier dynamics within these systems and hence to eventually enable functional synthesis. Additionally, planar fabrication technology of MESFET's on very thin epitaxial layers is defining active carrier regions of less than a thousand lattice constants. Application of basically bulk property theory to this relatively small (definitely non-infinite) system requires the modification of many of the bulk defined parameters [44-48]. Again, a new formalism is possibly in order to bracket the extreme (small) end of lattice size. The bulk and quantum level models can then be connected to obtain a better understanding of intermediate phenomena.

The advent of the large and fast digital computer has given the theoretician a new implement of formalism. Taken in the perspective of the overall development of quantum mechanical theory this is very important. Schrodinger developed his formalism in the trappings of well understood differential equations [49] whereas Heisenberg used the then new matrix methods [50]. Schrodinger's method thrived due to the acceptability of the mechanics of his formalism. Heisenberg's method is only now being used to any reasonable extent because the tools (computers) are available to manipulate the matrices.

Considerable qualitative insight into the characteristics of gases has been obtained by the solution of Schrodinger's equation for the hydrogen atom and the extrapolation by perturbation theory to heavier atoms [51]. Inclusion of the heavy atom model into a Kronig-Penny type infinite lattice [52-55] model has produced the definition of variables by which solid state materials are characterized and with which solid state devices are designed and analyzed. The reasons for use of an infinite lattice model is obvious in that the short lattice model is specialized and rather complex; however, the author proposes the use of a piecewise linear model for the crystal potential distribution to solve for the probability function from the Schrodinger wave equation. In this case there is no limitation placed upon the size and accuracy of the model except that dictated by the computer size and computational algorithms.

The author proposes the systematic definition and solution of short lattice problems in terms of piecewise linear models. The use of piecewise linear models is basic to the derivation of the fundamental concepts and understanding of quantum mechanics. The first problems encountered in band theory are the square infinite potential well problem (representing a tightly bound electron with no possibility of ionisation) and the non-infinite square potential well problem (representing an atom with the possibility of a conduction level electron). The first problems addressed in transport mechanisms are the free electron (infinitely flat potential less than the electron energy) and the quantum barrier (tunnel diode model). The theories of semiconductor junctions and thermonic emission are based upon simple barrier models that [56-58] can possibly be enhanced by more careful modelling of the barrier shapes. In all of these examples closer fitting of the mathematical potential distributions to the predictions from theory will result in the solutions moving closer to quantitative results.

The solution of the Schrodinger equation for a piecewise linear model yields the wave function Ψ (assuming a one dimension time independence). The probability function is then the wave function multiplied by its complex conjugate, Ψ^* . This distribution can now be used to compute the expectation value of any dynamical quantity ζ described by

$$E(\zeta) = \Psi^* \cdot \zeta(x) \cdot \Psi \, dx$$

where $E(\zeta)$ is the expectation value of ζ.

Appendix D contains the derivation of the equations used to structure the problem matrix, and a summary of the computer program written to solve the wave equation for Ψ. This is not represented to be a self-contained study of the definition and solution of small lattice problems but it is a description of a basic method that is being expanded by the author.

CHAPTER 5

CONCLUSIONS

A unique three-port travelling-wave mixer and extension of the concept to a frequency converter circuit based on the travelling-wave amplifier has been proposed, analyzed, constructed and tested. Correlation between theory and test data is very good. By using Schottky diode limiters the converter can be fabricated in monolithic microwave circuit technology with only minimal changes to existing travelling wave amplifier designs.

Adjustment and characterisation of the test components has been facilitated by the HP8510 Automatic Network Analyzer. Practical application of the time domain capability has been found in accurately locating discontinuities in a broadband transistor test fixture and, most especially, a level sensitive PIN diode limiter. This task would have been virtually impossible with standard time domain reflectometry.

The concept of complex circuit description by the four-port S-matrix has been carried to practical application by the derivation of transform pairs allowing analysis of large four-port circuits on small computers. The analysis method is not only applicable to travelling-wave amplifiers but also to various types of feedback circuits.

MESFET circuits are being pushed higher in frequency primarily by the extreme reduction in device geometries. This is important in the monolithic microwave integrated circuit implementation of travelling-wave devices as device performance is directly related to active element characteristics. As the devices become smaller and also as small heterojunction structures are developed the bulk derived semiconductor characteristics are increasingly inaccurate in describing device performance. The author has proposed a return to first principles and direct application of the Schrodinger wave equation to complex potential structures to describe extremely small devices. The first step of this approach is the development of a simple formalism that allows rapid solutions to potentially useful quantum structures. Modelling by piecewise linear segments has been proposed, the simultaneous differential

equations extracted and a computer program written to solve the equations. Considerable work is needed to further develop the concept but initial results are encouraging. The development of integrated functions as opposed to integrated circuits is a remote yet plausible possibility foreseen by using this analysis technique and fabrication methods such as molecular beam epitaxy.

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APPENDICES

APPENDIX A

RECEIVER CIRCUIT PATENT

United States Patent 3,942,120

Reference claim two
"...oscillator and said mixer.....
..... executed in integrated circuit form
on a common substrate."

United States Patent [19]

Ham

[11] **3,942,120**

[45] **Mar. 2, 1976**

[54] **SWD FM RECEIVER CIRCUIT**

[75] Inventor: **Ronald E. Ham**, Garland, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[22] Filed: **July 22, 1974**

[21] Appl. No.: **490,475**

[52] **U.S. Cl.** **325/344**; 325/388; 325/437; 325/451

[51] **Int. Cl.²** **H04B 1/26**

[58] **Field of Search** ..... 325/318, 344, 346, 388, 325/418, 434, 437, 442, 451, 472, 473, 488, 489, 461; 333/95 S

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Primary Examiner—Albert J. Mayer
Assistant Examiner—Jin F. Ng
Attorney, Agent, or Firm—Harold Levine; James T. Comfort; James O. Dixon

[57] **ABSTRACT**

An FM tuner for feeding an IF section of a receiver circuit includes an antenna signal input circuit with broad band response to signals in a selected FM broadcast band. A mixer is connected to receive the signal from the input circuit and a variable local oscillator is connected to the mixer operating for high side injection to produce an IF signal centered within an RF band of minimal signal content and to produce an image displaced outside the response of the input circuit. An SWD filter connected to the output of the mixer has narrow band response at the IF frequency.

4 Claims, 3 Drawing Figures

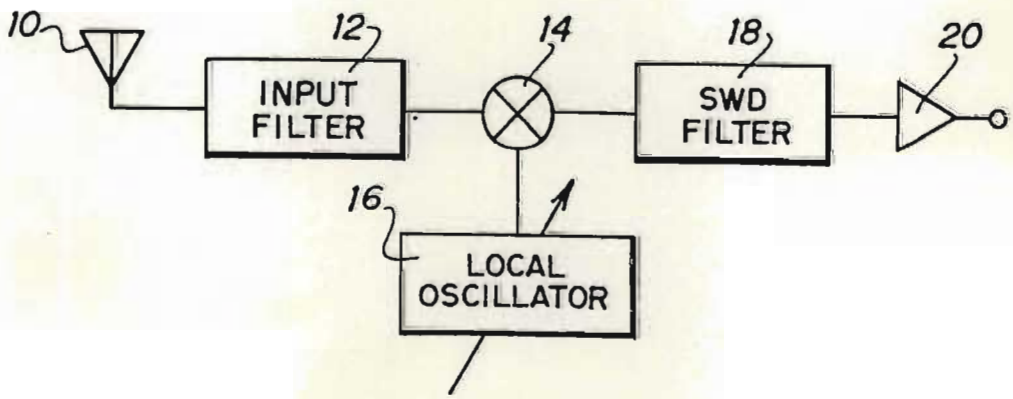


FIG. 1

FIG. 2

FIG. 3

SWD FM RECEIVER CIRCUIT

This invention relates to an FM tuner, and more particularly to a high fidelity FM tuner that may be executed extensively in integrated circuit form.

Broadcast or entertainment FM receivers of high quality generally are very expensive because of the necessity for narrow frequency selectivity. Such filtering with minimum phase distortion generally involves complex filter circuits with the result that FM systems free of phase distortion are costly.

Heretofore FM receivers with minimized phase distortion have utilized multisection high loss filters connected in tandem. This requires signal amplification in order to compensate for the loss and thus raises the noise level. The present invention provides a good signal-to-noise factor while minimizing phase distortion through the use of an IF filter comprising a surface wave device (SWD) operated at frequencies which minimize passage of unwanted signals and noise.

In prior art VHF receivers, especially FM receivers, the systems generally include a first mixer which is preceded by multisection filters and narrow band preselection filter designed to track a local oscillator to produce an IF frequency of, for example, 10.7 mHz. The use of such a low IF frequency requires the IF filtering following the mixer to be performed with inductor-capacitor resonators or bulk mode resonators. This causes band shaping to become difficult and extremely expensive if phase linearity is to be achieved.

The present invention is directed toward minimizing the foregoing problems through the use of nontracking broad band preselection and through the use of surface wave device (SWD) IF filters to provide linear phase response with minimum package size and little or no manual adjustment.

More particularly in accordance with the present invention, there is provided an FM tuner having a broad band input signal filter to cover with substantially uniform response a given entertainment FM broadcast band. A local oscillator feeds a mixer also fed by the output of the input signal filter to produce an IF signal substantially free from broadcast energy with the local oscillator providing high side injection to place image signals substantially outside the response band of the input signal filter. An SWD filter is connected as to apply the signal output from the mixer to an IF strip and to establish pass band response centered at said IF frequency.

In a more specific aspect, an FM tuner is provided for feeding an IF section of a receiver circuit in which an antenna signal input circuit is provided with broad band input response for signals in a selected FM broadcast band. A mixer is connected to receive the signals from the input filter along with the output from a variable local oscillator which is connected to the mixer operating to provide high side injection to produce an IF signal centered within an RF band of minimum signal content and producing an image outside the response of the input filter. An SWD filter is then provided having a narrow pass band at the IF frequency.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates in block diagram form an embodiment of the invention;

FIG. 2 illustrates operation of filters embodied in the invention; and

FIG. 3 illustrates a circuit diagram of an embodiment of the invention.

Referring now to FIG. 1, a VHF tuner is illustrated wherein the antenna 10 is connected by way of an input filter 12 to a mixer 14. The second input of the mixer 14 is supplied from a local oscillator 16. The output of the mixer is then applied to a surface wave device filter 18 whose output is connected to an IF strip generally indicated by amplifier 20. This superheterodyne arrangement differs from prior systems in that only the local oscillator 16 needs to be varied. Input filter 12 may be broad band to cover the particular broadcast band of interest without necessity for variable tuning. The input filter 12 may be variable. In any event, there is absent the necessity for close tracking conventionally required between oscillator 16 and the input filter 12 to achieve narrow band preselection over a wide broadcast band.

System operation as compared with prior systems can be illustrated by reference to FIG. 2 wherein a selected broadcast band, such as the FM band 24, occupies that portion of the spectrum lying between 88 and 108 mHz. Normally, prior art systems employ an IF frequency corresponding to the IF_A frequency at 10.7 mHz. In such case with low side injection of the local oscillator frequency at 89.3 mHz, the IF_A frequency is established for detection of a signal at 100 mHz. Normally, a fairly sharp filter which is represented by the dotted outline 22 is utilized and the peak frequency is varied simultaneously with variations in the frequency in the local oscillator to tune in different frequencies within band 24. The use of the local oscillator frequency of 89.3 mHz results in an image band at 78.6 mHz. Normally, this is not sufficiently rejectable by the filter having the pass band 22. Feed through of unwanted components represented by the LO_A image frequency at 78.6 mHz cannot be readily avoided.

In accordance with the present invention, local oscillator 16 is selected for high side injection using an IF frequency IF_B which leads to the use of a SWD filter 18 of size compatible with inexpensive packaging while having a controllable characteristic. It is necessary that for minimum phase distortion filter 18 have a gaussian attenuation characteristic to provide a linear phase characteristic thereby minimizing phase distortion. Furthermore, the IF_B frequency at 73.5 mHz is in the center of a radio-astronomy listening band of 73to 74.6 mHz, thus assuring the absence in the IF of feed through interference. A broad band front end filter can be used if the mixer 14 is designed for high signal levels, i.e., minimum intermodulation distortion inferring maximum intercept point. This eliminates the preselect oscillator tracking problems and avoids excessive front end gain which heretofore has been required to compensate for loss in narrow band tracking filters. By the use of a local oscillator at 173.5 mHz for detection of a signal at 100 mHz, the LO_B image is at 247 mHz, well beyond the response range of the broad band response characteristic 26 of filter 12.

Referring now to the circuit of FIG. 3, an oscillator circuit and a mixer circuit are illustrated for supplying

an IF signal to a SWD filter whose output is applied to an IF section of a receiver system.

In the mixer circuit a VHF input signal such as derived from antenna **10** is applied to a low impedance tap on an inductor L2. The output signal if then applied to the first gate of a dual gate field effect transistor (DGFET) Q2. The inductor L2 is effectively tuned by capacitors C7 and voltage variable capacitor VVC2. Capacitors C7 and VVC2 are connected in series to ground to parallel inductor L2. The magnitude of capacitor VVC2 is controlled by a voltage applied through resistor R8. Capacitor C4 is provided to bypass any A.C. components to ground

The source terminal of Q2 is connected to ground and to the Q2 substrate. The drain terminal of Q2 is connected through inductor L3 to the source V_{cc}. Inductor L3 is connected in parallel with a capacitor C6. The low impedance tap on inductor L3 is connected to an SWD filter **18** whose output is then connected to an IF amplifier strip.

A variable voltage from battery B applied through resistor R8 serves to vary the frequency to which the input circuit is tuned.

In the oscillator circuit, a D.C. voltage from battery B is applied through resistor R7 to a variable tuned circuit. The oscillator is controlled in frequency by the LC circuit comprising inductor L1, capacitor C8 and the variable capacitor VVC1. Resistor R7 is connected to the terminal common to capacitors VVC1 and C8. The junction between inductor L1 and capacitor C8 is connected to the first gate of the DGFET Q1. The source terminal of C is supported to a low impedance tap on inductor L1 and to the Q1 substrate. The drain terminal of Q1 is connected to the second gate of Q2 and by way of resistor R3 to the second gate of Q1. The second gate of Q1 is also connected through capacitor C2 to ground and to the supply V_{cc} by way of resistor R4. Capacitors C2 and C3 and resistor R4 perform bypass functions for the V_{cc} voltage.

In practice, the control voltage applied to the mixer through resistor R8 and to the oscillator through resistor R7 may be from the same source. Depending upon the construction of the voltage variable capacitors, they may be of the same magnitude or may be displaced one from another.

In an FM receiver it is necessary to use an IF filter which has a band pass of about 300 kHz. The FM broadcast band extends over a range of 20 mHz. SWD **18** acting as a filter may be provided at a minimal cost with a pass band of the order of **300** kHz. Because of the band pass characteristics of the SWD, it is possible to select the IF frequency such that the wide band filter may be employed on the front end of an FM receiver utilizing a SWD for an IF filter thereby permitting a simplified front end that may be constructed in integrated circuit form.

In the circuit of FIG. **3**, for example, the oscillator components and mixer components may all be integrated on a single substrate except for inductors L1, L2 and L3. Fabrication techniques may allow excluding capacitor C6, resistor R4 and capacitor C3 from the circuit. The circuit thus meets a criterion of low cost elements desired for the consumer market while providing an FM receiver of high performance, particularly for entertainment type of reception. Over the range of from 88 to 108 megacycles of broadcast signals, the related IF pass band is maintained at about 300 kHz wide. The system satisfies the requirement that any FM IF system needs linear phase characteristics in order to minimize phase distortion of the signal. At 10.7 mHz, the IF problem is very difficult to solve. In accordance with the present invention, it is readily solved through the use of SWD **18** at 73.5 mHz.

An SWD could be constructed to operate at 10.7 mHz, but in such case it is very large and does not lend itself to the achievement of the objectives set out. With the IF set at 73.5 mHz or at some frequency within the range of from 60 to 80 mHz, the SWD size is reduced, typically to about 1 inch in length, ⅜ inch wide and 0.030 inch thick. The local oscillator may operate at frequencies in the range of from 161.5 to 181.5 mHz to tune the broadcast band with high side injection. The image is then greatly displaced from the band of interest, i.e., in the band of from 235 to 255 mHz. Use of 10.7 mHz IF with high side injection, the local oscillator would range from 98.7 to 118.7 mHz with the image in the band from 109.4 to 121.4 which would not be readily eliminated. In contrast, the 235–255 mHz image range can readily be eliminated. This permits the use of a broad band front end filter with SWD **18** as the IF filter. The front end tuner comprising the present invention can be executed in large part in integrated circuit form, selecting operating frequencies such that feed through of unwanted signals is minimized.

In FIG. **3**, there is noted that the input filter comprising inductor L2, capacitors C7 and VV is variable through the use of the tuning voltage applied through resistor R8. Preferably the present invention involves a fixed broad band input filter having character **26** of FIG. **2**.

Having described the invention in connection with certain specific embodiments thereof, it is to be understood that further modifications may now suggest themselves to those skilled in the art, and it is intended to cover such modifications as fall within the scope of the appended claims.

What is claimed is:

1. An FM tuner for feeding an IF section of a receiver circuit which comprises:

a. an antenna signal input circuit including a broad band pass input filter having an essentially flat response to signals in the 88 to 108 mHz FM broadcast band,

b. a mixer connected to receive the signal from said input circuit,

c. a variable local oscillator connected to said mixer operating for high side injection to produce an IF signal centered within the radio astronomy listening band of 73 to 74.6 mHz and an image frequency displaced outside the response of said input filter, and

d. an SWD filter connected to the output of said mixer having a narrow pass band of 300 kHz centered at the frequency of said IF signal, the output of said SWD filter being the IF output of said tuner.

2. The combination set forth in claim **1** in which said oscillator and said mixer exclusive of their inductance components are executed in integrated circuit form on a common substrate.

3. The combination set forth in claim **1** in which said IF signal is about 73.5 mHz.

4. An FM tuner which comprises:

a. a first dual gate MOSFET,

b. a voltage tuned oscillator circuit connected at its output to the second gate of said MOSFET, the oscillation frequency of said oscillator being vari-

able over a range of from about 161.5 to 181.5 mHz,

c. an antenna input signal circuit connected to a first gate of said MOSFET by way of a voltage tuned resonant circuit responsive to pass signals within the frequency range of from 88 to 108 mHz and to

reject signals of the frequency of said oscillator and higher frequencies, and

d. a SWD filter connected to receive signals from said MOSFET having a narrow band pass of about 300 kHz centered at about 73.5 mHz.

* * * * *

APPENDIX B

FOUR-PORT NETWORK ANALYSIS

Appendix B

Table of Contents

ABSTRACT

FOUR-PORT NETWORK ANALYSIS

A four-port scattering matrix and the associated chain scattering matrix components are derived by the author. This matrix pair together with matrix multiplication facilitates the analysis of cascaded four-port devices without the necessity of limited coupling assumptions.

Section B.1. INTRODUCTION

The two-port scattering matrix in conjunction with its chain scattering matrix is used extensively for the analysis of devices composed of cascadable two-port elements; however, an increasingly important class of device requires a method of systematically treating cross coupling among four-ports. The most obvious devices to analyze with four-port elements are the distributed amplifier [B1], [B2], [B3] and the feedback amplifier [B4]. Niclas et al [B5] have suggested the use of a four-port hybrid matrix which is then used to compute the necessary S-parameters. The method herein presented by the author starts with the S-matrix thereby simplifying the use of measured parameters in an analysis. The output is also in S-parameters by use of the wave scattering-to-scattering transformation.

Section B.2. SCATTERING AND CHAIN SCATTERING MATRICES

The convention for scattering voltage wave directions incident to and reflected from a four-port device is shown in Figure B-1. From this the four equations defining the S-parameters are written:

$$\begin{bmatrix} v_1^- \\ v_2^- \\ v_3^- \\ v_4^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \cdot \begin{bmatrix} v_1^+ \\ v_2^+ \\ v_3^+ \\ v_4^+ \end{bmatrix} . \qquad \text{eq.(B-1)}$$

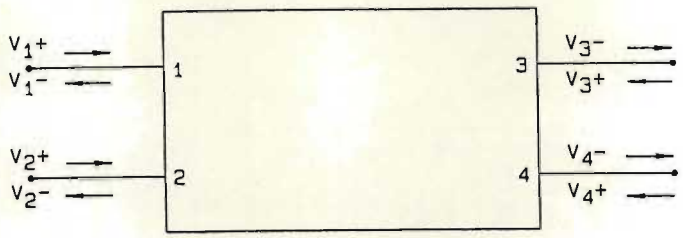


Figure B-1. FOUR-PORT SCATTERING MATRIX VOLTAGE WAVES

Figure B-2 gives the chain scattering matrix wave definitions for a two input two output element. The chain scattering matrix is defined such that ports (1) and (2) are inputs. Output ports (3) and (4) are cascaded to input ports (1) and (2) respectively of the next element. Cascading of elements is done by multiplying the chain scattering matrices of successive elements; that is, for n cascaded elements

$$\phi_T = \prod_{m=1}^{n} \phi_m$$

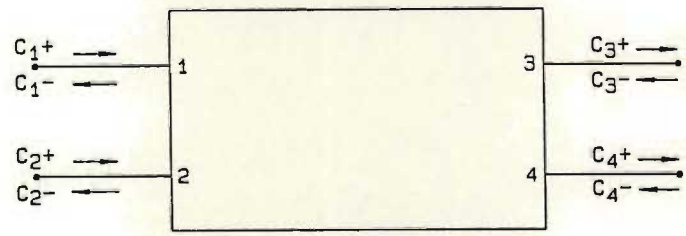


Figure B-2 FOUR-PORT CHAIN SCATTERING MATRIX VOLTAGE WAVES

The elements ϕ are defined by the chain scattering matrix

$$\begin{bmatrix} c_1^+ \\ c_1^- \\ c_2^+ \\ c_2^- \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} & \phi_{13} & \phi_{14} \\ \phi_{21} & \phi_{22} & \phi_{23} & \phi_{24} \\ \phi_{31} & \phi_{32} & \phi_{33} & \phi_{34} \\ \phi_{41} & \phi_{42} & \phi_{43} & \phi_{44} \end{bmatrix} \cdot \begin{bmatrix} c_3^+ \\ c_3^- \\ c_4^+ \\ c_4^- \end{bmatrix} . \qquad \text{eq.(B-2)}$$

From Figures B-1 and B-2 the chain scattering matrix components are equated to the scattering matrix components:

$$V_1^+ = C_1^+ \qquad V_3^+ = C_3^- \qquad \text{eq.(B-3a,b)}$$

$$V_1^- = C_1^- \qquad V_3^- = C_3^+ \qquad \text{eq.(B-3c,d)}$$

$$V_2^+ = C_2^+ \qquad V_4^+ = C_4^- \qquad \text{eq.(B-3e,f)}$$

$$V_2^- = C_2^- \qquad V_4^- = C_4^+ \; . \qquad \text{eq.(B-3g,h)}$$

Section B.3. SCATTERING MATRIX AS $f(\phi)$

Equation pairs are now obtained by substituting equation B-3 into equation B-2, arranging equation B-2 into the format of equation B-1 equating $S_{nm} = f(\phi_{kl})$ and arranging equation B-1 into the format of equation B-2 equating $\phi = f(s)$. A set of solutions for $S_{1m} = f(\phi_{kl})$ is:

$$S_{11} = \frac{E\phi_{21}}{G} \qquad \text{eq.(B-4a)}$$

$$S_{12} = \frac{B\phi_{21}}{G} \qquad \text{eq.(B-4b)}$$

$$S_{13} = \frac{BD-EA}{G} \qquad \text{eq.(B-4c)}$$

$$S_{14} = \frac{BF-EC}{G} \qquad \text{eq.(B-4d)}$$

where

$$A = \phi_{21}\phi_{12} - \phi_{11}\,\phi_{22} \qquad \text{eq.(B-4e)}$$

$$B = \phi_{21}\phi_{13} - \phi_{11}\,\phi_{23} \qquad \text{eq.(B-4f)}$$

$$C = \phi_{21}\phi_{14} - \phi_{11}\,\phi_{24} \qquad \text{eq.(B-4g)}$$

$$D = \phi_{31}\phi_{22} - \phi_{21}\,\phi_{32} \qquad \text{eq.(B-4h)}$$

$$E = \phi_{31}\phi_{23} - \phi_{21}\,\phi_{33} \qquad \text{eq.(B-4i)}$$

$$F = \phi_{31}\phi_{24} - \phi_{21}\,\phi_{34} \qquad \text{eq.(B-4j)}$$

and

$$G = B\phi_{31} - E\phi_{11}. \qquad \text{eq.(B-4k)}$$

Solutions for $S_{2m} = f(\phi_{k1})$ are

$$S_{21} = -\frac{A}{D} \qquad \text{eq.(B-5a)}$$

$$S_{22} = \frac{D\phi_{43} - A\phi_{13}}{D\phi_{33}} \qquad \text{eq.(B-5b)}$$

$$S_{23} = \frac{AE - DB}{D\phi_{33}} \qquad \text{eq.(B-5c)}$$

$$S_{24} = \frac{AF - DC}{D\phi_{33}} \qquad \text{eq.(B-5d)}$$

where

$$A = \phi_{43}\phi_{31} - \phi_{33}\,\phi_{41} \qquad \text{eq.(B-5e)}$$

$$B = \phi_{43}\phi_{32} - \phi_{33}\,\phi_{42} \qquad \text{eq.(B-5f)}$$

$$C = \phi_{43}\phi_{34} - \phi_{33}\,\phi_{44} \qquad \text{eq.(B-5g)}$$

$$D = \phi_{33}\phi_{11} - \phi_{13}\,\phi_{31} \qquad \text{eq.(B-5h)}$$

$$E = \phi_{33}\phi_{12} - \phi_{13}\,\phi_{32} \qquad \text{eq.(B-5i)}$$

and

$$F = \phi_{33}\phi_{14} - \phi_{13}\,\phi_{34} \qquad \text{eq.(B-5j)}$$

Equations for $S_{3m} = f(\phi_{k1})$ are

$$S_{31} = \frac{\phi_{33}}{A} \qquad \text{eq.(B-6a)}$$

$$S_{32} = \frac{-\phi_{13}}{A} \qquad \text{eq.(B-6b)}$$

$$S_{33} = \frac{\phi_{13}\phi_{32} - \phi_{33}\phi_{12}}{A} \qquad \text{eq.(B-6c)}$$

$$S_{34} = \frac{\phi_{13}\phi_{34} - \phi_{33}\phi_{14}}{A} \qquad \text{eq.(B-6d)}$$

where

$$A = \phi_{33}\phi_{11} - \phi_{13}\,\phi_{31}. \qquad \text{eq.(B-6e)}$$

Finally, a set of solutions for $S_{4m} = f(\phi_{k1})$ is

$$S_{41} = \frac{\phi_{31}}{A} \qquad \text{eq.(B-7a)}$$

$$S_{42} = \frac{-\phi_{11}}{A} \qquad \text{eq.(B-7b)}$$

$$S_{43} = \frac{\phi_{11}\phi_{32} - \phi_{31}\phi_{12}}{A} \qquad \text{eq.(B-7c)}$$

$$S_{44} = \frac{\phi_{11}\phi_{34} - \phi_{31}\phi_{14}}{A} \qquad \text{eq.(B-7d)}$$

where $A = \phi_{31}\phi_{13} - \phi_{11}\phi_{33}.$ eq.(B7-e)

Section B.4. Chain Scattering Matrix as f(S)

The chain scattering matrix is obtained by solving for $\phi_{mn} = f(S_{kl})$ yielding a set of equations for ϕ_{1n}:

$$\phi_{11} = \frac{-S_{43}}{A} \qquad \text{eq.(B-8a)}$$

$$\phi_{12} = \frac{S_{42}S_{33} - S_{32}S_{43}}{A} \qquad \text{eq.(B-8b)}$$

$$\phi_{13} = \frac{S_{32}}{A} \qquad \text{eq.(B-8c)}$$

$$\phi_{14} = \frac{S_{42}S_{34} - S_{32}S_{44}}{A} \qquad \text{eq.(B-8d)}$$

where $A = S_{32}S_{41} - S_{42}S_{31}$. eq.(B-8e)

Equations for ϕ_{2n} are

$$\phi_{21} = \frac{DS_{11} + AS_{41}}{DS_{31}} \qquad \text{eq.(B-9a)}$$

$$\phi_{22} = \frac{DB - AE}{DS_{31}} \qquad \text{eq.(B-9b)}$$

$$\phi_{23} = -\frac{A}{D} \qquad \text{eq.(B-9c)}$$

$$\phi_{24} = \frac{DC - AF}{DS_{31}} \qquad \text{eq.(B-9d)}$$

where $A = S_{31}S_{12} - S_{11}S_{32}$ eq.(B-9e)

$B = S_{31}S_{13} - S_{11}S_{33}$ eq.(B-9f)

$C = S_{31}S_{14} - S_{11}S_{34}$ eq.(B-9g)

$D = S_{41}S_{32} - S_{31}S_{42}$ eq.(B-9h)

$E = S_{41}S_{33} - S_{31}S_{43}$ eq.(B-9i)

and

$F = S_{41}S_{34} - S_{31}S_{44}$. eq.(B-9j)

For $\phi_{3n} = f(S_{k1})$ the equations are

$$\phi_{31} = \frac{-S_{41}}{A} \quad \text{eq.(B-10a)}$$

$$\phi_{32} = \frac{S_{41}S_{33} - S_{31}S_{43}}{A} \quad \text{eq.(B-10b)}$$

$$\phi_{34} = \frac{S_{31}}{A} \quad \text{eq.(B-10c)}$$

and

$$\phi_{34} = \frac{S_{41}S_{34} - S_{31}S_{44}}{A} \quad \text{eq.(B-10d)}$$

where

$A = S_{31}S_{42} - S_{41}S_{32}$. eq.(B-10e)

Comparable solutions for $\phi_{4m} = f(S_{k1})$ are

$$\phi_{41} = \frac{DS_{21} + AS_{41}}{DS_{31}} \qquad \text{eq.(B-11a)}$$

$$\phi_{42} = \frac{DB - AE}{DS_{31}} \qquad \text{eq.(B-11b)}$$

$$\phi_{43} = -\frac{A}{D} \qquad \text{eq.(B-11c)}$$

and

$$\phi_{44} = \frac{DC - AF}{DS_{31}} \qquad \text{eq.(B-11d)}$$

where $A = S_{31}S_{22} - S_{21}S_{32}$ eq.(B-11e)

$B = S_{31}S_{23} - S_{21}S_{33}$ eq.(B-11f)

$C = S_{31}S_{24} - S_{21}S_{34}$ eq.(B-11g)

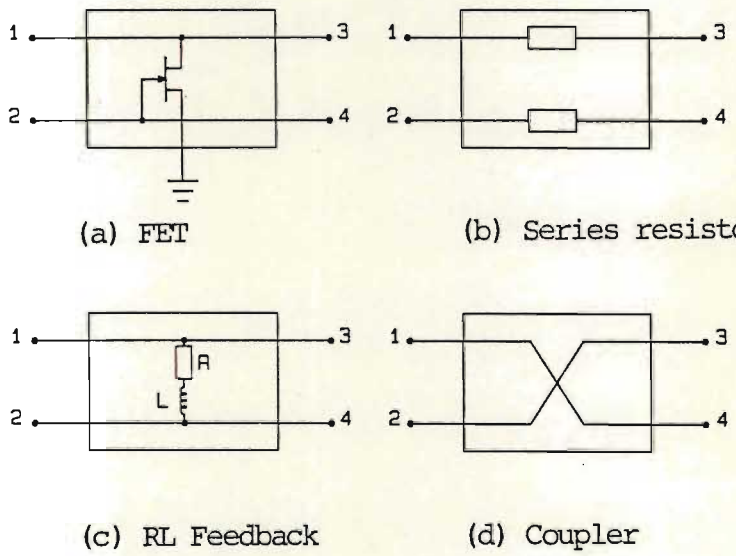
$D = S_{41}S_{32} - S_{31}S_{42}$ eq.(B-11h)

$E = S_{41}S_{33} - S_{31}S_{43}$ eq.(B-11i)

and $F = S_{41}S_{34} - S_{31}S_{44}$. eq.(B-11j)

Section B.5. Cascaded Circuits

Numerous elements can be used in a catalog for building circuits. Some of the most useful are illustrated in Figure B-3. The active device (Figure B-3a) and reactive feedback (Figure B-3c) elements have coupling between ports (1) and (4) and ports (2) and (3). By repeatedly cascading active devices with shunt capacitors, shunt resistors and series inductors (or high impedance transmission lines) as in Figure B-4 a distributed amplifier can be simulated with no assumptions of minimum coupling being necessary.



(a) FET (b) Series resistors

(c) RL Feedback (d) Coupler

Figure B-3. Some Four-Port Circuit Elements

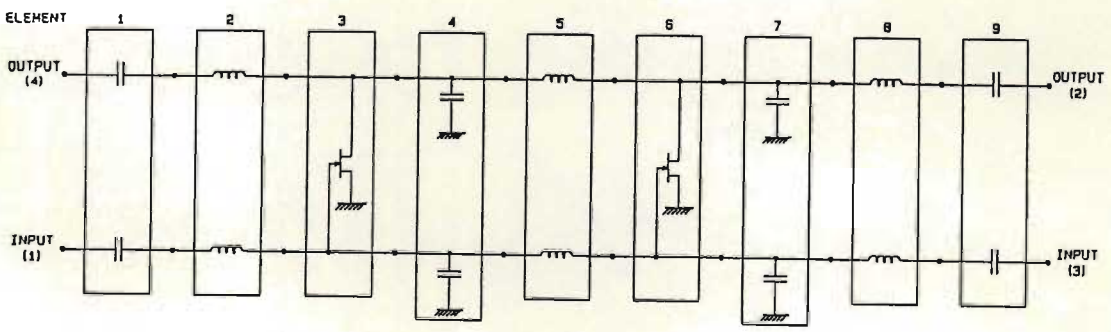


Figure B-4. A Distributed Amplifier Configured from Four-Port Elements

Section B.6. Computer Program

A computer program was written to assist the designer to input the circuit topography and compute the four-port frequency response. Referencing Figure B-5 the input is interactive and the elements are entered sequentially. Element definition consists of element type and component value(s). The analysis frequency and number of steps is then defined.

The analysis procedure begins by computing the first analysis frequency, f_1. The scattering matrices and chain scattering matrices for the first two elements are calculated for F_1 and the chain scattering matrices are multiplied together. The resultant is stored for the next pass with the third element. The chain scattering matrix for the third element is calculated and multiplied by the resultant matrix from the first pass. This process continues until the last element value has been computed and multiplied. The resultant ϕ_T is used to compute the total scattering matrix S_T. If there is another frequency at which the response is to be repeated the frequency is iterated and the process repeated after storing and/or outputting the result.

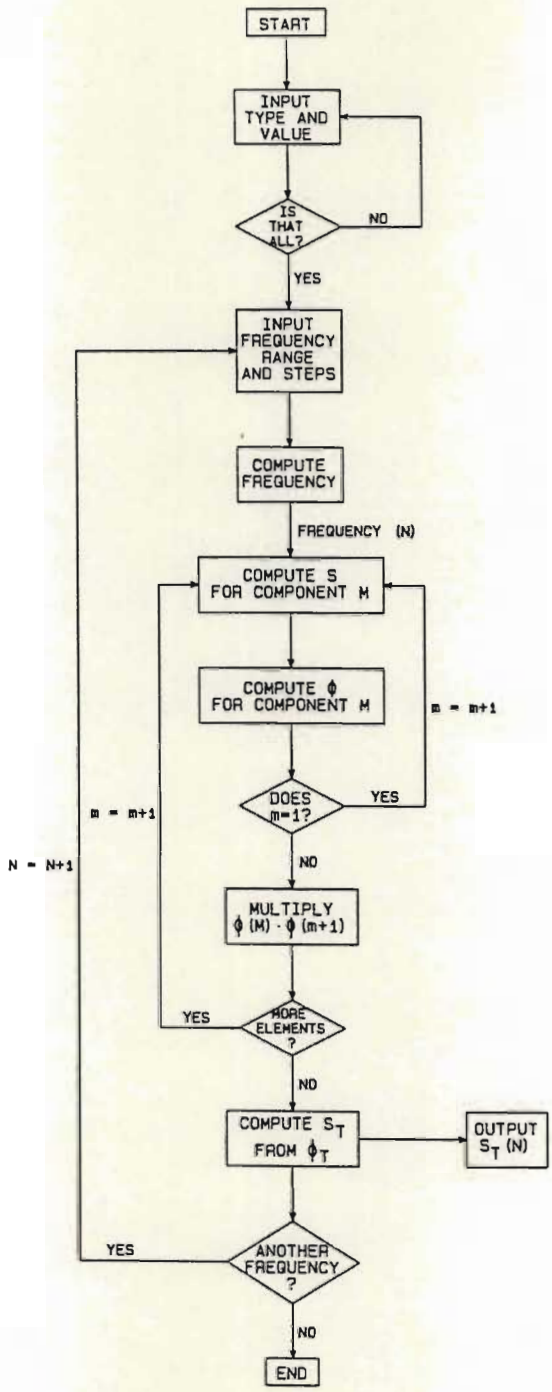


Figure B-5. Computer Program Flow Diagram

Section B.7. Conclusions

The equation pairs to convert between the scattering matrix and the cascadable chain scattering matrix have been derived and a computer program has been written to (1) calculate the scattering matrices for elements, (2) compute the chain scattering matrices, (3) multiply the matrices and (4) compute the scattering matrix for the entire circuit. This program facilitates the analysis of rather complex circuits on a small computer with minimal memory.

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APPENDIX C

MESFET Measurements and Modelling

ABSTRACT

MESFET Measurement and Modelling

To enable the construction and analysis of the travelling-wave three-port mixer and frequency converter the characteristics of the devices used were required. More data was needed than was supplied by the device supplier; therefore, the author built a test fixture and wrote the necessary software for de-embedding using the inverse of the chain scattering matrix. A model of the device was then derived to fit the measured data.

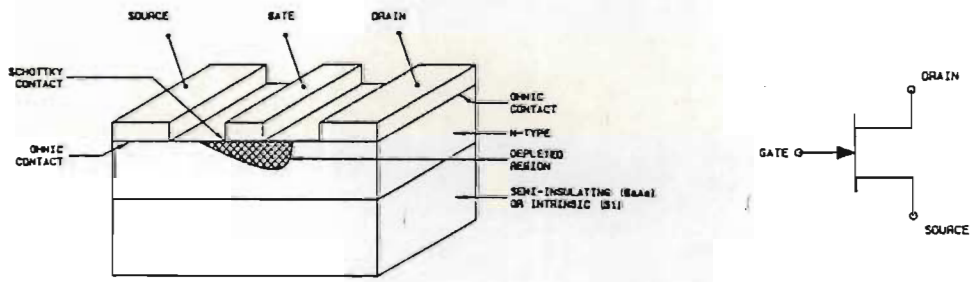
Appendix C

Table of Contents

Section C.1. Introduction

Most of the circuits addressed in this thesis are based on metal semiconductor field effect transistors (MESFET's); therefore, this appendix covering the measurement and modelling of the MESFET is necessary to justify the models and model values used in the demonstration circuit design.

Pucel et al [C1], Sze [C2], and Liechti [C3] have given complete phenomenological descriptions of the junction and metal semiconductor FET for moderate gate widths. The basic operation of these devices as shown in Figure C-1 depends upon reducing the conduction channel cross section by forcing a depleted region into the channel with the application of reverse voltage to the gate diode.



(a) Physical Construction (b) Symbol

Figure C-1. The Metal Semiconductor Field Effect Transistor

At microwave frequencies many parasitic and intrinsic components are required to model the FET device for inclusion in circuit designs. Additionally, the device has to be placed into some form of test media, usually a multilead package, and this also adds parasitics that mask the actual device characteristics. Therefore, a well defined test fixture is required to measure the device performance such that any undesired parasitics can be calculated out of the measured data; that is, the desired information can be de-embedded [C4] from the measurements.

The sequence of events necessary to obtain the device equivalent circuits needed for circuit designs in the thesis are (1) construct and characterize a broadband transistor test fixture, (2) make the

measurements and de-embed unwanted test fixture parasitics (this results in final test results) and (3) create and optimise a device equivalent circuit to mimic the measured results. This model is then used for the circuit design. The following sections address these points.

Section C.2. Test Fixture and De-embedding

The transistor test fixture must provide a controlled characteristic mount for the device in which the transmission lines in and out of the device are identical to the measurement system characteristic impedance (usually fifty ohms). Additionally, a direct ground return must be provided for the common terminal. Biasing is supplied through components external to the test fixture. The fixture then takes the form of a transmission line with a mounting gap supplied for the unit under test and some means of accurately determining the reference planes at the device.

Plate C-1 is a photograph of the completed transistor test fixture and plate C-2 shows the fixture opened with a transistor in place. The transistor mounts into slots (plate C-3) in the transmission lines (Figure C-2) and the common leads are shorted to ground by the central segment (Figure C-3). Figure C-4 is a planar assembly diagram for the test fixture configured to accept a device. Figures C-5 and C-6 are of the end plates and large spacer segment. The large spacer segments are also the outer conductor of the transmission line.

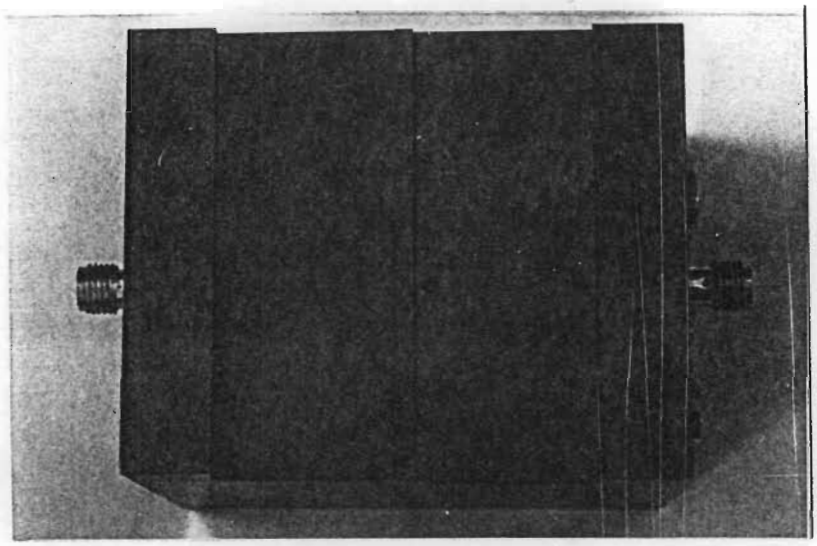


Plate C-1. Transistor Test Fixture

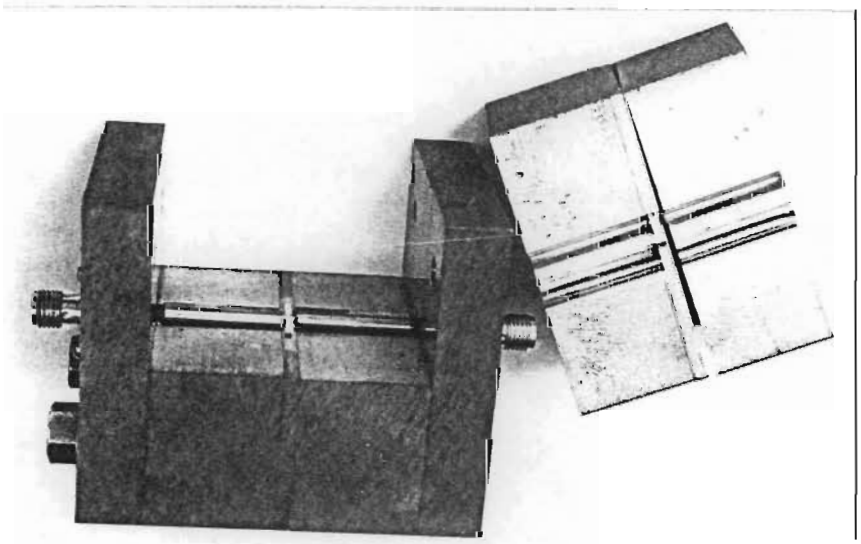


Plate C-2. Transistor Test Fixture with Top Section Removed

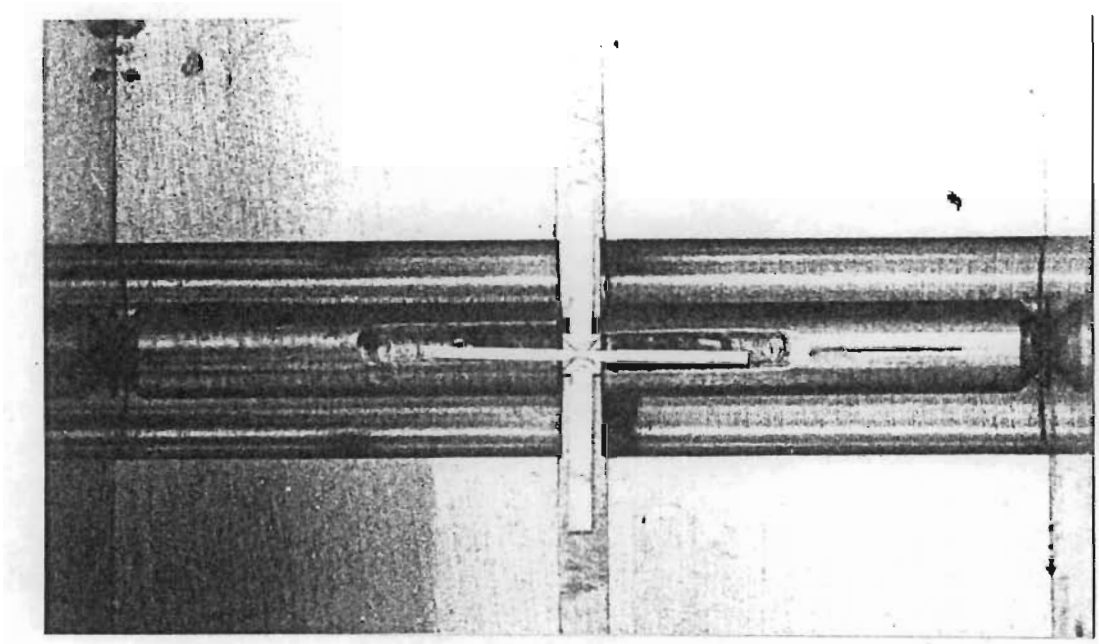


Plate C-3. Transistor Placed in the Test Fixture

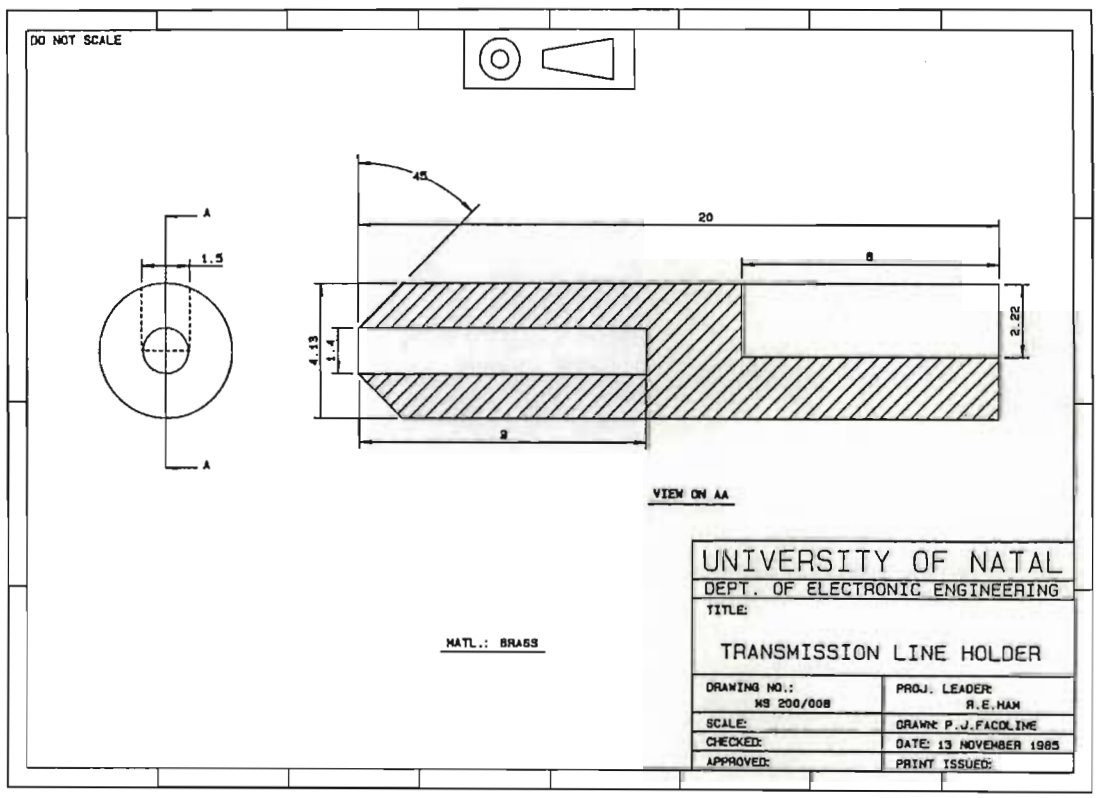


Figure C-2.

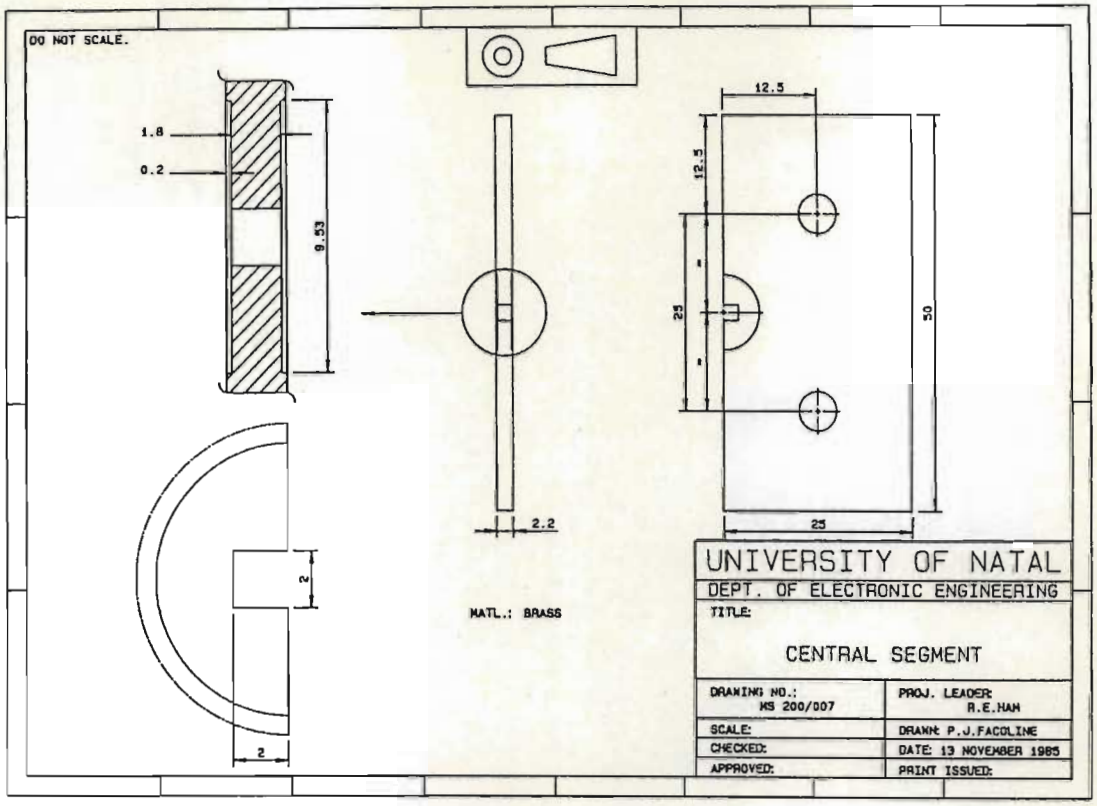
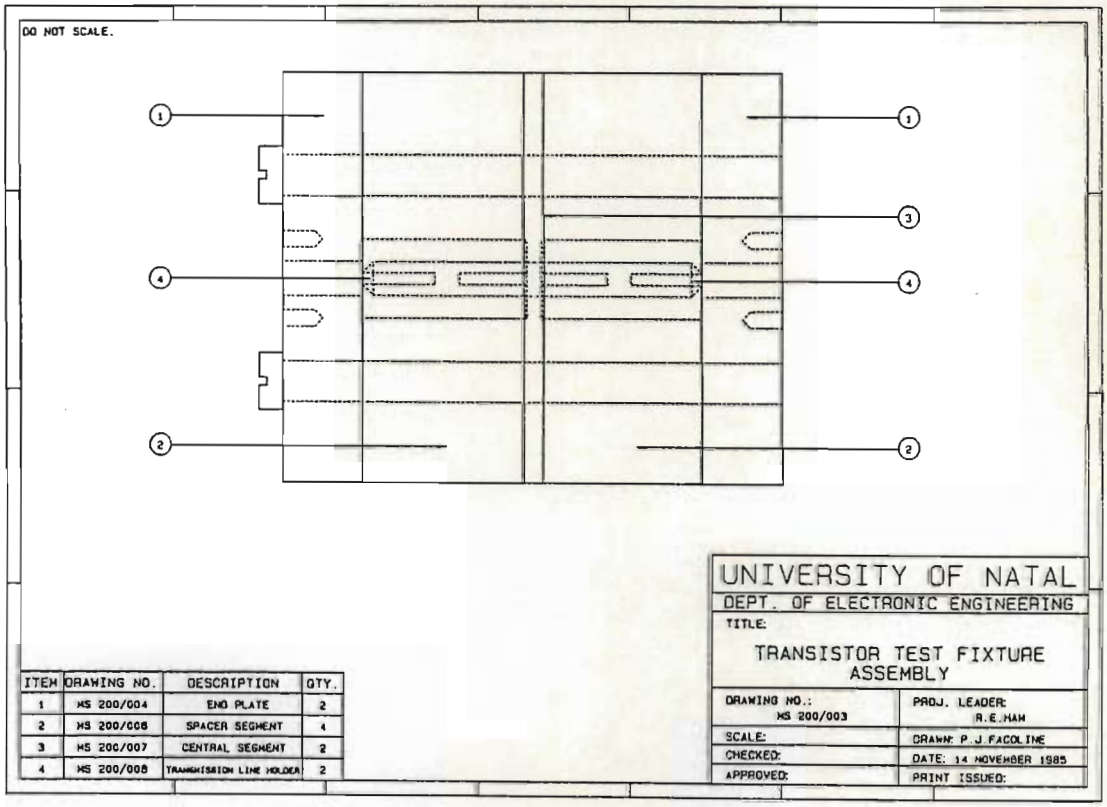


Figure C-3.



ITEM	DRAWING NO.	DESCRIPTION	QTY.
1	MS 200/004	END PLATE	2
2	MS 200/006	SPACER SEGMENT	4
3	MS 200/007	CENTRAL SEGMENT	2
4	MS 200/008	TRANSMISSION LINE HOLDER	2

Figure C-4.

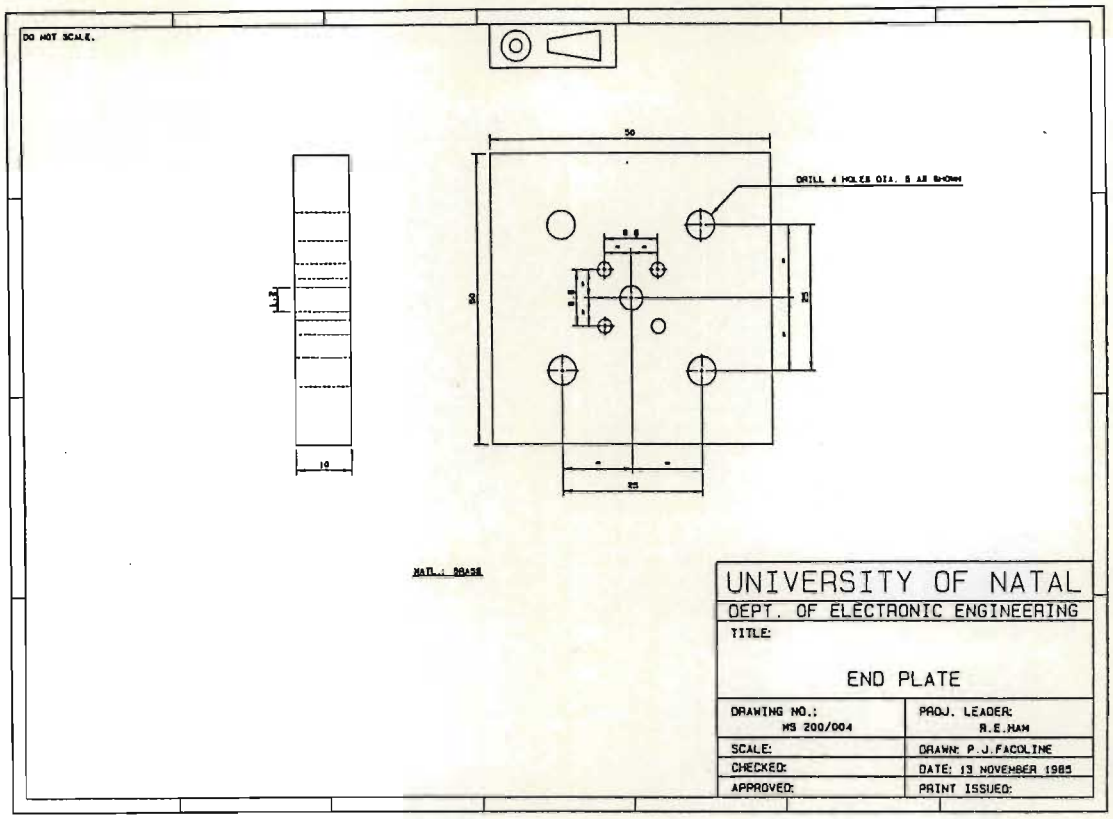


Figure C-5.

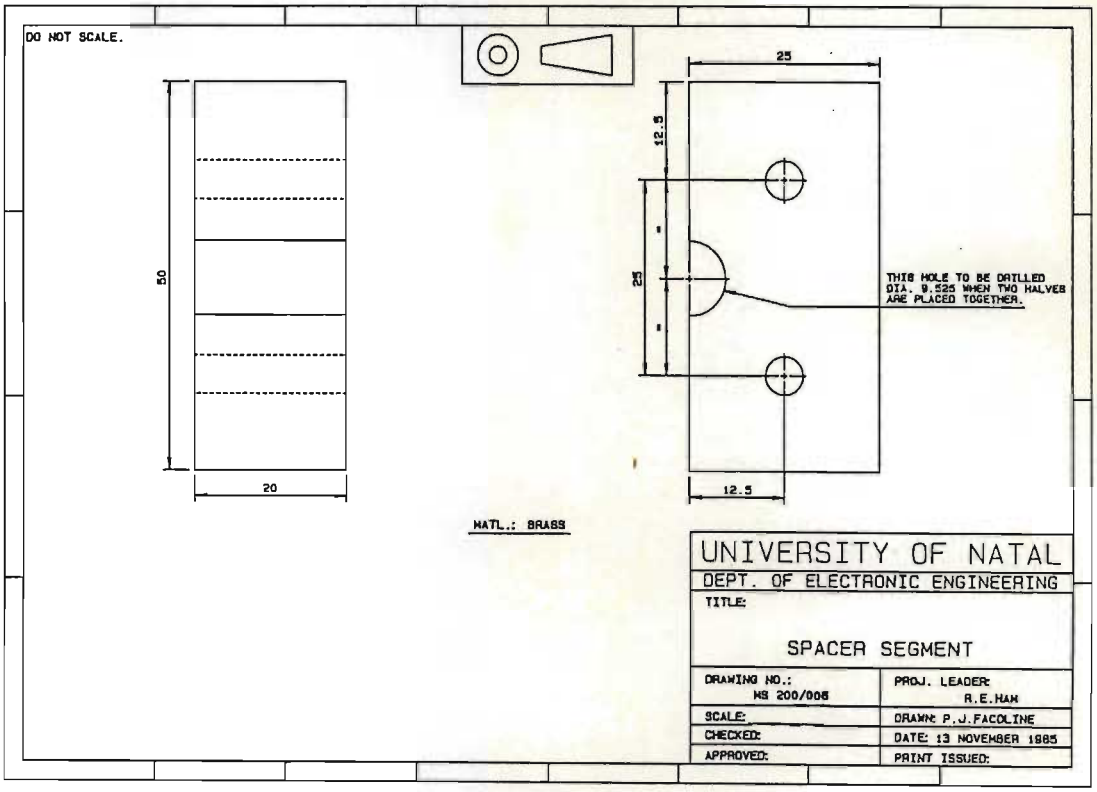


Figure C-6

To adjust and through calibrate the fixture the central segment is removed and the fixture is bolted together with all large spacer segments in place. The fixture is then ideally just a piece of air line. The fixture in this configuration was tested in the time domain with the HP8510 Automatic Network Analyzer (Appendix E). The time response before any adjustments were made is shown in Figure C-7a. This shows capacitive discontinuities at the transitions from the connectors to the centered conductors.

The teflon insulators in the SMA connectors were cut back into the connectors to reduce the capacitance and introduce series inductance. This reduced the discontinuity considerably as shown by Figure C-7b. Portions of the residual discontinuities were then gated out (Figure C-8a) resulting in an effective VSWR for the test fixture of 1.1:1 or less up to about 15 GHz (Figure C-8b). The fixture is considered useable in the present configuration up to about 10 GHz with a VSWR of less than 1.05:1.

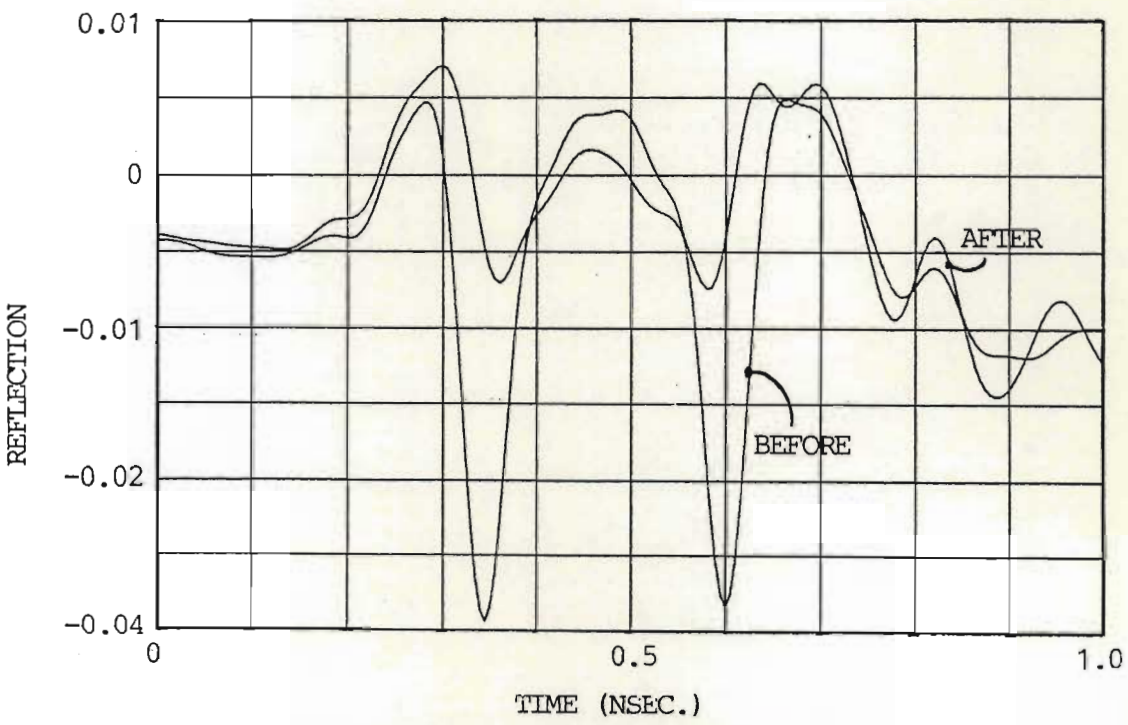
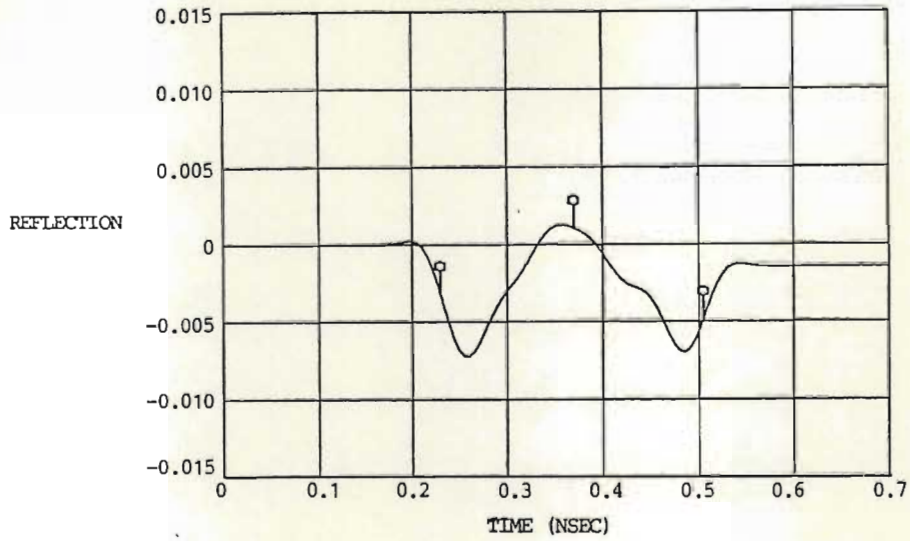
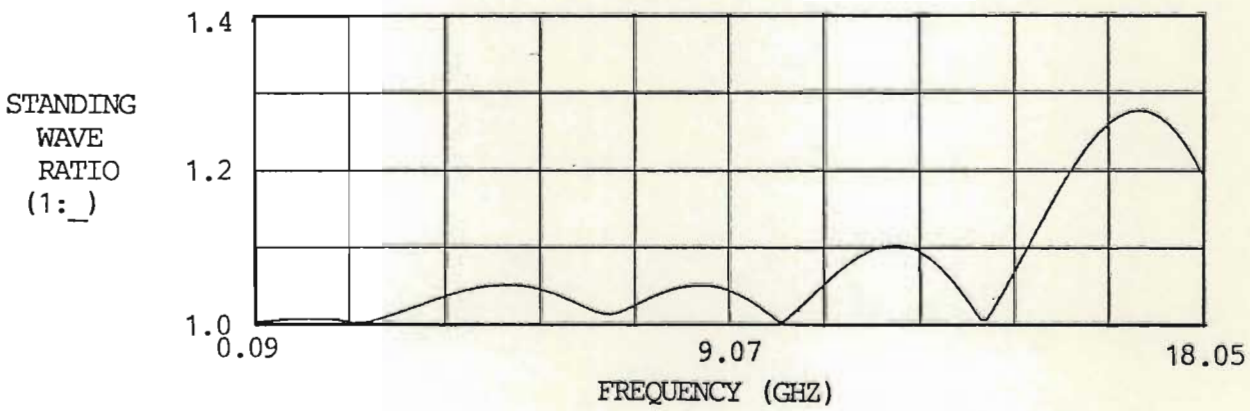


Figure C-7. Time Domain Response of Test Fixture (a) Before and (b) After Adjusting Connector Capacitance



(a) Time



(b) Frequency

Figure C-8. Time Gated Response of the Transistor Test Fixture

The primary contributors to band limiting discontinuities are the SMA connectors and the large diameter transitions necessary to change from the SMA bulkhead connectors to the transistor mount. The use of a larger connector type (preferably APC-7) is necessary to reduce the discontinuities and increase the useable fixture bandwidth.

A calibration of each port up to the plane defined by the end of each centre conductor/transistor mount was performed by terminating the fixture in the through configuration with a matched sliding load. This allows the analyzer to compute correction factors for the centre region of the Smith chart. A short circuit was defined with a shorting plate at the position of the central segment. A shielded open circuit was formed by withdrawing the opposing centre line/transistor mount. An end capacitance was estimated and placed into the calibration kit correction factors. This capacitance correction value was iterated until a short circuit at the end of the line yielded a point at zero resistance over the measurement range on the HP8510 Smith chart output.

The test fixture was reassembled with the central segment in place but with no device. The frequency response of the fixture was measured. Ideally, the measurements should show open circuits at the reference planes and zero transmission; however, the measurement data in Figure C-9 shows, as expected, capacitive reactance at the end of the lines due to end capacitance to the central segment. The approximate capacitance values are both 0.6 pF. The magnitudes of the transmission components S_{12} and S_{21} are both less than 0.012. The effect of the transmission component on a transistor device is negligible in most cases; however, the end capacitance must be removed by post measurement processing.

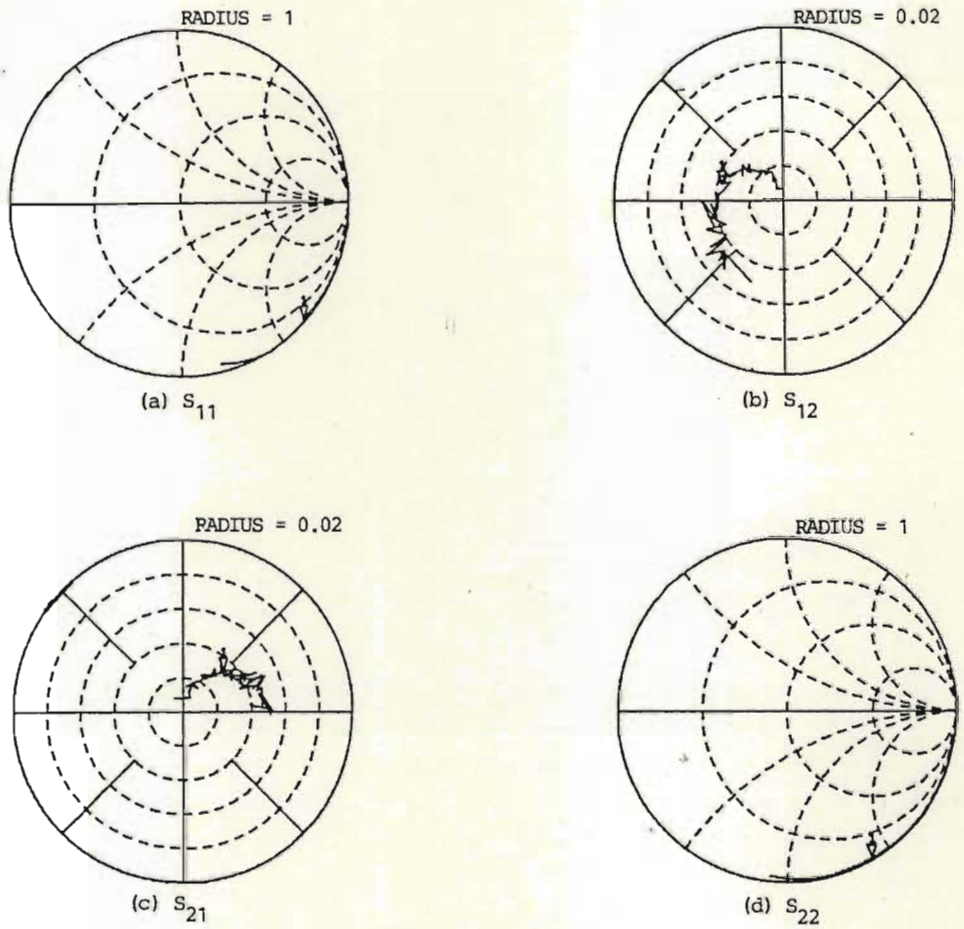


Figure C-9. Transistor Test Fixture with Centre Spacer in Place (no device, no de-embedding) Frequency = 0.5 to 5.5 GHz

Removal of unwanted circuit parasitics and discontinuities after measurements have been made is de-embedding and can be considered to be the inverse of circuit analysis. The circuit resulting from the capacitances at the reference planes with a device in place is shown in Figure C-10. The measured S-matrix is for the entire circuit. The S-matrix of the device is the desired data. The measured S-matrix can be converted to the chain scattering matrix (reference Appendix B) and is equal to the product of the chain scattering matrices of the three cascaded components

$$\phi_T = \phi_{C1} \cdot \phi_{FET} \cdot \phi_{C2}.$$

Multiplying each side of the equation by the inverse of ϕ_{C1} and then the inverse of ϕ_{C2} yields

$$\phi_{FET} = \phi_{C1}^{-1} \cdot \phi_T \cdot \phi_{C2}^{-1}.$$

The device S-matrix is then calculated from the resultant chain scattering matrix ϕ_{FET}.

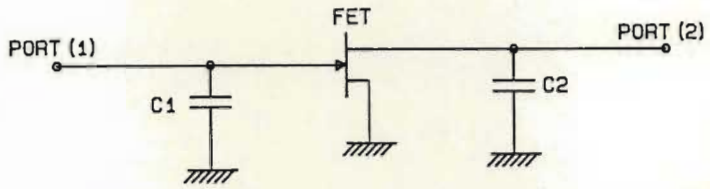


Figure C-10. Measured Circuit before De-Embedding

The HP8510 Network Analyzer at the University of Natal microwave laboratory is interfaced to an HP9836C computer that facilitates control of measurements by computer software. A program was written to initiate device measurements, download the data to the computer, de-embed the desired information and transfer the resultant back into the HP8510 memory to be displayed and plotted.

Before measuring device data the test fixture without a device was characterized to assure that the unwanted components were being removed and that the information remaining was due only to the device being tested. The result of this measurement is shown in Figure C-11. Note that S_{12} and S_{21} are less than 0.02, a slight increase; however, the open circuit at ends of the lines are points over the frequency range at infinite resistance as they should be. From these measurements it is deduced that the de-embedding is working properly.

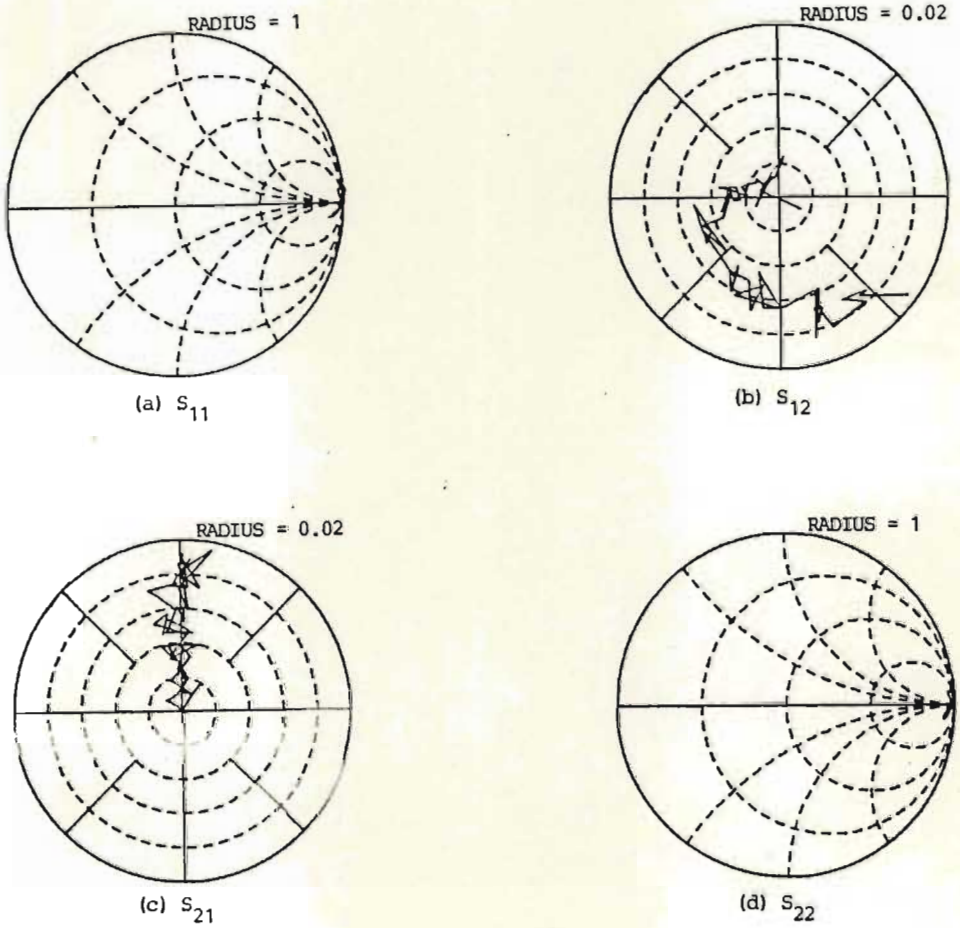


Figure C-11. Transistor Test Fixture with Centre Spacer in Place (no device, with de-embedding) Frequency = 0.5 to 5.5 GHz.

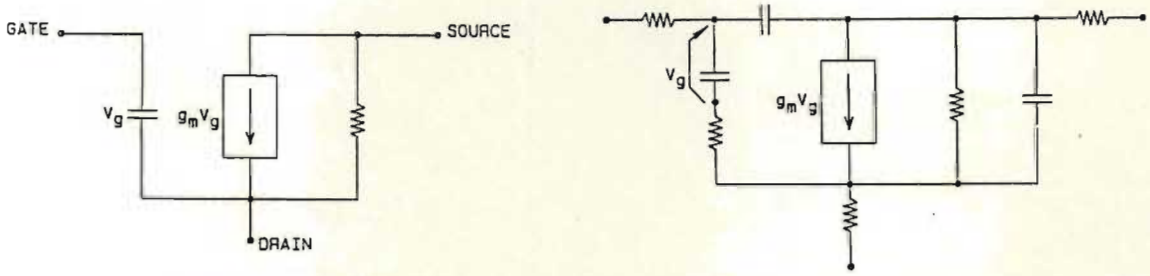
Section C.3. Device Measurements and Modelling

Device measurements and modelling of the devices will be treated in one section because little distinction between the processes was made in fact. The data was measured under computer control yielding de-embedded measurement data files. These files were then fed to a Touchstone program with the proper topology to simulate the measured device and approximate element values. The program was instructed to optimise the model to the measured S-parameter data. The derivation of the model and the results of the measurements and optimisations are presented in this section.

The low frequency intrinsic saturation model of an FET consists only of a high input impedance (or small capacitor) and a current source that is dependent upon the voltage across the input capacitor as in Figure C-12a. This low frequency model can be modified for higher frequency use by the addition of circuit parasites and by allowing for transit time by including a time delay term τ in the transconductance g_m so that

$$g_m = g_m' \cdot \exp(j\omega\tau)$$

as shown in Figure C-12b. A packaged MESFET model is obtained by adding package parasites to the high frequency chip model. All of the terminals of the chip must be bonded out to the package resulting in a series inductance. The non-grounded terminals (gate and source for common drain and drain and source for common gate connections) are usually transmission lines that become the outside leads. The transmission lines then connect to an external circuit where there is a small amount of discontinuity capacitance. Figure C-13 is the composite equivalent high frequency circuit for a packaged device.



(a) Low Frequency Intrinsic Model

(b) High Frequency Model

Figure C-12. Unpackaged MESFET Chip Equivalent Circuit Models

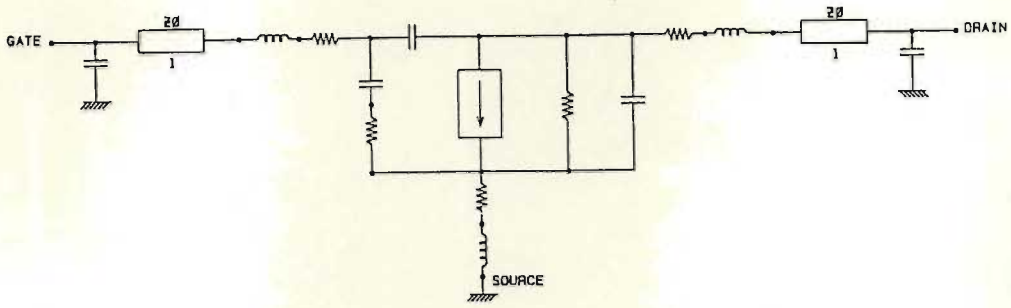


Figure C-13. Composite High Frequency Equivalent Circuit for a Packaged MESFET

By comparing the equivalent circuit performance with that of the actual transistor it was determined that the series resistors in each lead were of minimal importance at low to moderate bias levels. As this was the range over which the device was to be used, the elements were removed from the model.

The device used for testing the travelling-wave frequency converter was the Dexcel DXL 2501. The non-linear components of this device were identified by measuring the S-parameters at different bias levels. The transistor model is shown in Figure C-14 and the resulting model component values for various gate bias levels are listed in Table C-1. Figures C-15 through C-18 contain plots of the measured and modelled S-parameters. Figure C-19 shows the variation of g_m, C_{gs} and R_{ds} with gate bias.

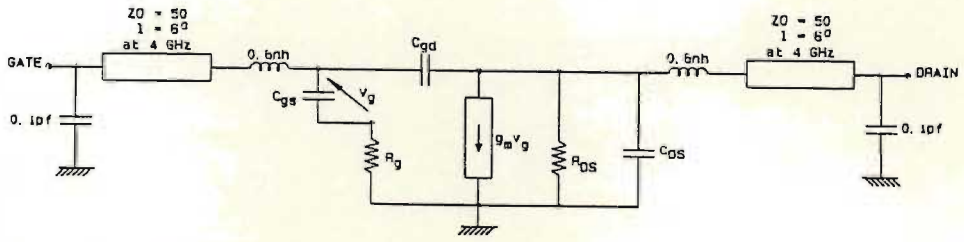


Figure C-14. High Frequency Packaged MESFET Equivalent Circuit Model

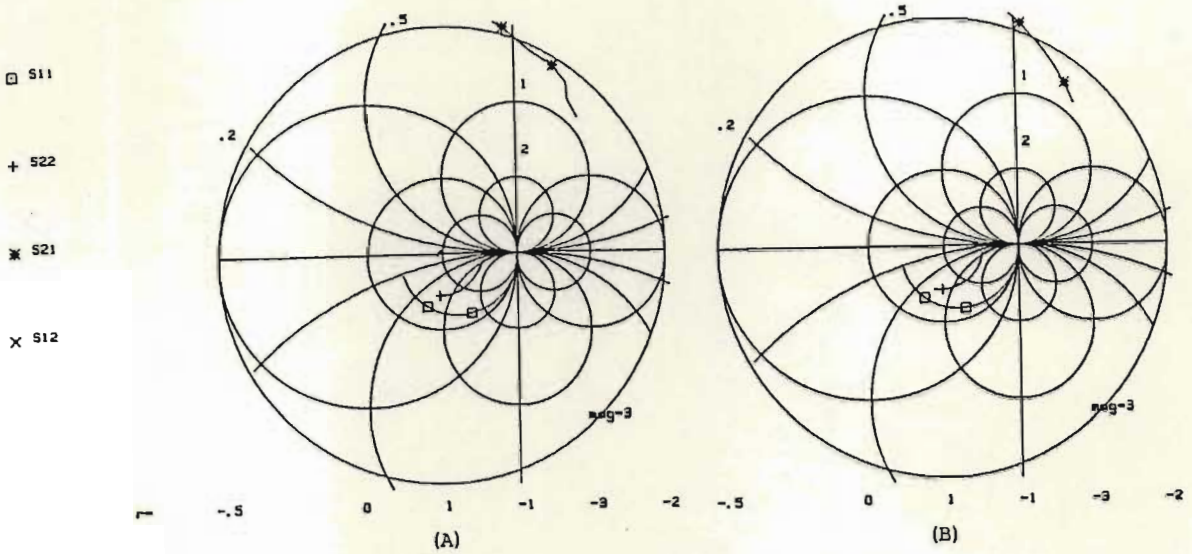


Figure C-15. S-Parameters for DXL 2501 with
V_{ds} = 2.2 v, V_{gs} = 0 v.
(A) Measured Data (B) Computed from Model
Frequency = 0.5 to 5.5 GHz.

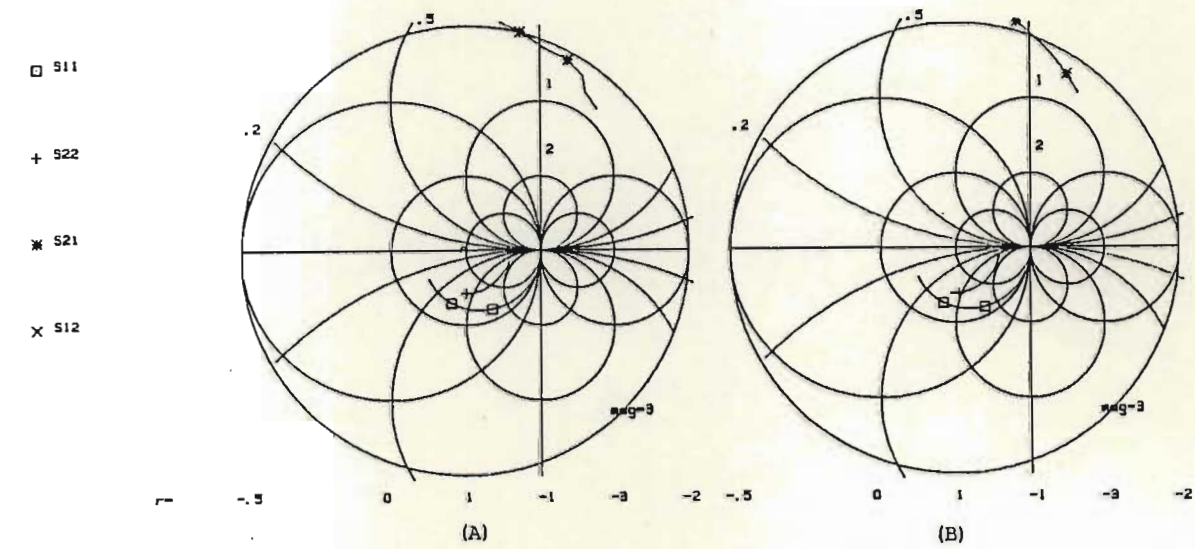


Figure C-16. S-Parameter for DXL 2501 with
V_{ds} = 2.2 v, V_{gs} = 0.3 v.
(A) Measured Data (B) Computed from Model
Frequency = 0.5 to 5.5 GHz.

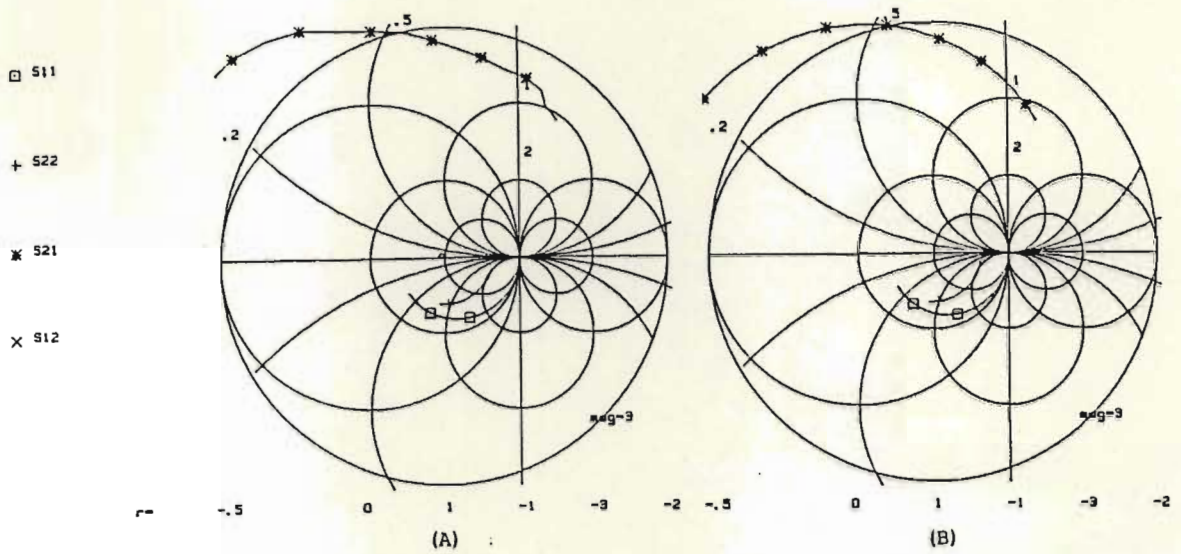


Figure C-17. S-Parameters for DXL 2501 with
V_{ds} = 2.2 v, V_{gs} = -0.8 v.
(A) Measured Data (B) Computed from Model
Frequency = 0.5 to 5.5 GHz.

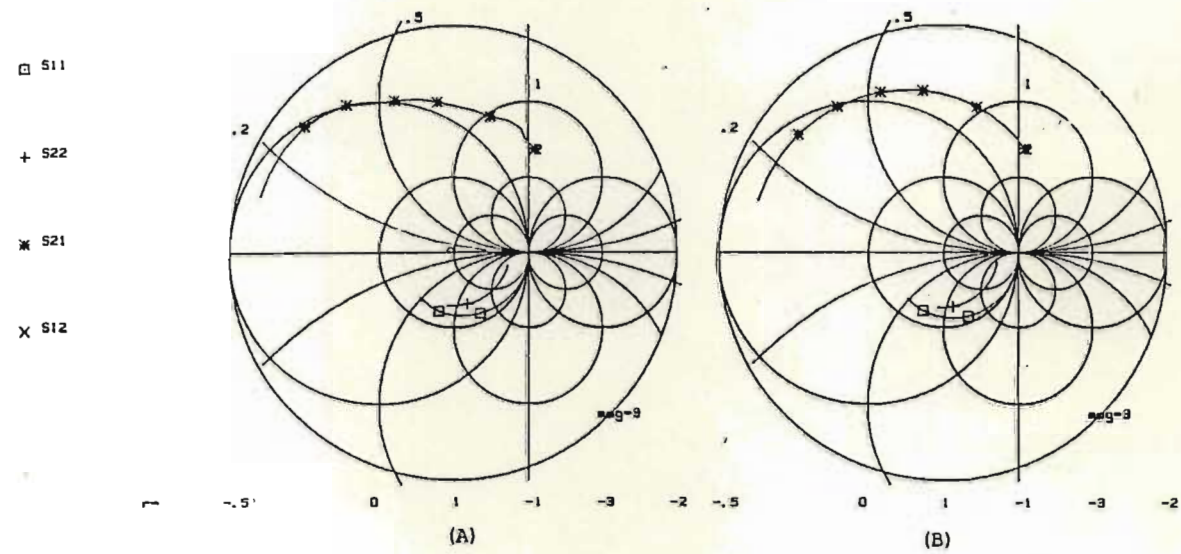
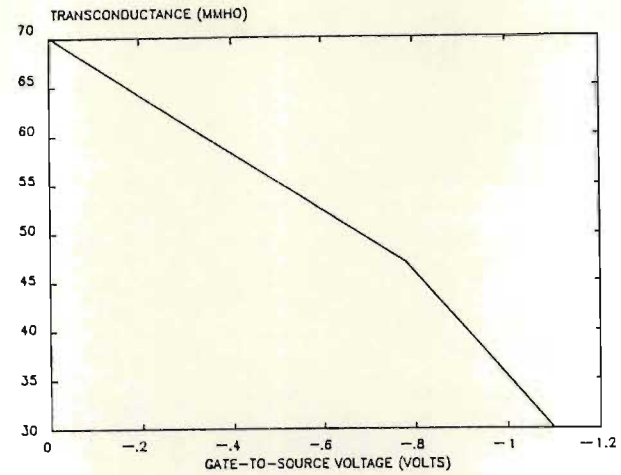


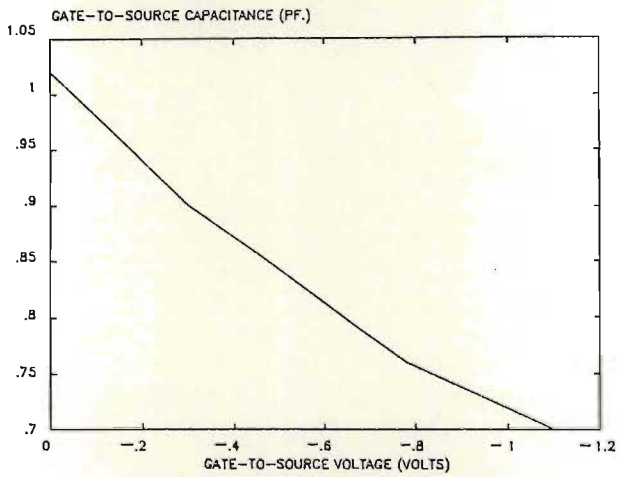
Figure C-18. S-Parameters for DXL 2501 with
(A) Measured Data (B) Computed from Model.
V_{ds} = 2.2 v, V_{gs} = -1.1 v., Frequency = 0.5 to 5.5 GHz.

Gate Bias	g_m (mmhos)	C_{gs} (pf)	R_{ds} (ohms)	τ_{gm} (nsec)	C_{gd} (pf)	R_g (ohms)
0v	70	1.02	160	3.4	0.0006	15
-0.3v	61	0.90	185	4.0	0.0006	14
-0.8v	47	0.76	235	5.2	0.0006	13
-1.1v	30	0.70	290	7.0	0.0006	10

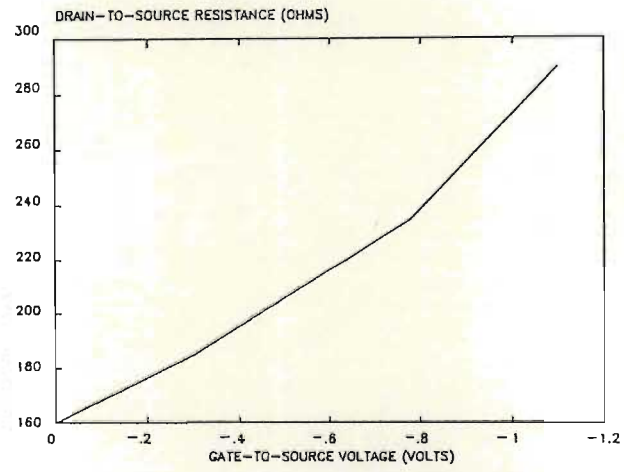
Table C-1. Transistor Model Component Values (V_{ds} = 2.2 v.)



(A) Transconductance



(B) Gate-to-Source Capitance



(C) Drain-to-Source Resistance

Figure C-19. Circuit Parameters from Transistor Model as a Function of Gate-to-Source Voltage

Section C.4. Conclusions

A transistor test fixture has been made to measure devices in the lower microwave frequency range and software has been written to facilitate automatic de-embedded measurement. The automatic network analyzer operating under the control of a computer enables very rapid and accurate measurements. Data from such measurements has been used to design numerous circuits, primarily mixers and amplifiers, and computations based on the measured data are in excellent agreement with the test data on the circuits.

References

[C1] Pucel, R.A., Haus, H.A. and Statz, H., "Signal and Noise Properties of Gallium Arsenide Microwave Field-Effect Transistors," Advances in Electronics and Electron Physics, Vol. 38, pp. 195-265, 1975.

[C2] Sze, S.M., Physics of Semiconductor Devices, John Wiley and Sons, New York, pp 312-361, 1981.

[C3] Liechti, C.A., "Microwave Field-Effect Transistors," IEEE Trans. on MTT, Vol. MTT-24, No. 6, June 1976.

[C4] Bauer, R.F. and Penfield Jr.,P., "De-embedding and Unterminating" IEEE Trans. on MTT, Vol. MTT-22, No. 3, pp. 282-288, March 1974.

Appendix D

Quantum Mechanical Modelling

ABSTRACT

Quantum Mechanical Modelling

Solution of the Schrodinger wave equation for simple potential barriers is essential to the understanding of many quantum phenomena; however, extension of the quantum theory to real models is seldom done due to mathematical complexity. In this appendix the author presents a formalism enabling the solution of the wave equation for piecewise linear potentials. A computer program has been written to solve both closed system and barrier transmission problems in one dimension.

Table of Contents

Section D.1. Introduction

Virtually all quantum mechanical conduction mechanism problems can be formulated in terms of spatial potential distributions. The fundamental problem in semiconductor conduction is the infinite periodic lattice represented by cascaded potential wells (Kronig-Penny model [D1,D2]). The wells are the binding energy of the constituent atoms. The distance between the wells is the interatomic lattice spacing. Solution of the Schrodinger wave equation for this structure yields a probability distribution ($\psi^*\psi$) that is descriptive of various characteristics $\zeta(x)$ of the system so that the expectation value may be found from the integral

$$E(\ ) = \int_{-\infty}^{\infty} \zeta(x)\ |\Psi|^2\ dx$$

where x is the spatial coordinate.

The infinite potential lattice problem is usually considered for idealized square well models of constituent atoms and, as the solution for ψ even for this model is rather complex, the problem is solved only for the allowed conduction particle energy as a function of the crystal momentum. This solution then leads to the synthesis of material descriptors such as energy gaps and effective mass. Methods of analysis have been devised to evaluate these descriptors for real materials. The calculated and derived descriptors are strictly valid only for bulk (infinite lattice) materials.

Advanced material fabrication techniques are enabling the construction of devices that depend on very small geometries for their operational characteristics. The smallest of these geometries are presently measured in tens to hundreds of lattice constants. The behaviour of conduction particles in systems of such size can definitely not be described by bulk derived characteristics. Indeed, greatly modified bulk derived quantities are falling short of describing the behaviour of devices the size of a thousand lattice constants. A return to the first principles of solid state theory is possibly in order to reduce the increasing complexity of a bulk theory being continually updated to solve systems describable by the quantum mechanical wave equation.

In the following sections of this appendix the author proposes a straightforward method of modelling and analysing potential barrier problems.

Section D.2. Modelling

The hydrogen atom is the only quantum mechanical system that is readily definable and solvable. Solution of the wave equation for even slightly more complex problems requires the application of perturbation theory. The binding forces of multiple atoms and the internal atomic forces are usually simplified to a non-infinite potential well for the individual atom and a cascade of wells for the crystal problem. The model bears little resemblance to the actual r^{-n} atomic bonding [D3,D4] and the various types and combinations [D5-D7] of interatomic bonding; however, the deviation is compounded by assuming an infinite lattice for the solid state formalism. The method provides the framework for explaining qualitative performance but does not support design and synthesis with quantitative results.

Direct solution of complex barrier problems represents an extremely complex alternative. The author proposes a viable compromise between rough qualitative solutions and exact solutions. The basic proposal is for the accurate potential barriers to be modelled by rectangular potential barriers of width and height sufficient to approximate the exact barrier as closely as is required to obtain the desired accuracy. A formalism for the solution of this piecewise linear model is developed in Section D.3.

To devise a general numerical method for the solution of the Schrodinger wave equation, thus obtaining the probability distribution for a particle within a defined system consider the non-infinite potential well problem defined in Figure D-1. This roughly approximates in one dimension the electron binding energy of an atom.

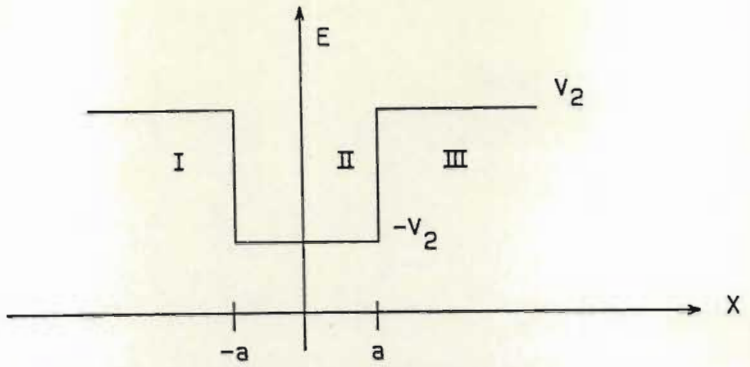


Figure D-1. Non-Infinite Potential Well

The well is defined for three regions. In region I the barrier height is V_2 as it is also in region III. The region II height is V_1.

For an atom, such as hydrogen, the binding energy for the electron is less the further the electron is removed from the nucleus. The walls of the square well problem should then be functions of $1/x_n$. The actual potential curve can be broken into numerous rectangular barriers as shown in Figure D-2 to model the actual distribution.

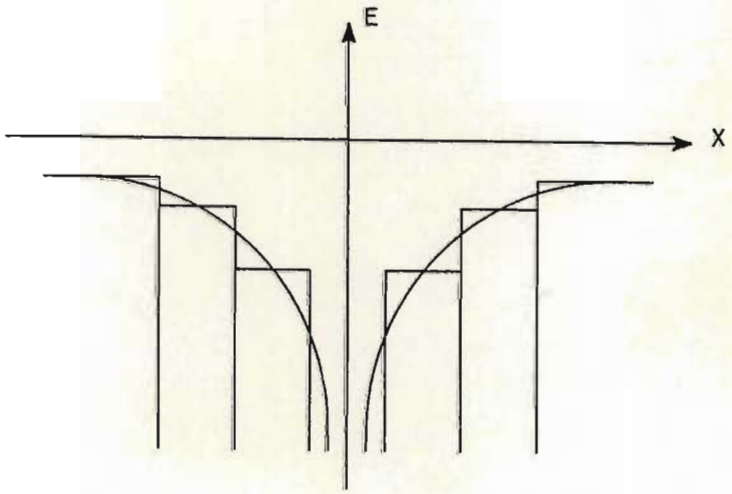


Figure D-2. Model of Atomic Binding Energy

The solution of the rectangular barrier case will not be as accurate as that for the exact curve but if greater accuracy is desired more barrier segments can be used.

Section D.3. System of Equations

As discussed in Section D-2 any potential distribution can be modelled with segments of constant potential barriers. (At this point only time independent one-dimensional solutions will be considered. Extension to two-dimensional time dependent systems will be under-taken in the near future.) The set of equations to be configured will assume a constant potential level from minus infinity to x = 0 of V_0 and n barriers to the right of x = 0 each of potential V_n with the last barrier extending to infinity at a level V_m.

The time invariant Schrodinger wave equation is

$$\frac{d^2\psi_n}{dx^2} + \frac{2m}{\hbar^2}(E-V_n)\,\psi_n = 0 \qquad \text{eq.(D-1)}$$

If the particle energy is greater than the barrier potential ($E>V_n$) then a general solution for the rectangular barrier is

$$c_n = A_n \exp(jk_n s) + B_n \exp(-jk_n x) \qquad \text{eq.(D-2)}$$

where $$k_n^2 = \frac{2m\,(E-V_n)}{\hbar^2} \qquad \text{eq.(D-3)}$$

A_n and B_n are complex:

$$A_n = AR(n) + j\,AI(n)$$

and $$B_n = BR(n) + j\,BI(n).$$

By letting $\exp(jk_n x) = \cos k_n x + j \sin k_n x$ the real part of ψ is

$$\text{Re}\{\psi_n\} = AR(n)\cdot\cos k_n x - AI(n)\cdot\sin k_n x + BR(n)\cdot\cos k_n x + BI(n)\cdot\sin k_n x \qquad \text{eq.(D-4)}$$

and the imaginary part is

$$\text{Im}\{\psi_n\} = AR(n)\cdot\sin k_n x + AI(n)\cdot\cos k_n x - BR(n)\cdot\sin k_n x + BI(n)\cdot\cos k_n x. \qquad \text{eq.(D-5)}$$

If the particle energy is less than the barrier potential ($E<V_n$) then k_n is imaginary and

$$\psi_n = A_n \exp(k_n x) + B_n \exp(-k_n x) \qquad \text{eq.(D-6)}$$

where

$$k_n^2 = \frac{2m\,(V_n - E)}{\hbar^2} \,. \qquad \text{eq.(D-7)}$$

Again, A_n and B_n are complex so

$$\text{Re}\{\psi_n\} = AR(n)\, \exp(-k_n x) + BR(n)\, \exp(k_n x) \qquad \text{eq.(D-8)}$$

$$\text{Im}\{\psi_n\} = AI(n)\, \exp(-k_n x) + BI(n)\, \exp(k_n x). \qquad \text{eq.(D-9)}$$

The solution to the wave equation within each barrier must be equated to the equations in adjacent barriers at the interfaces. The real and imaginary components can be equated individually so that

$$\text{Re}\{\psi_n\} = \text{Re}\{\psi_{n+1}\} \qquad \text{eq.(D-10)}$$

and

$$\text{Im}\{\psi_n\} = \text{Im}\{\psi_{n+1}\} \,. \qquad \text{eq.(D-11)}$$

The derivatives must also be equated at the barrier interfaces. The derivatives of Equations D-4 and D-5 are

$$\frac{d}{dx}\,\text{Re}\{\psi_n\} = -\,AR(n) \cdot k_n \sin k_n x - AI(n) \cdot k_n \cos k_n x$$
$$- BR(n) \cdot k_n \sin k_n x + BI(n) \cdot k_n \cos k_n x \qquad \text{eq.(D-12)}$$

and

$$\frac{d}{dx}\,\text{Im}\{\psi_n\} = AR(n) \cdot k_n \cos k_n x - AI(n) \cdot k_n \sin k_n x$$
$$- BR(n) \cdot k_n \cos k_n x - BI(n) \cdot k_n \sin k_n x \qquad \text{eq.(D-13)}$$

The derivatives of D-8 and D-9 are

$$\frac{d}{dx}\,\text{Re}\{\psi_n\} = -AR(n) \cdot k_n \exp(k_n x) + BR(n) \cdot k_n \exp(-k_n x) \qquad \text{eq.(D-14)}$$

and

$$\frac{d}{dx}\,\text{Im}\{\psi_n\} = -AI(n) \cdot k_n \exp(k_n x) + BI(n) \cdot k_n \exp(-k_n x). \qquad \text{eq.(D-15)}$$

These equations are equated at adjacent boundaries so that

$$\frac{d}{dx} \quad \mathrm{Re}\{\psi_n\} = \frac{d}{dx} \quad \mathrm{Re}\{\psi_{n+1}\} \qquad \text{eq.(D-16)}$$

and

$$\frac{d}{dx} \quad \mathrm{Im}\{\psi_n\} = \frac{d}{dx} \quad \mathrm{Im}\{\psi_{n+1}\} \; . \qquad \text{eq.(D-17)}$$

Each boundary then yields four equations with eight variables. For an arbitrary set of barriers as in Figure D-3 the terms AR(0) represent a wave travelling from left to right and the terms BR(3) and BI(3) are for a wave incident on the barrier set from the right; therefore, a matrix equation can be configured as follows:

$$[A] \cdot [B] = [C]$$

where A is the coefficient matrix for the barriers with the two incident waves composing the C matrix. B is then the column matrix composed of the AR, AI, BR and BI terms. For a barrier problem with an incident "test particle" C is non-zero and the objective is to solve for B and insert the values back into the equations for . This then solves for a barrier problem. The solution for B is $[B] = [A]^{-1} \cdot [C]$.

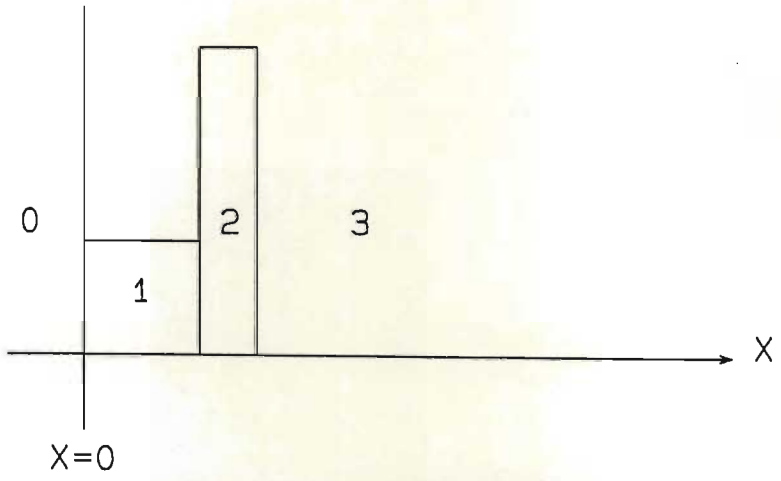


Figure D-3. Arbitrary Barrier Set

For a problem with no incident particles C is identically zero and the system has no valid solution unless the determinate A is zero. Energy values where A is zero are "allowed energies." To solve for these

energies a range of values is swept and the derivative of the solutions versus the energy level is computed. The minimas of the derivatives are further swept until the derivative approximates zero.

To test actual transmission of a current carrying particle through a lattice an electric field is applied thereby "tilting" the static barrier and an incident particle is introduced; that is, AR(0) and AI(0) are non-zero. The system of equations is solved for AR(n) and AI(n) to compute the probability of the particle being at the exit of the set of barriers.

Section D.4. The computer program

The system of equations was programmed by the author into a computer. The data entry is by interactive terminal connection. The program queries the operator to enter potential levels and intervals to define the barriers of the piecewise linear model. Statement of the incident/transmitted probabilities establishes the method of data processing the wave function. If there are no defined unity probabilities (incident electrons) the coefficient matrix is tested for energy levels of valid solutions. If there is an incident electron defined the wave function is computed as a function of energy. In both cases the derivative of the determinate with respect to energy is required to establish validity of a solution.

The simplied flow diagram for the program is shown in Figure D-4. The data defining the problem is entered. The coefficient matrix is computed. If the problem has no incident particles [C] equals zero and if the determinate is zero a valid energy level has been tested. The next energy level is computed and tested. If the problem was to test for transmission of an incident particle the determinate of [A] must be non-zero for a valid solution. If this is the case [C] and then [B] is computed enabling the calculation of $\psi(x)$. The energy level is then incremented and the process repeated.

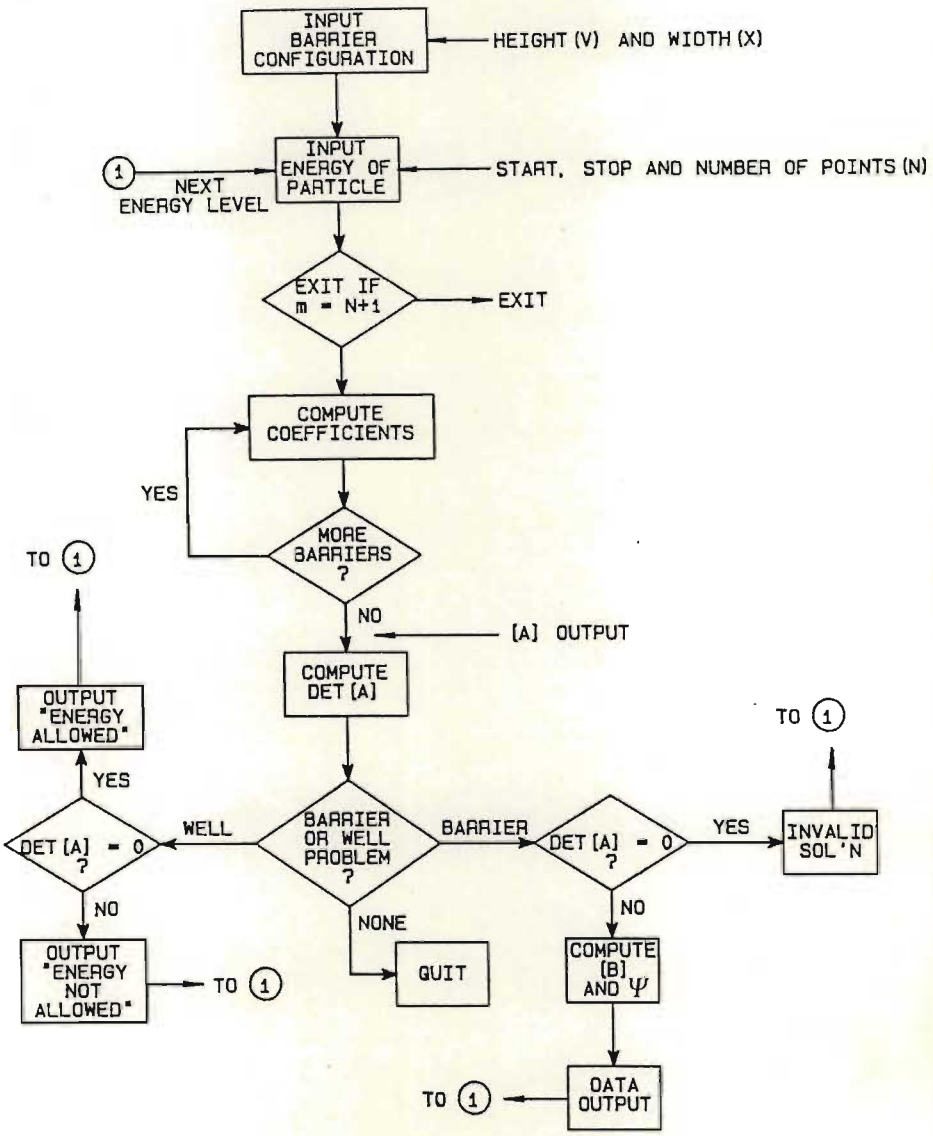


Figure D-4. Quantum Mechanical Modelling Simplied Program Flow Diagram

Section D.5. Conclusions

A formalism for the use of the digital computer for the numerical computation of solutions to the Schrodinger wave equation has been proposed and a program for one dimensional problems has been written by the author. Application of this technique to areas such as semiconductor

junctions and thermonic emission can lead to models more exactly describing observed phenomena thus increasing the understanding of potential structures causing the phenomena. Extension of this method into two dimensional structures will aid in the solution and explanation of planar heterojunction problems. The two dimensional method should be useful in 2DEG HEMPT regions and some FET channels. Further extension to three dimensions will be helpful in the analysis of short channel FET devices.

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APPENDIX E

Automatic Network Analyser

Appendix E.

Table of Contents

Section E.1. Introduction

The HP8510 network analyser has been used extensively by the author in developing the circuits analysed in this thesis. The following description of the principles and operation of the analyser is provided for the information of the reader and for completeness of this thesis.

The network analyser (Plate E-1) is basically a multi-channel phase coherent receiver with a tracking signal source. When interfaced with various power splitters and couplers the channels can simultaneously measure forward, reverse and transmitted waves. As the phase and amplitude information is available on each channel parameters of the device being measured can be computed. The most common configuration measures the forward and reflected waves to and from a two port device. From these measurements the two port scattering matrix can be computed.

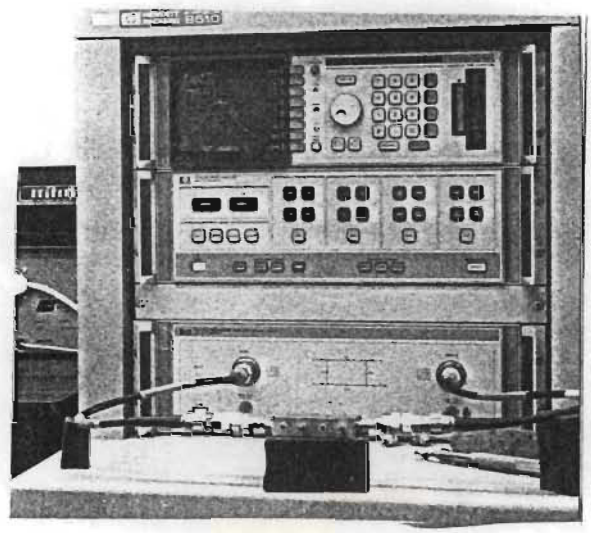


Plate E-1. HP8510 Automatic Network Analyser

The automatic network analyser performs these operations under the supervision of a computer requiring the operator to input instructions relating to the desired data. The computer performs the routine "housekeeping."

The use of computers also facilitates extensive improvement in measurement accuracy by measuring known high quality components, calculating non-ideal characteristics of the measurement system, and applying corrections derived from these measurements to data from other devices. In other words, the accuracy of a known component can be transferred to the measurement accuracy of an unknown component.

With the measurement frequency accurately known and the phase and amplitude response measured and corrected the Fourier transform of the frequency domain yields the time domain response. A very useful measurement of this type transforms the S_{11} frequency domain to a time domain response with the same information as time domain reflectometry.

Section E.2. System Description

The simplified block diagram of the HP8510 is shown in Figure E-1. There are four channels fed from the test set. The inputs are down converted first to 20 MHz and then to 100 KHz before being routed to phase detectors. The first conversion oscillator is followed by a comb generator and the oscillator is phase locked to the mixer output so the unit will frequency track the test source. The second local oscillator is the crystal controlled reference source.

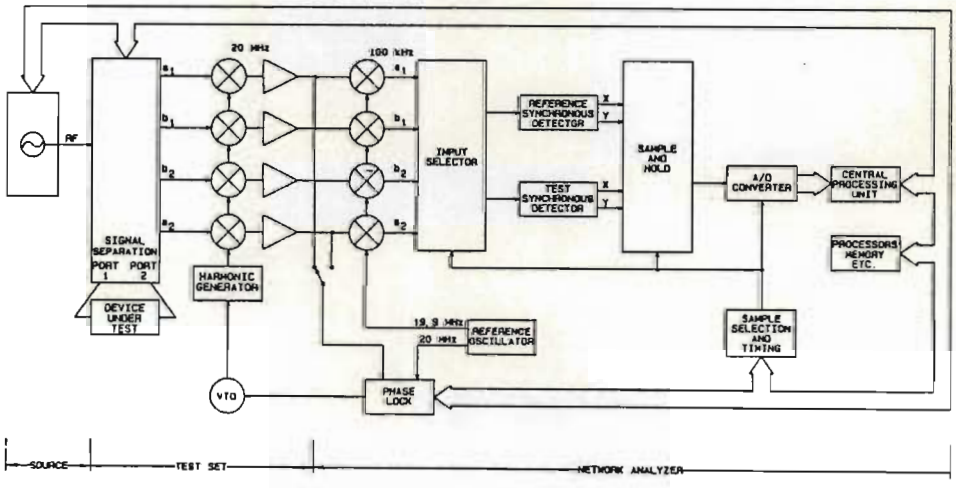


Figure E-1. Simplified Block Diagram of the Network Analyser (HP8510)

The outputs of the synchronous detectors supply the raw data to be converted to a format compatible to the computer. Corrections and manipulation of the data to the required output form is then done by the processors.

The test set supplies the first mixer inputs with the sampled signals necessary to make the desired measurement and there are many possible configurations. The most versatile and also the unit used for the measurements in this thesis is the two-port scattering matrix test set. This unit enables full two port measurements to be made without the necessity of changing cable connections to the device. The simplified block diagram of the HP8514A test set is shown in Figure E-2. The RF input is switched between port (1) and port (2) measurements. In each case the RF is split into a reference and test channel. The reference channel is fed directly to a reference channel converter. The test channel feeds the device under test by way of a directional coupler. The coupler output sampling the reflected power is routed to the test channel converter. Sampled components of incident and reflected power to both the input and the output of the test device are available for processing.

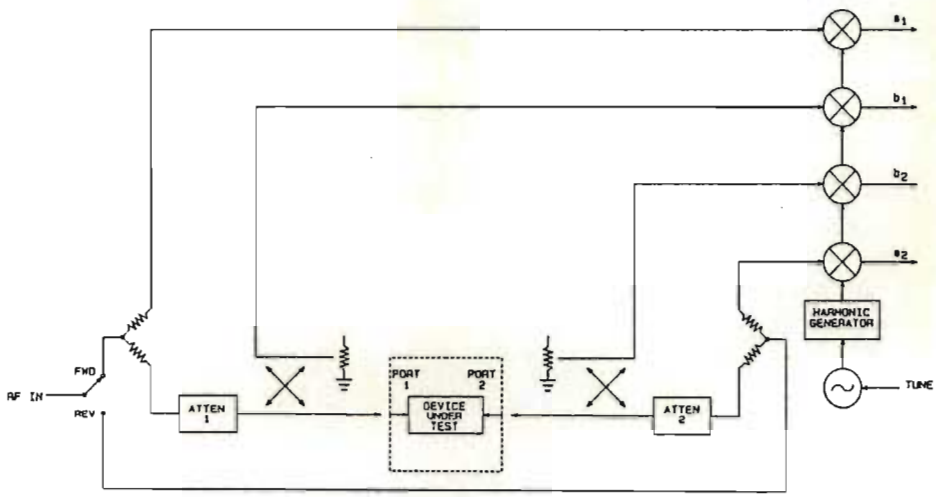


Figure E-2. Simplified Block Diagram of the S-Parameter Test Set (HP8514A)

Section E.3. Computations

Various levels of computations in the HP8510 are assigned to different processors within the equipment to optimise computational capability and speed to the desired measurement. For example, error correction is virtually a real time process due to the use of an array processor.

Section E.3.a. Error Correction

In a full two port measurement twelve error terms can be identified. Referencing Figure E-3 and associating the subscript F with measurements made from port (1) and R with those from port (2), the terms are defined as follows with S subscripts A meaning actual and M meaning measured value:

E_D - Non-ideal directivity of signal separation device.

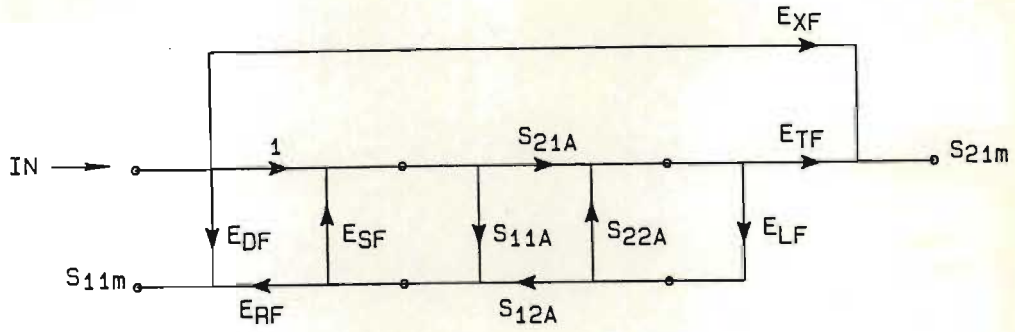
E_R - Tracking error in frequency response between test and reference signal paths.

E_S - Source mismatch causing part of reflected component to return as incident signal.

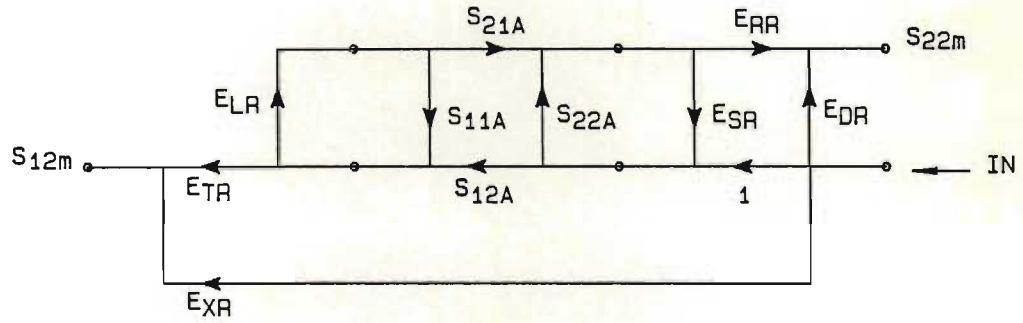
E_L - Load mismatch causing some of the device output to be reflected back into the device.

E_T - Transmission tracking between input and output.

E_X - Isolation between input and output.



(a) Forward



(b) Reverse

Figure E-3. Definition of Error Terms*

*HP8510 manual page 71.

Error correction equations are then derived in terms of these sources of error that are measured during system calibration by using well defined (nearly ideal) reference components. The correction factors when applied to measured quantities yield the actual error corrected frequency domain values.

Section E.3.b. Time Domain Analysis

By measuring the vector frequency response H(f) of a circuit at specific frequencies, the Fourier transform can be used to compute the time domain response h(t). The HP8510 uses the Chirp-Z FFT for this computation.

There are two modes of time domain operation. The first, Low Pass Mode, simulates conventional time domain reflectometry (TDR) with either an impulse or step driving response. The usual TDR requirement that the circuit have a very low frequency response applies and harmonic relationship of the test frequencies is necessary. The more frequencies used and the higher the upper frequency the better will be the resolution.

A unique implementation of time domain response for network analysis is found in the Band Pass Mode in that devices with other than a low pass frequency response can be analysed. Although the Band Pass Mode response contains none of the impedance information that can be obtained from the Low Pass Mode response the "return" is proportional to the average reflection coefficient across the sampled frequency range for measurements of S_{11} and S_{22}. Likewise, in S_{12} and S_{21} measurements the time axis represents average propagation time and the magnitude is proportional to average gain or loss.

Section E.4. Conclusion

The HP8510 Automatic Network Analyser represents the state of the art in microwave measurements at this time. Not only are very accurate conventional frequency domain measurement made in minimal time but options such as time domain analysis facilitate new possibilities for fault finding and device specification.

Reference

HP8510 Network Analyser Operating and Service Manual, Volume 1, Basic Measurements, pp. 1-150, Santa Rosa, March 1984.