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Harmonic and Current Ripple Analysis of Flying Capacitor Multilevel Inverters with Active Control Algorithms

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DECLARATION 1 - PLAGIARISM

As the candidate's Supervisor I agree/do not agree to the submission of this thesis.

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DETAILS OF CONTRIBUTION TO PUBLICATIONS:

Publications

K. Jones, and A. Saha, "Analysis of ripple current in pulsewidth modulation for flying capacitor multilevel inverters," *26th Southern African Universities Power Engineering Conference,* pp. 234-239, Jan. 2018.

K. Jones, and A. Saha, "Comparative analysis of an optimised modified phase shifted modulation strategy for flying capacitor multilevel inverters," *26th Southern African Universities Power Engineering Conference,* pp. 240-245, Jan. 2018.

K. Jones, and A. Saha, "Analytical modelling of ripple current in pulsewidth modulation controlled flying capacitor multilevel inverters" *Submitted to IET, Transactions on Power Electronics*. currently under review.

K. Jones, and A. Saha, "Comparative analysis of an optimized phase shifted modulation strategy for flying capacitor multilevel inverters" *Submitted to Journal of Electrical Systems*. currently under review.

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To my family, thank you for your support, patience and always guiding me towards success.

ABSTRACT

This thesis is focused on enhancing flying capacitor multilevel inverters by determining the most optimal pulsewidth modulation control strategy to reduce current ripple and subsequently filter requirements and improve balancing mechanics of the flying capacitors. The two specific control methods of interest within the research work are the phase shifted and phase disposition pulsewidth modulation. There stands a cloudy consensus on the optimal of the two techniques, some researchers cite phase shifted a more suitable technique for its natural balancing mechanics, while others cite phase disposition as superior due to the improved harmonic performance. The purpose of this research is to identify and describe the aptness of each technique in terms of capacitor balancing, harmonic performance and efficiency; to clarify when either technique should be chosen over the other. Analysis of the current ripple is achieved by well-known methods for calculating current ripple in two-level inverters combined with analytical models of representing flying capacitor multilevel inverters. Using this analysis it is shown that because of the greater effective switching frequency of the phase shifted strategy it has reduced output current ripples and harmonic power losses over the phase disposition strategy, which is heavily dictated by the number of levels of the inverter. The research work additionally proposes a closed-loop modified phase shifted control strategy focused primarily on restoring voltage balance. The algorithm selects switching states bounded by times where no capacitor charging/discharging occurs. Through this strategy, it is shown that phase shifted and phase disposition can achieve similar balancing characteristics when operated optimally. Additionally, it is shown that the phase shifted strategy has a fraction of the inductor filter requirements. The critical question of which methodology is superior was found to not have a simple answer; however the circumstances where one method may be more beneficial than another are highlighted and discussed.

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LIST OF ABBREVIATIONS

CHB:	Cascaded H-bridge
CRPWM:	Carrier redistribution pulsewidth modulation
FC:	Flying capacitor
FCMLI:	Flying capacitor multilevel inverter
MLI:	Multilevel Inverter
MVA:	Mega volt amp
MW:	Megawatt
NPC:	Neutral point clamped
PD-PWM:	Phase disposition pulsewidth modulation
PS-PWM:	Phase shifted pulsewidth modulation
PWM:	Pulsewidth modulation
RLC:	Resistor inductor capacitor
SVM:	Space vector modulation
SMC:	Stacked multilevel converter
THD:	Total harmonic distortion
VSI:	Voltage source inverter
WTHD:	Weighted total harmonic distortion

Chapter 1. Introduction

1.1 Introduction to research work

Multilevel inverters (MLI) have gained increasing popularity for high-power conversion systems over the past few decades because the semiconductor device requirements are a fraction of the converter voltage and power ratings. The flying capacitor multilevel inverter (FCMLI) is an attractive topology which can operate transformerless and uniformly distribute switching losses across all the switching devices. This topology has successfully made its way into industry in applications such as train traction drives, pumps in the water industry, medium voltage adjustable speed drives, and flexible alternating current transmission systems [1] [2]. Although it is a proven technology, the range of possibilities that MLIs offer is so large that there is continual research and development in this field. The FCMLI topology still faces many challenges as it is a rather complex scheme to optimally control, furthermore there is still many opportunities to improve it in terms of energy efficiency, capacitor balancing, harmonic performance, reliability, simplicity and cost.

1.2 Background

The basic concept of a MLI is to achieve high voltage power conversion through a combination of lower voltage semiconductor switches by synthesising a staircase voltage waveform. By increasing the levels of the inverter the staircase waveform has reduced harmonic distortion, but this usually comes with more complex control algorithms and introduces voltage imbalances. The MLI has several advantages over the conventional two-level inverter [1]-[4] which can briefly be summarized as:

- Output waveforms have much lower harmonic distortion hence they can operate at lower frequencies.
- Reduced dv/dt stresses therefore electromagnetic compatibility is reduced.
- Draws input current with low distortion.
- Reduced common mode (CM) voltage.

An abundant of MLI topologies have been proposed since there conceptualisation over four decades ago however the three fundamental MLI topologies which have been perused the furthest are the cascaded H-bridge (CHB), neutral point clamped (NPC) and the flying capacitor (FC) as summarized in figure 1.1. These are usually found in the medium-voltage high-power

range and are classified as voltage source converters. Additionally numerous control strategies have been developed for operating MLIs, ranging from sinusoidal pulsewidth modulation (PWM) multilevel selective harmonic elimination, and space vector modulation (SVM).

The CHB and NPC are both exceptional topologies with many applications in the MLI industrial field, however this research is focused only on the FC topology and more specifically the three, four and five-level as well as the stacked multilevel converter (SMC) as they are the most popular FCMLI variations observed currently by industry [1] [2].

The advantage of the FC over the CHB and NPC are [1]:

- Higher flexibility in synthesising the output.
- Increased possibility to control the DC-link voltage.

The disadvantages of the FC over the CHB and NP are:

- Higher number of capacitors.
- Capacitors are more to failure than the diodes of the NPC.
- Balancing of the flying capacitors is complex.

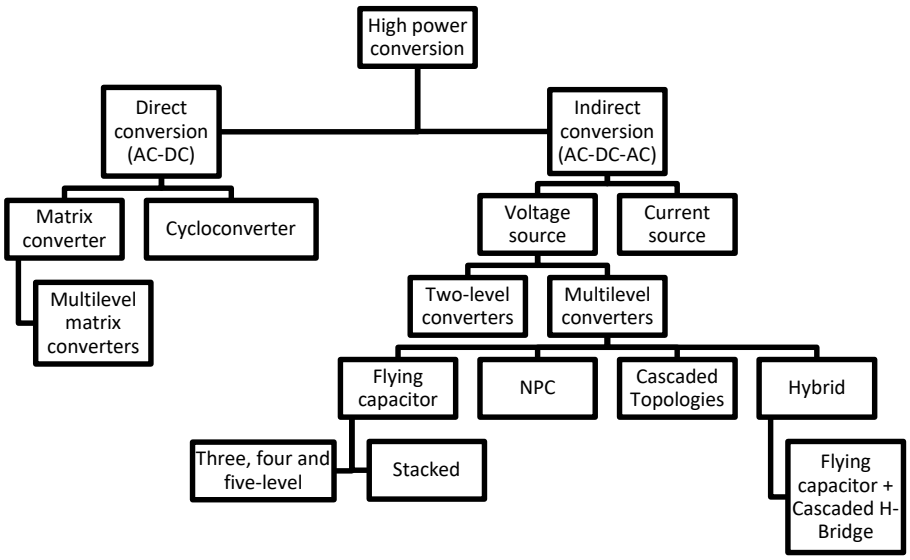

Figure 1.1: Classification of FCMLIs [4].

1.2.1 Basic operation

The structure of a five-level FCMLI is shown in figure 1.2. The inverter is comprised of power cells which consist of 2 complementary power electronic switches; hence if the upper switch is on the lower switch is open. For a *N*-level inverter *N*-1 power cells per phase are connected through FCs, labelled C_1-C_3 in figure 1.2. The FC's are considered voltage sources and are

responsible for the different voltage levels found in the inverter. In order for the converter to operate correctly the voltages of each FC must be maintained at its respective voltage level which are uniformly distributed amongst the capacitors. Hence the capacitors C_1, C_2 and C_3 would be maintained at $3V_{DC}/4$, $V_{DC}/2$ and $V_{DC}/4$ respectively. One of the main challenges faced with providing proper operation of the inverter is ensuring balanced distribution of the voltage levels [5] [6].

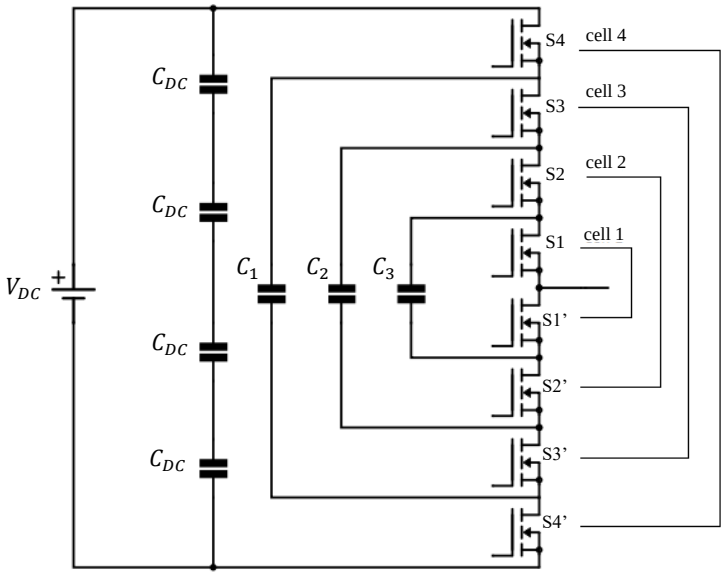

Figure 1.2: Single phase of a five-level FCMLI.

1.2.2 Control techniques

The simplest technique to control the FC voltages is natural balancing, achieved by switching the complementary power switching devices at the same duty cycle but phase shifted by $2\pi/(N\text{-}1)$ [7] [8] [9]. This is generally implemented by a carrier based method such as phase-shifted pulsewidth modulation (PS-PWM) as shown in figure 1.3. This technique uses three sinusoidal reference waveforms, one for each phase, of equal amplitude and frequency displaced by a phase difference of 120°, and N-1 triangular carrier signals of equal amplitude and frequency displaced by a phase difference of $360°/(N\text{-}1)$, one for every power cell of each phase. The cell gate signals are determined by comparing the carrier signals and the reference signal, when the carriers are larger the output to the gate is high and vice versa.

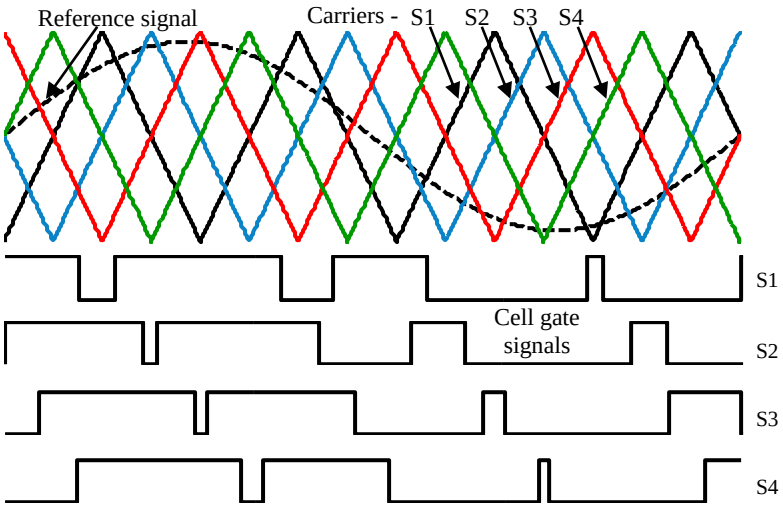

Figure 1.3: Five-level PS-PWM

A variant of this technique instead places its carriers in phase but vertically displaces them to equally occupy the modulation range as such is called phase disposition pulsewidth modulation (PD-PWM) as shown in figure 1.4. The gate signals within this technique are determined in the same fashion as PS-PWM but of course the switching pattern is very different hence the output voltage is synthesised in a completely different manner.

There are further variants of the PD-PWM strategy such as phase displacing the carriers above the zero reference with the carriers below by 180°, known as phase opposition disposition (POD-PWM) or phase displacing consecutive carriers by 180°, known as alternate phase opposition disposition (APOD-PWM) as are illustrated in figure 1.5. However PD-PWM is widely preferred for conventional MLIs as it produces the lowest distortion of the output waveform [6] [8] [9].

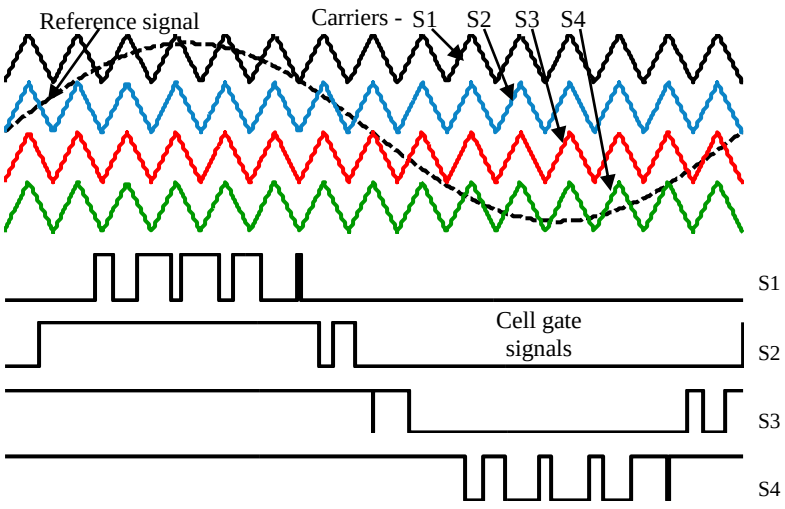

Figure 1.4: Five-level PD-PWM

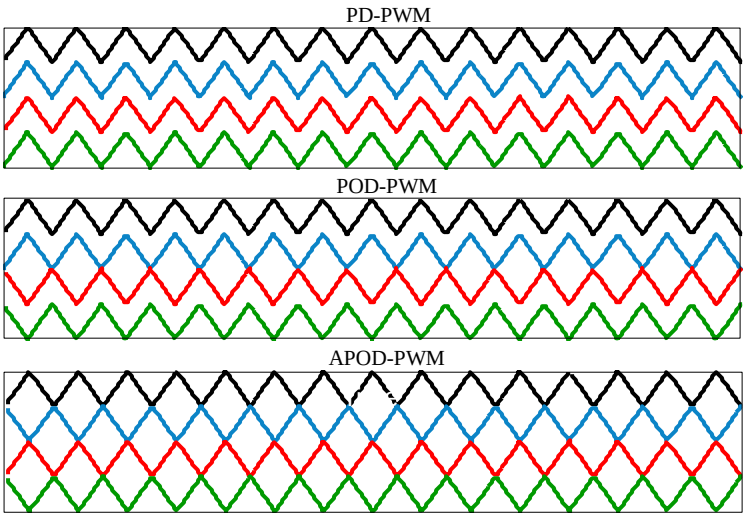

Figure 1.5: PD-PWM variants

The final carrier based method considered is carrier redistribution pulsewidth modulation (CRPWM) otherwise known as decode PD-PWM. It is a modified form of the PD-PWM strategy introduced early in the 21st century and reported to be the solution to the voltage imbalance problem of FCMLIs [10]. In this method the carriers are reconstructed to create the two-level switching cells states for each phase leg, accomplished by using a set of special trapezoidal waveforms [11] or by a state machine decoder [12]. The carrier shapes are illustrated in figure 1.6, the first carrier waveform is repeated for each carrier but phase displaced by 360°/(*N*-1).

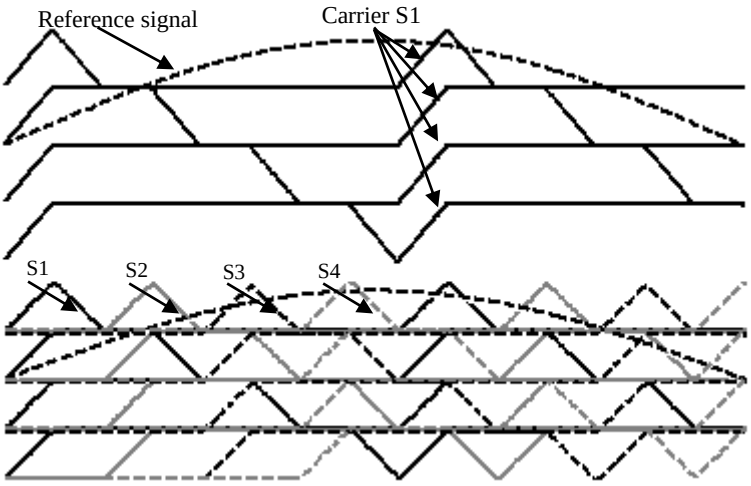

Figure 1.6: Five-level CRPWM

1.2.3 Flying capacitor balancing

The advantage of the PS-PWM strategy lies in that it evenly distributes the duty cycles of the power cells across the entire modulation range, this gives it natural balancing properties which is not the case for PD-PWM [1] [6] [9]. This phenomenon is illustrated through a five-level FCMLI controlled by both strategies in figure 1.7, here the PS-PWM strategy naturally will rebalance the capacitor voltage unbalance caused by the step change in DC supply however the process is slow and can be improved. In contrast the capacitor voltage using PD-PWM begins deteriorating.

The purpose of CRPWM is to rectify these flaws of PD-PWM, by reconstruction the carriers the strategy can gain and moreover improve on the natural balancing of PS-PWM [6] [11]. Subsequently using CRPWM the benefits of PD-PWM can be exploited.

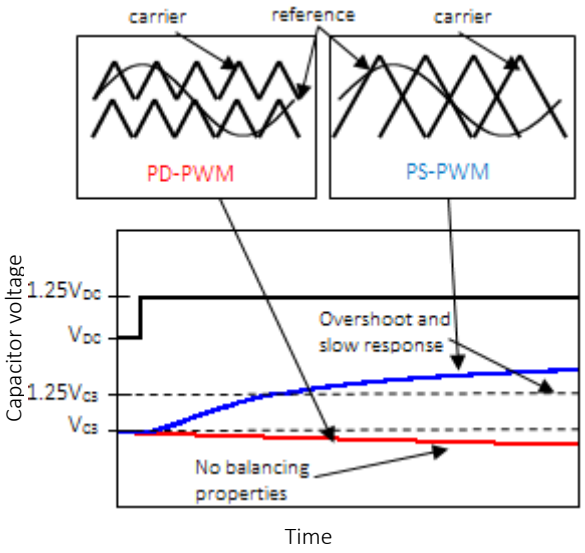

Figure 1.7: Natural balancing properties of PD-PWM and PS-PWM

1.3 Research questions

What is the optimal PWM control strategy for FCMLI operation? Why is there varying opinions on the answer to this question found in literature? Finally, are simpler active control algorithms a viable solution to FCMLI control?

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1.4 Thesis aims and objectives

- To clear the uncertainty that currently exists in the optimal control strategy for FCMLIs.
- To develop analytical current ripple solutions to the three primary carrier based PWM control methods for FCMLIs.
- Determine through simulations and analytical solutions the optimal control strategy for FCMLIs in terms of balancing performance, total harmonic distortion (THD), current ripple, efficiency and cost.
- Investigate the viability of simpler active control algorithms for FCMLIs.

1.5 Outline of chapters

Chapter two of this dissertation reviews the relevant literature regarding FCMLIs, specifically the current state of art of the topology in commercial applications and the preferred methods of control. Additionally the efforts towards active and natural balancing control methods are reviewed. Chapter 3 provides the methods and tools utilised throughout the dissertation which include analytical and simulation models.

Chapter 4 is the preliminary research steps undertaken, here simulations of the control techniques are provided to form the basis of the main research. The theory is verified and some propositions are formed. Additionally a simpler active control strategy is presented.

Chapter 5 provides evaluation and analysis of the main research findings of the dissertation. Finally Chapter 6 concludes the research work with recommendations for future work.

Chapter 2. Literature Review

2.1 Introduction

The increasing popularity of MLIs for high-power conversion systems over the past few decades has produced a flourishing research environment where the technology is constantly advancing [1] [2]. The FCMLI is arguably the least preferred topology, with its main applications only found in train traction drives and pumps in the water industry. This is mainly because the FCs are more prone to failure compared to the other components and the challenge of balancing the FCs creates barriers for this topology [2]. However there is substantial research supporting this topology by some of the leading researchers in this field such as Brendan Peter McGrath and Donald Grahame Holmes signifying that there still lies merit to advancing the topology.

2.2 Flying capacitor multilevel inverters state of the art

Besides train traction drives and pumps the FCMLI topology has found limited application in medium-voltage drives where it was first industrially developed in the 1990s [13]. The four-level configuration for example, was developed for the ALSPA VDM6000, a medium-voltage power drive system that can operate a 3.3 kV motor up to 4.6 MVA or 6.6 kV up to 9.2 MVA [14]. However the complexity of balancing the FCs and the high number of capacitors required are the main drawback of this topology for medium-voltage drives, consequently they are not under production [2].

To overcome some of the drawbacks of the FC topology a variation called the SMC was introduced early in the 2000's [15]. By placing two conventional FCMLIs atop the other a SMC could reach higher voltage levels without the increased complexity of balancing the FCs which is usually associated with higher levels of this topology. By achieving higher voltage levels the voltage stresses on the switching devices and FCs can be reduced. The main hindrance on the SMC is the increased number of capacitors required which appear to outweigh its benefits; hence it has not yet found much industrial applications [2].

2.3 Modulation control methods

The primary modulation strategies which are applicable to FCMLI are PWM based methods and SVM methods. SVM is superior in terms of producing lower THD levels, providing a wider modulation range and its ease of implementation however PWM based methods can be favourable in utilising the redundancy in switching states producing superior FC balancing mechanics.

2.3.1 PWM based methods

PD-PWM and PS-PWM are the two natural extensions of carrier based sinusoidal PWM for the MLI control. The PD-PWM method is often cited by researchers as superior since it leads to less distortion of the line voltages [1] [16], the reasoning behind this common acceptance can be tracked down to the reputable work of Brendan Peter McGrath and Donald Grahame Holmes [9]. Their research provides profound mathematical analysis on the harmonic performance of PS-PWM and PD-PWM which identified PD-PWM as the superior modulation technique both in terms of output waveform distortion and FC balancing mechanics. The former is the result of in phase carriers compared to PS-PWM and the latter is a result of larger differential-mode current harmonics. It's important to note that these findings assume purely resistive loads without considerations of the current waveforms for resistive-inductive loads. A study considering the current waveform in [17] identified that PS-PWM may in fact have lower current THD levels. These findings were only shown through simulations and required further investigation before the hypothesis could be proved.

In order to optimise the PD-PWM strategy a technique termed decoded PD-PWM otherwise known as CRPWM exists. The CRPWM strategy reconstructs the carrier signals by utilising the redundancy of switching states in FCMLIs to distribute duty cycles and balance switching losses; additionally it advances the PD-PWM strategy to have natural balancing properties [18]. It has the least harmonic content for the same reason as PD-PWM however causes fluctuation of the FC voltages as the carriers are not utilised equally within a cycle. This causes unequal charging and discharging of the FCs and the voltage does not become zero during a switching period. A method for overcoming this problem was proposed in [11], here, compensation of the unbalanced quantity of charging/discharging is rectified by symmetrically disposing carriers of each band at every fundamental period during the next fundamental period.

Regardless of the evidence supporting PD-PWM there are still many researchers who cite PS-PWM as the superior technique for operating FCMLIs for its natural balancing properties among other reasons. From a practical point, according to [1], the improved harmonic performance of PD-PWM is negligible in high-frequency applications since the harmonic content will be filtered by the load. Therefore PS-PWM is considered the only real commercial modulation scheme applicable for FCMLIs, as the industry trend exhibits. In the following papers [1] [2] [19] PS-PWM is cited as the preferred strategy for FCMLI control.

Clearly there is contradicting opinions on the optimal control strategy for FCMLI operation. An explanation for this may be that CRPWM and its benefits are not well known within industry. This could be because the benefits found in any realistic scenario may be too small to warrant the added complexity of the technique. Nevertheless, if the CRPWM strategy outperforms PS-PWM in every regard then industry should exhibit a favourable trend towards it.

2.3.2 Natural balancing vs active control

The necessity to maintain voltage balance within FCMLIs has led to the development of a variety of control techniques. The two main types of control are natural balancing and active control methods. Natural balancing or ‘open loop’ control refers to methods which balance the FCs by ensuring the duty cycle of the switching cells within the algorithm are equal [9] [20]. This method generally results in a slow transient response to dynamics and often requires additional components, such as RLC balance boost circuits, to operate satisfactory.

There have, however, been efforts to improve the natural balancing properties of some open loop techniques as in [21] it was proposed that switching states within the PS-PWM strategy could be modified to achieve faster balancing of the FCs. Specifically increasing the amount of states resulting in zero output voltage would guarantee faster balancing. In order to implement this strategy the following requirements were met:

- States were modified to switch to the nearest levels to improve voltage quality.
- Consecutive switching states would only change the state of one switch in order to reduce switching losses.
- Balanced duty cycles of switching pairs.
- Distribution of switching losses between switching pairs.

Following these criteria the proposed method was able to produce faster balancing dynamics of a five-level FCMLI while maintaining the optimal voltage quality and equally distributing

switching losses across the switches. Additionally it was identified in this paper that good characterization of the load is required to obtain correct theoretical values.

The second group of control methods is based on a closed-loop approach. In this method the converters switching pattern is modified in real time according to the voltage imbalance readings taken by the system. This method however, has some major drawbacks which usually hinder its applications [1] [2], these including:

- Expansion of the algorithms to higher level converters can be intricate.
- Highly dependent on circuit parameters.
- Prone to increased harmonic content, switching losses and *dv*/*dt* spikes.
- Overly complex algorithms.
- Require stored information such as lookup tables.

Thus explaining why the idea of actively controlling the FC voltages has not gathered major attention by researchers. Regardless it has been presented in a limited number of research papers. Specifically, in [22] a feedback control scheme was proposed based on the concept of adjusting duty cycles proportional to the unbalanced voltage and with relation to the output current. However, this was specific to three-level converters which consist of only one FC. There is a more elaborate relationship between the FC voltages and the switching pattern for higher-level converters requiring complex control algorithms to operate the nonlinear system.

An alternate method was proposed in [23] which was based on the adjustment of switching times of selected switching states to maintain the capacitor voltage balance without adversely affecting the system's performance. By properly selecting the adjusted switching states, this method demonstrated how capacitor voltages can be controlled independently without introducing any extra harmonic distortion. This is the most flexible of the discussed approaches, however expanding the algorithm to higher levels or altered inverters will be tedious and problematic.

Finally there also exists the idea of correcting the voltage imbalance by introducing a corrected modulation waveform through the injection of square wave signals [24].This method showed that a square wave could be injected into the normal modulation signal wave with the same phase shift as the phase load current, based on a simple control algorithm, to regulate the FC voltages. Furthermore the injection of the square wave had very little effect on the output wave distortion.

Although there have been some promising applications for actively controlling the FC voltages, it is still very much an underdeveloped field. The FC topology has found very limited industrial applications as the added capacitors are considered a drawback, subsequently the added complexity of active control is likely viewed as unnecessary hence the preference towards the simpler natural balancing route of PS-PWM and CRPWM.

2.3.3 Space vector modulation

MLIs have many degrees of freedom, meaning that there are multiple arrangements of switching states that result in the same output; this is especially the case for FCMLIs as this topology has more flexibility in synthesising the output waveform compared to the CHB and NPC topologies. The SVM method has the potential to be one of the most effective strategies for FCMLI control as it can utilise the switching redundancies of the topology which is not always fully exploited by carrier based methods. Hence there has been attractive development of this field specific to FCMLI control in recent years. A general SVM-based scheme is divided into three stages [25]:

1. Switching states or vectors are selected based on an algorithm of the scheme. This determines the harmonic content and the switching losses of the system.
2. The duty cycles of each vector are calculated to achieve the desired reference over a time average
3. The sequence in which the vectors are generated is determined

A trend was observed amongst the contributions towards SVM development [1] [25], in general, they pursue one or more of the following goals:

- Reducing switching frequency.
- Reducing computational costs.
- CM voltage elimination.
- Lower THD.
- Operating unbalanced systems.
- Improving FC balancing mechanics.
- Output current ripple reduction.

One attractive development proposing to resolve many of the FC topology drawbacks can be found in [26] where an effective closed-loop SVM based algorithm capable of controlling the FC voltages of any level FCMLI is presented. This method uses a fast-paced computationally algorithm which does not change with increasing number of levels. Although it is promising this approach needs to be properly compared with other PWM methods to perceive its

practicality. Since no such data exists it is difficult to fully determine the effectiveness of this method.

Despite all the reported development in this field, according to [1] currently SVM-based MLIs are not the preferred modulation scheme found in industrial applications. A plausible explanation may be that manufacturers prefer the proven technology and simplicity of carrier-based PWM strategies over new methods that have advantages but require elaborate control system which are difficult to implement.

2.4 Harmonics and current ripple

The continual endeavour to optimise MLIs has brought about the need to consider the degree to which undesirable harmonics exist. Conventionally THD and weighted total harmonic distortion (WTHD) are used as the basis of comparison for modulation strategies, however analysis of peak-peak current ripple (I_{PP}) in voltage source inverters (VSI) has received much attention by researchers in recent years as a means to reduce power losses and waveform distortion [27]-[30]. The majority of this research is centred on two-level inverters controlled by discontinuous PWM methods with little extension into MLIs.

Minimising current ripple in applications such as MW adjustable speed drives is key to reducing noise and losses both within the PWM inverter and the load [28]. Much of the recent studies in this field focus on minimising current ripple and switching losses, as in [31] [32] [33] this is achieved through the method of controlling the carrier switching period which is varied based on the pattern of total current ripple. Additionally the studies in [28] proposed a method for calculating maximum peak to peak current ripple based on the location of the reference signal with relation to space vector transforms. This was used to accurately predict the current waveforms of a VSI controlled induction motor. There has also been thorough analysis of utilising the superior high modulation range performance of discontinuous PWM for minimising current ripple in two-level VSIs [27] [28] [34].

Mitigating harmonics and output current ripple is often the centre of many a research paper, as this subsequently reduces filter costs and ensures the converter adheres to regulations. Any grid connected application will require some form of harmonic filtering, some more advanced techniques involve combinations of inductor-capacitor filter designs [35], while the rudimentary practice is the inductor sizing found at the load.

2.5 Balance boost circuits

The balance boost circuit is a combination of RLC components designed to create an impedance for the CM currents when the FC voltages are unbalanced, rather than relying only on the unbalanced differential harmonics to create harmonic currents to rebalance the FCs. In [20] it was shown that a balance boost filter tuned to the sideband harmonics could drastically improve the balancing performance of both PS-PWM and CRPWM. It is reported that this method will produce the best balancing performance; of course these benefits will have to outweigh the added cost of the additional circuit components

2.6 Conclusion

There appears to be a disconnect between commercial manufacturing trends and research conclusions regarding control of FCMLIs. The natural balancing properties of PS-PWM strategy is preferred by industry despite many research developments pointing towards alternative methods such as CRPWM and SVM. As mentioned before this may be because manufacturers prefer the proven technology, alternatively it may be the varying conclusions given by different sources that are causing the uncertainty. There is a need to clear this uncertainty through comparative analysis of the proposed methods. Furthermore current ripple theory in the MLI field is underdeveloped with much of the research thus far focused on the conventional two-level inverters. Combining the well-known harmonic modelling theory with current ripple theory provides an opportunity to develop this field.

Chapter 3. Methodology

The two fundamental variations of carrier-PWM techniques within MLI control differ only by displacing carrier signals one atop (PD-PWM) or besides (PS-PWM) the other. There stands a cloudy consensus on the optimal of the two techniques for the operation of FCMLIs, some researchers site PS-PWM a more suitable technique for its natural balancing mechanics, while others site PD-PWM/CRPWM as superior due the improved harmonic performance. The purpose of this research is to identify and describe the aptness of each technique in terms of capacitor balancing, harmonic performance and efficiency; to clarify when either technique should be chosen over the other.

This work takes an analytical as well as a simulation driven approach when drawing any conclusions. The analytical perspective is focused on theorising the expected current ripple of an inverter; this requires a foundation of Fourier series representation of FCMLIs. Each modulation technique is represented with a double Fourier harmonic series as described in this chapter. The simulations are undertaken in MATLAB where data collection of THD and FC balancing performance is taken.

3.1 Fourier representations

The model representing a single phase of an *N*-level FCMLI used throughout this work is shown in figure 3-1. The principle of a carrier based PWM inverter is placing (*N*-1) triangular carrier signals across the modulation range. Intersections between the reference signal and carrier signal then determine the phase leg switching functions $S_{q,k}$ which dictates the switching output waveform. It is well known that the switching functions of a MLI can be described with a double Fourier harmonic series [6] [20] [36]. If individual cell switching functions are defined as $S_{q,k}(t)$ where q represents each phase, $q \in \{a, b, c\}$, and k represents the voltage levels, $k = 1, 2, \dots, N-2$, and $S_{q,k}(t) \in \{0,1\}$, and M is the modulation index, then:

$$S_{q,k}(t) = \frac{|C_{00}|}{2} + \sum_{n=1}^{\infty}[|C_{0n}|\cos(n[w_0 t + \emptyset_q] - \delta_{0n})] + \sum_{m=1}^{\infty}\sum_{n-\infty}^{\infty}[|C_{mn}|\cos(m[w_c t + \emptyset_{c,k}] + n[w_0 t + \emptyset_q] - \delta_{c,k})] \quad (3\text{-}1)$$

Where w_0 and w_c, $\emptyset_q$ and $\emptyset_{c,k}$ are the frequency and phase offsets for the reference and carrier waveforms, respectively.

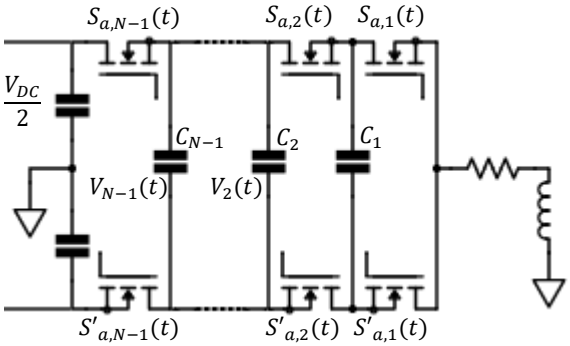


Figure 3-1: Single phase of a three phase N-level FC topology.

3.1.1 PD-PWM Fourier representation

The coefficients of equation 3-1 defined by C_{mn} represent the magnitudes of the baseband ($m = 0$), carrier ($n = 0$), and sideband ($m > 0\ and\ n \neq 0$) harmonics and must be evaluated for each modulation technique. Evaluation of these coefficients is undertaken by the principles of [6] [9] which requires deriving expressions for the switching cell carrier waveforms, shown for three-level PD-PWM in figure 3-2. These functions are then compared with the cosine reference signal shown in figure 3-3. As the reference crosses the boundaries defined by the rules of the particular modulation technique the (*x*,*y*) carrier reference phase space is split into separate regions as shown in figure 3-4. Thereafter final evaluation of equation 3-1 is completed through some considerable Fourier analysis and algebra which can be found in [6]. Hence for three-level PD-PWM the coefficients are evaluated to:

$$C_{00} = 0 \quad C_{01} = MV_{DC} \quad C_{0n} = 0, n > 1$$

For $m > 0$, $n \neq 0$

$$C_{mn} = \frac{2V_{DC}}{m\pi}\{1 - \cos([n+m]\pi)\}\ \text{x}$$
$$\left[J_n(m\pi M)\sin n\frac{\pi}{2} + \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{J_{2k-1}(m\pi M)\ \text{x}\ [2k+1]cosn\frac{\pi}{2}}{[2k-1+n][2k-1-n]}\Big|_{|n|\neq 2k-1}\right] \tag{3-2}$$

Where $J_n(x)$ is a Bessel function of first kind with argument *x* and order *n*. For higher level PD-PWM controlled inverters full derivations of the coefficients of C_{mn} can be found in [6].

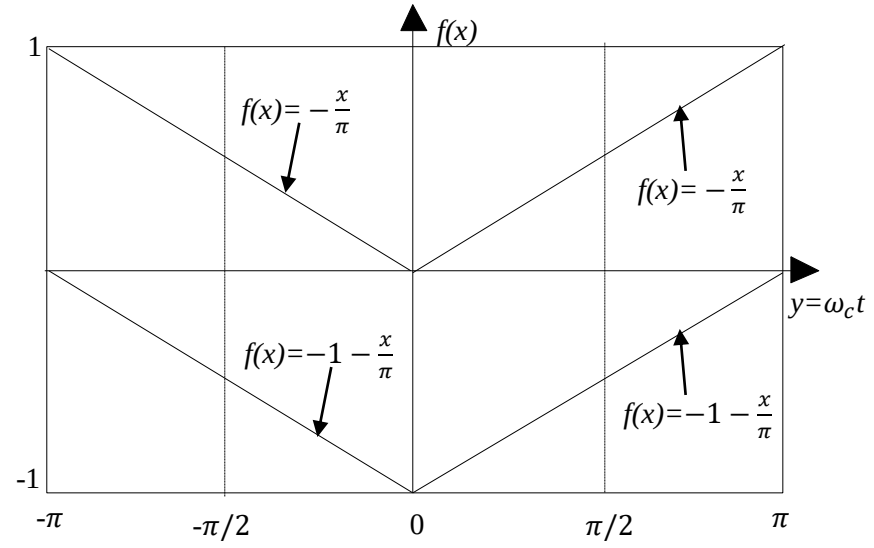


Figure 3-2: Three-level PD-PWM carrier waveform.

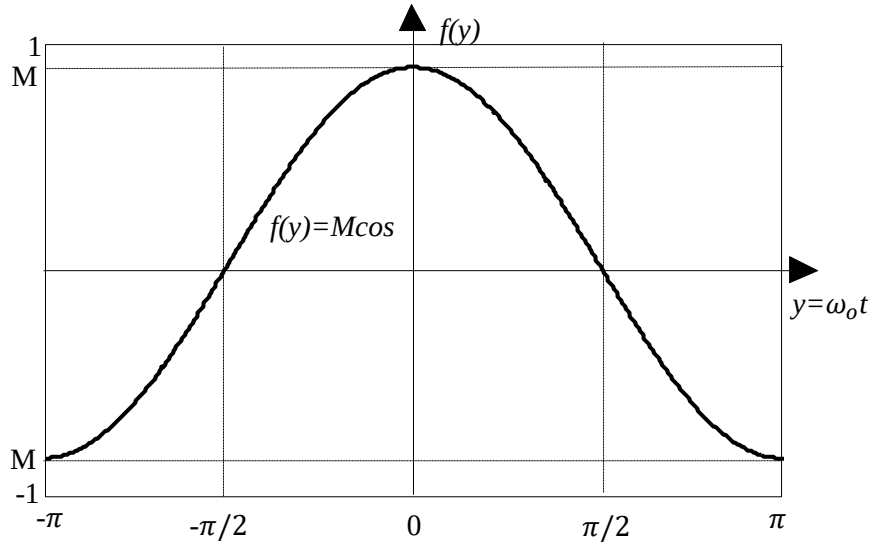


Figure 3-3: Cosine reference signal.

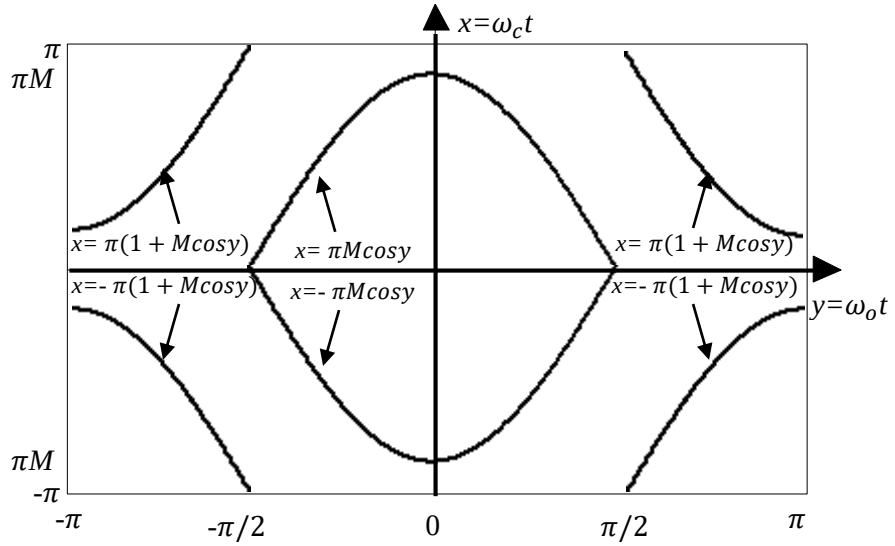


Figure 3-4: Three-level PD-PWM contour plot.

3.1.2 PS-PWM Fourier representation

Since the sideband and carrier coefficients for PS-PWM are not affected by the number of inverter levels the coefficients for any level inverter are simplified to:

$$C_{mn} = \frac{2}{m\pi}\sin\left([m+n]\frac{\pi}{2}\right)J_n\,(m\frac{\pi}{2}M) \tag{3-3}$$

Where m = 1, . . . ,∞; n = -∞, . . . ,-1, 0, 1, . . . , ∞.

3.1.3 CRPWM Fourier representation

For CRPWM the harmonic coefficient expression can be derived in a similar fashion to PD-PWM, the three-level inverter expression simplifies to:

$$C_{mn} = \frac{2}{\pi^2 m}[e^{-\frac{j[2n+m]\pi}{2}} - 1]\begin{bmatrix} (\pi/2 J_n\left(\frac{mM\pi}{2}\right)\sin\left(\frac{[m-n]\pi}{2}\right) \\ +\left\{\left(\frac{1}{n}\right)\sin\left(\frac{m\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)J_o\left(\frac{mM\pi}{2}\right)\right\}|_{n\neq 0} \\ +\sum_{h=1,h\neq|n|}^{\infty} J_h\left(\frac{mM\pi}{2}\right)\sin\left(\frac{[m-h]\pi}{2}\right)\left[\frac{\sin([n+h]\pi/2)}{n+h}+\frac{\sin([n-h]\pi/2)}{n-h}\right] \end{bmatrix} \tag{3-4}$$

3.1.4 Flying capacitor multilevel inverter output equations

The current passing into the *k*th flying capacitor can now be evaluated by applying Kirchhoff's current law to each phase leg of the inverter circuit, giving:

$$i_{q,C_k}(t) = [S_{q,k+1}(t) - S_{q,k}(t)]i_q(t) \tag{3-5}$$

The switched output voltage of each phase can be found by applying Kirchhoff's voltage law and summing adjacent two-level switching cells to give:

$$v_q(t) = \left[2S_{q,N}(t) - 1\right]\frac{V_{DC}}{2} - \sum_{k=1}^{N-2}[S_{q,k+1}(t) - S_{q,k}(t)]\,v_{q,k}(t) \tag{3-6}$$

3.2 Simulation models

The concepts are simulated in the technical computing environment of MATLAB; this provides a tool for analysing the effectiveness of control strategies for MLIs. MATLAB additionally has a Fourier analysis tool providing a method to effectively determine harmonics and THD of waveforms. The system block diagram is shown in figure 3-5, consisting of a DC supply, FCMLI, three-phase load and control block. The gate control signals are generated with a mathematical operational circuit as shown in figure 3-6.

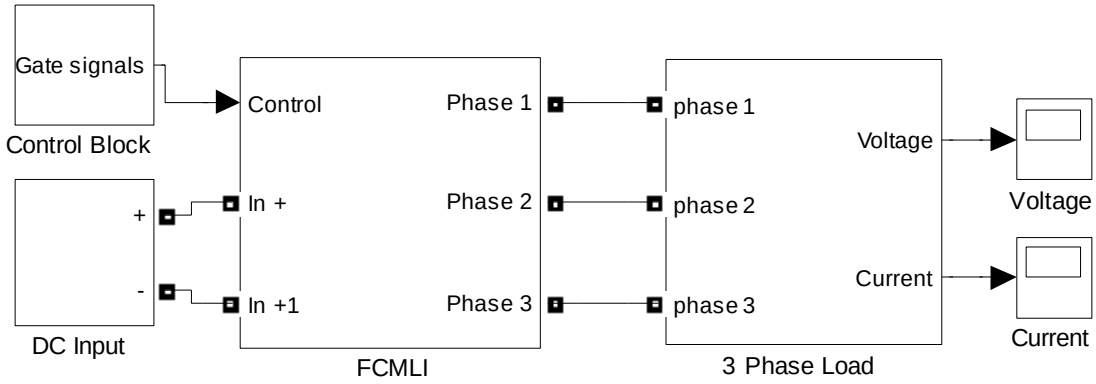


Figure 3-5: Simulink block diagram.

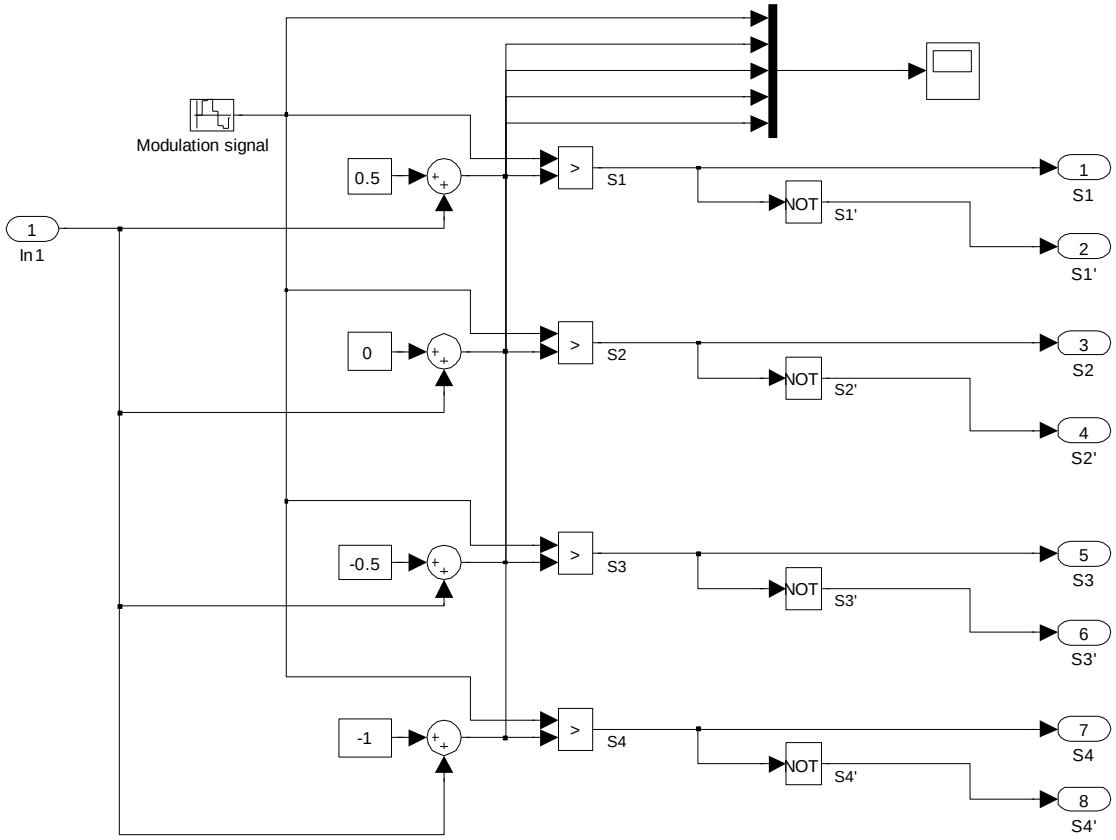


Figure 3-6: Control block diagram for PS-PWM.

3.2.1 Flying capacitor balancing performance

As discussed previously maintaining voltage balance of the FCs is an important aspect in ensuring acceptable operation of the inverter however due to non-idealities of real world applications voltage imbalance is likely to occur. Hence determining the effectiveness of a control strategy in terms of voltage balancing is one of the prime comparing characteristics. In order to induce a voltage imbalance in the simulation domain, which would not occur otherwise unless the control strategy is naturally unbalanced, a step change in the DC supply is generated.

This allows the control strategy to rebalance the FC voltages in accordance to the requirements of the voltage levels on the inverter. For example, if the DC supply of a three-level FCMLI is increased by 0.25, in order to maintain voltage balance the FC voltage of each phase must be increased by 0.125. The balancing perform is quantified by extracting the time taken for the FC voltage to reach 5% of its desired value which is standard for determining the settling time of a control system, figure 3-7 illustrates this example.

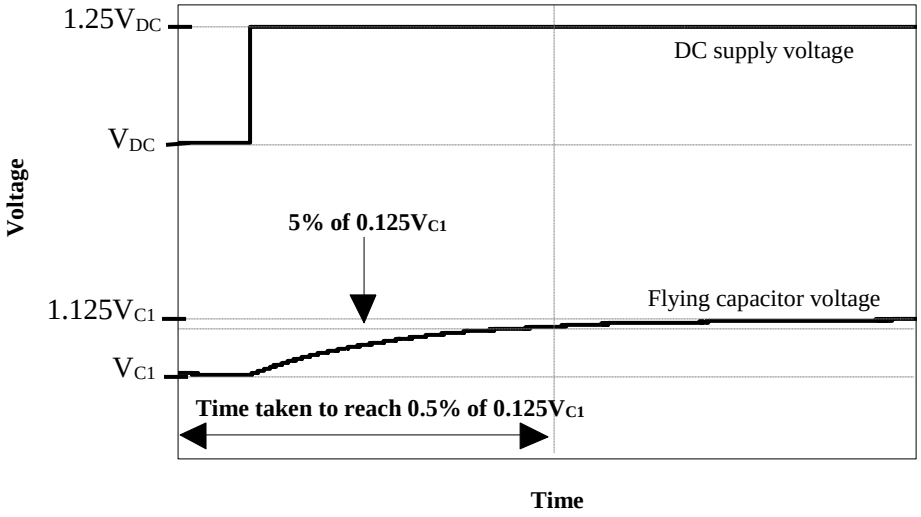


Figure 3-7: Quantifying balancing performance.

3.2.2 Switching frequency and harmonics

Due to the limitations that exist within switching devices it is important to consider the switching frequency of an inverter when comparing control strategies. The nature of PWM controlled inverters leads to fluctuating switching frequencies hence it is difficult to quantify this. It may be true to assume that the switching frequency of the individual cells at a given time will be close to the carrier frequency, particularly at modulation indices below 0.9, moreover for indices closer to 1 this statement may be untrue as carrier intersections at this modulation index can cause high frequency spikes. Regardless, depending on the control strategy the effective switching frequency of the switched output will differ significantly to the individual cell switching frequency. For example, the PS-PWM strategy places its carriers horizontally prompting greater intersections with the reference signal compared to PD-PWM, henceforth greater switching of the output will occur. Fourier analysis provides a tool for determining the effective switching frequency since harmonics are formed at the switching frequencies. Using the FFT analysis tool of MATLAB the waveforms can be simulated and the effective switching frequency determined by evaluating the observed harmonics.

In figure 3-8 the FFT analysis of the output waveform is shown for a five-level PS-PWM controlled FCMLI at a carrier frequency of 750 Hz. There are observed harmonic groupings at four times the carrier frequency, these are the sideband harmonics caused by the (N-1) carrier intersection. The 50 Hz grouping is caused by the baseband harmonics and as illustrated in figure 3-9 the carrier harmonics occur at multiples of 750 Hz. This is a good illustration of the greater effective switching frequency that can occur in MLIs.

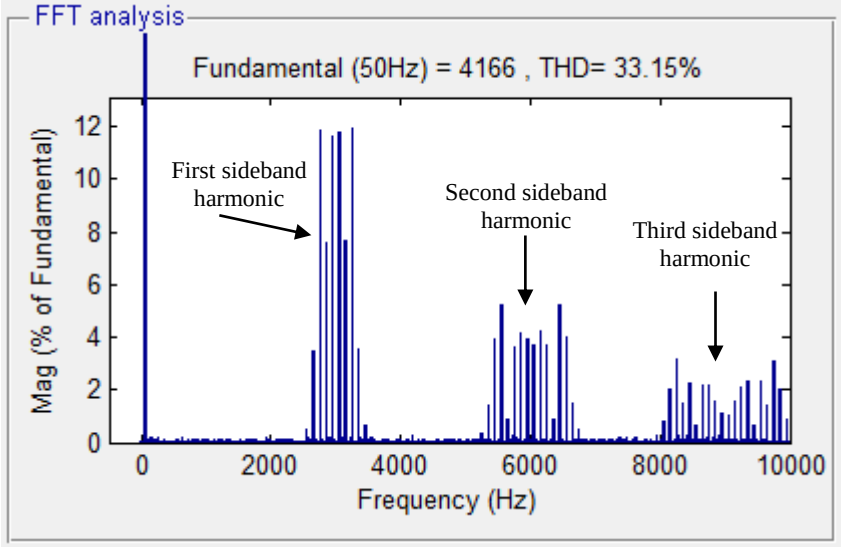


Figure 3-8: FFT analysis of output waveform for five-level PS-PWM f_o = 50 Hz, f_c = 750 Hz.

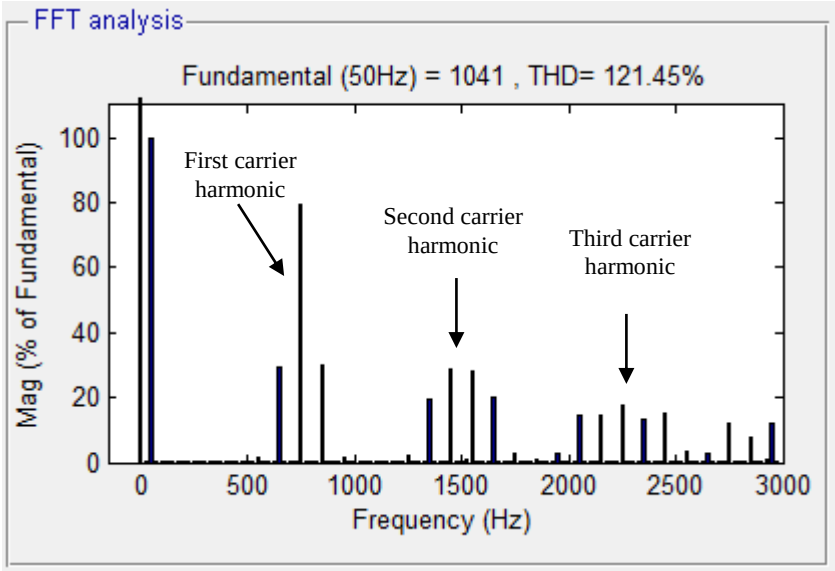


Figure 3-9: FFT analysis of individual cell waveform for five-level PS-PWM f_o = 50 Hz, f_c = 750 Hz.

By extracting the data of the FFT analysis for multiple simulations of varying load inductance a three dimensional plot of harmonic spectra's can be generated. These plots provide an important tool for identifying reductions in harmonics and comparing PWM control strategies. An example of this extraction is shown in figure 3-10.

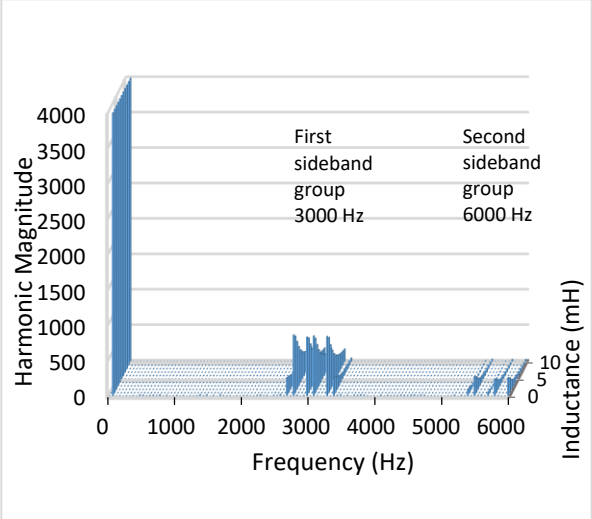


Figure 3-10: Harmonic spectra for varying load inductance five-level PS-PWM f_o = 50 Hz, f_c = 750 Hz

3.3 Conclusion

This chapter provides the necessary theory and background to understand the steps and techniques used to gather information for comparing FCMLI control strategies. Analytically modelling the control strategies is the first step undertaken; this allows analysis at a deep and theoretical level. Here, the foundation of the answer to the problem is formed. The technique for verifying these theories is continued through simulations which provide an avenue for calculating THD and quantifying the balancing performance.

Chapter 4. Study of PWM methods

4.1 Introduction

The purpose of this chapter is to dwell deeper into the present research of PWM methods for FCMLI control and the development of active control methods. The investigation focuses primarily on the two most industrially relevant techniques, namely PS-PWM and PD-PWM. Simulations are undertaken in MATLAB for the case of a medium-voltage, high-power range replicating the conditions associated with these types of inverters. For acceptable operation of FCMLIs the harmonic characteristics and FC voltage balance are especially important, hence these properties are closely observed. Furthermore an active control method is presented which aims at resolving the flaws of former developments.

4.2 System model

Generally the medium-voltage range is considered from 2.3 kV-6.6 kV and the high-power from 1 MW-50 MW [1] [2]. Hence a 6.6 kV output voltage was selected for this simulation with loads varying in the high-power range. The structure of a five-level FCMLI used throughout this chapter is shown in figure 4-1. The parameters of the inverter are listed in table 4-1 where the flying capacitance was determined using equation 2.1, a high capacitance is required to ensure a low voltage ripple, however this must be balanced with the increased the time constant of the FC voltage balancing [7].

$$\Delta V_c = \frac{I_{out,max}}{(N-1)f_{sw}C} \tag{4-1}$$

The frequency modulation index *mf*, and amplitude modulation index m_a, which are calculated using the equations below are taken as 15 and 0.9 respectively.

For PS-PWM:

$$m_f = \frac{f_{cr}}{f_m} \tag{4-2}$$

$$m_a = \frac{V_{ma}}{V_{cr}} \tag{4-3}$$

For PD-PWM:

$$m_f = \frac{f_{cr}}{f_m} \tag{4-4}$$

$$m_a = \frac{V_{ma}}{V_{cr}(N-1)} \tag{4-5}$$

Where f_m, and f_{cr}, V_{ma} and V_{cr} are the frequency and voltage amplitudes of the modulation and carrier signals respectively.

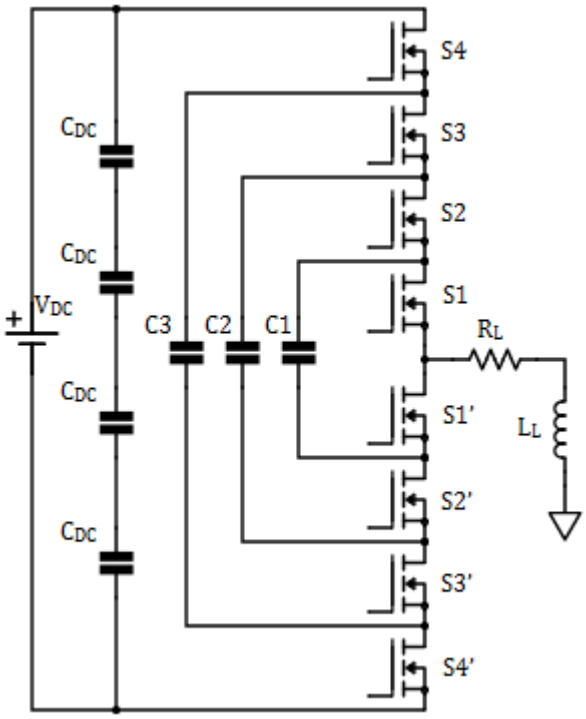


Figure 4-1: Single phase of a five-level FCMLI.

Table 4-1: Five-level inverter parameters

Circuit Parameter	Value
Voltage (V_{DC})	6.6 kV
Output voltage frequency (f_o)	50Hz
Flying capacitance (C_1-C_3)	3600 uF
DC link capacitance (C_{DC})	300 uF
Carrier frequency (f_{CR})	1.5 kHz
Load resistance (R_L)	43.56 Ω
Load inductance (L_L)	1 mH

4.3 Simulation results

Figures 4-2 (a)-(c) show the output waveforms for PS-PWM. The inductive component of the load acts as a filter smoothening the output voltage producing lower THD levels. This phenomenon can be seen in figures 4-2 (b) and (c), however produces a phase difference between the voltage and current causing a portion of the transferred power to be lost. Section 4.3.1 further investigates the need for a large load inductance to produce acceptable levels of harmonic distortion.

Using the same carrier frequency and frequency modulation index the individual switches contained in PD-PWM controlled system are switched comparative much less than PD-PWM as observed in figure 4-3 (a)-(c), this results in lower THD levels across the modulation index range as summarised in figure 4-4. Additionally it can be concluded that PD-PWM will result in lower switching losses but higher conduction losses of individual semiconductor switches.

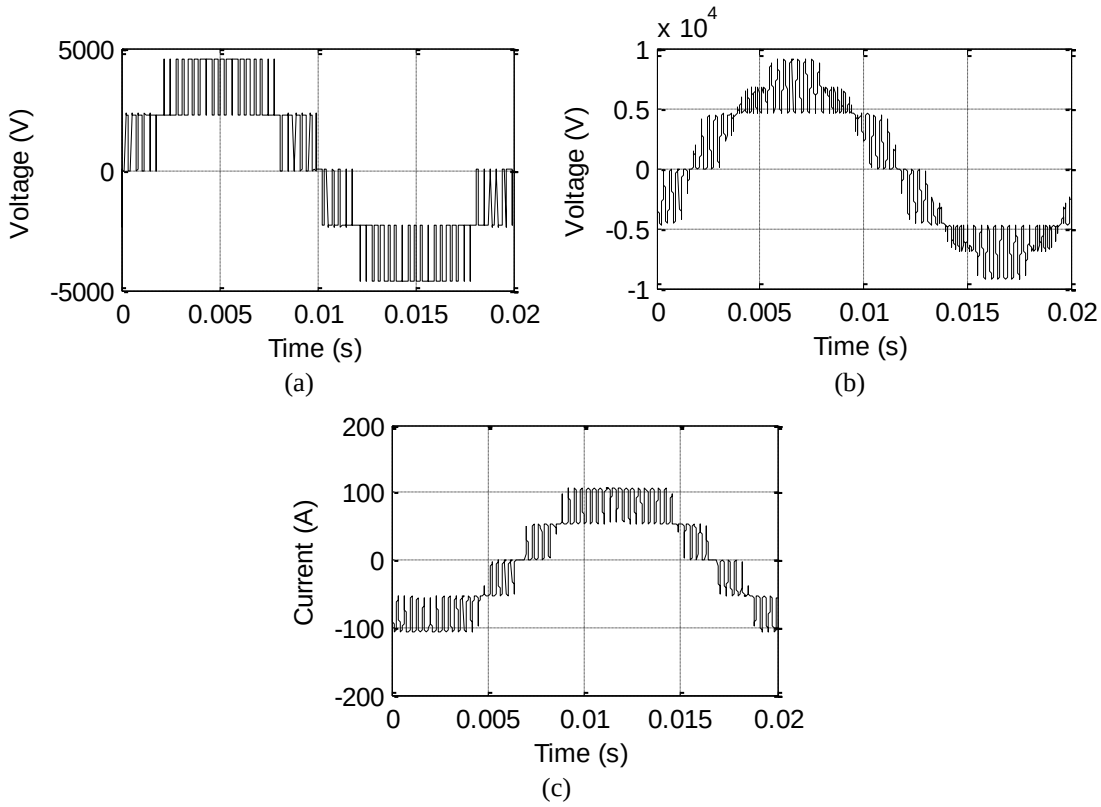


Figure 4-2: Five-level output waveforms (PS-PWM m_f = 15, m_a = 0.9) (a) Line voltage, (b) Phase voltage-after load inductance, (c) Phase current.

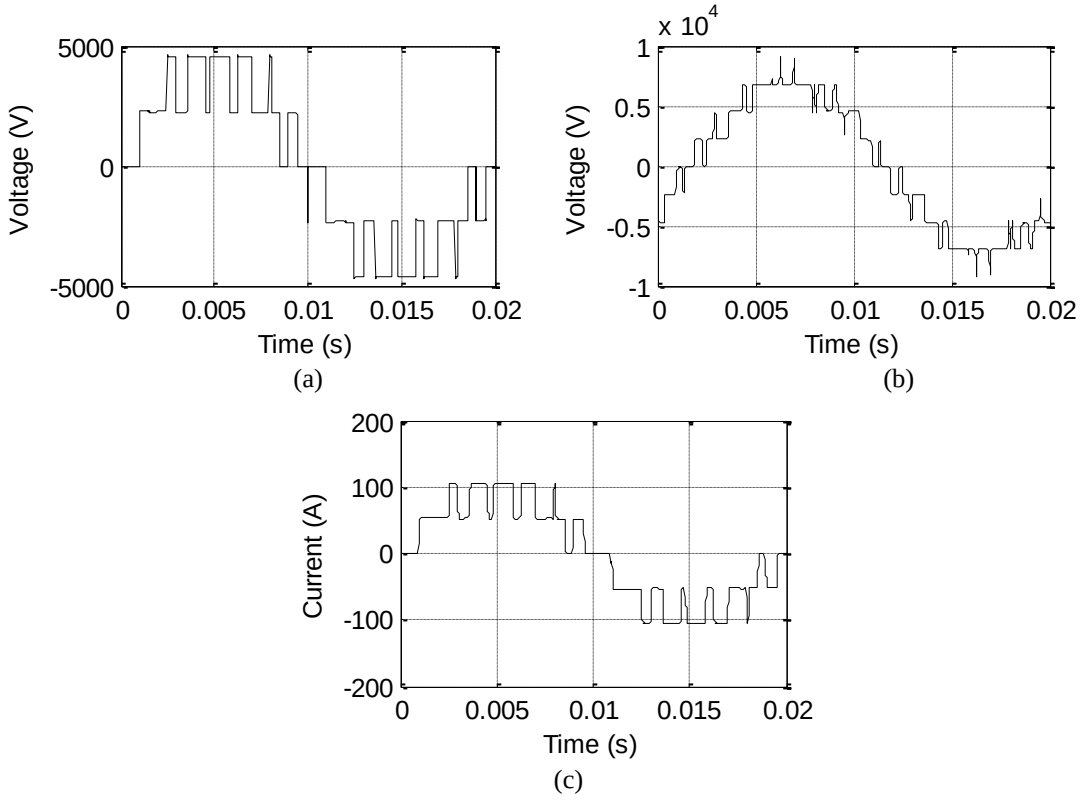


Figure 4-3: Five-level output waveforms (PD-PWM m_f = 15, m_a = 0.9) (a) Line voltage, (b) Phase voltage-after load inductance, (c) Phase current.

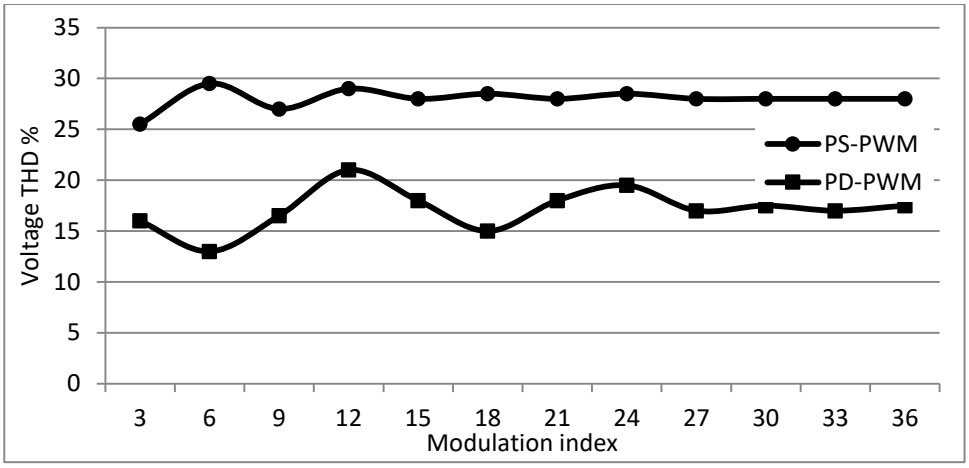


Figure 4-4: Comparison of voltage THD

4.3.1 Varying load inductance

The benefits of PS-PWM over PD-PWM with respect THD levels for varying load inductance of the current waveform are illustrated in figure 4-5. The IEEE standard 519-1992 "Recommended practices and requirements for harmonic control in electrical power systems" sets limits for the voltage and currents harmonic levels. For utilities the voltage and current limit is equal to 5%. For a five-level FCMLI to adhere to this practice it would require approximately an inductive load of 400 mH using the PD-PWM strategy, whereas only requiring approximately 10 mH for the PS-PWM strategy. Considering a 6.6 kV, 1 MWA inverter, the reactive power loss due to the required inductive load would be 24 kVar for the 10 mH and 64 kVar for the 400 mH load, an overall decrease in efficiency of 3.9% for PD-PWM. The increased cost of the larger inductance also adds to the downside of PD-PWM.

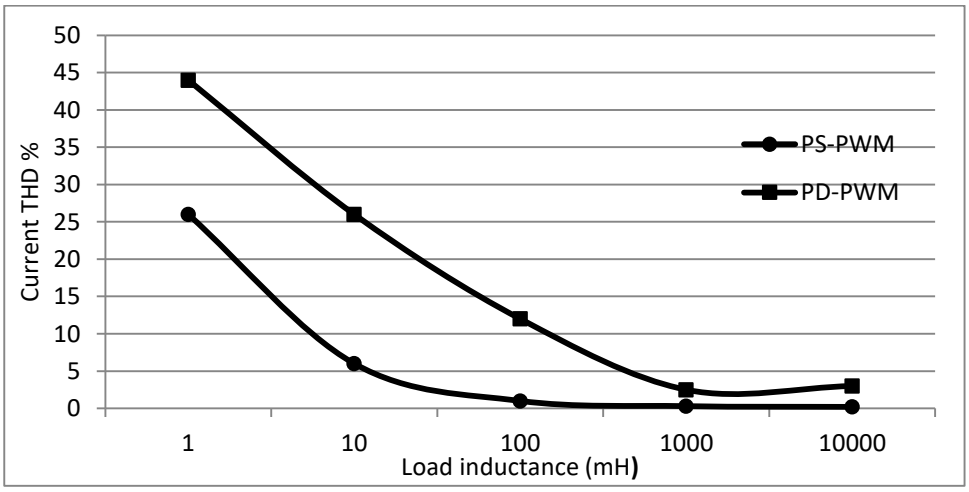


Figure 4-5: Comparison of current waveform distortion for varying inductance.

4.3.2 Varying load resistance

For this simulation the load resistance is reduced to replicate increased power rating, to ensure consistent results the power factor is maintained throughout, therefor the ratio of R_L/L_L is kept equal. Figure 4-6 illustrates a reduction in harmonic quality as the power rating increasees, this is much more apparent for PD-PWM and coincides with the earlier findings that load inductance heavily affects the THD levels at 10 mH for PD-PWM. The findings suggest that when reduced load inductance is the primary focus PS-PWM is far superior to PD-PWM.

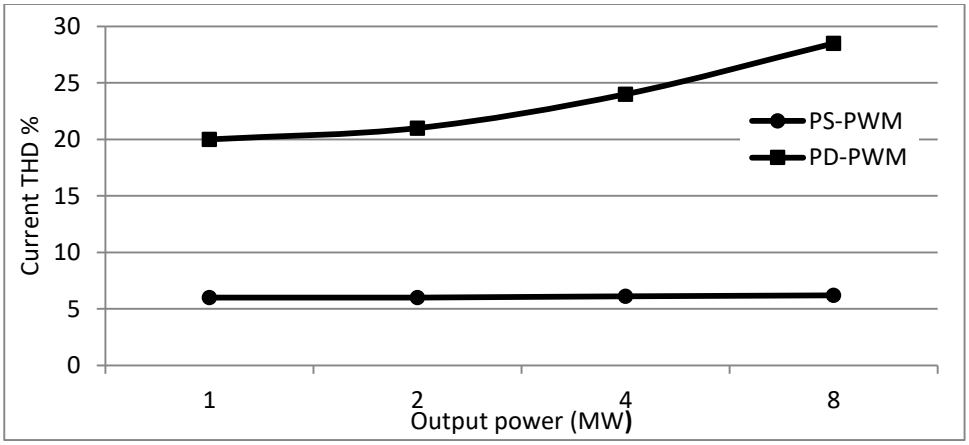


Figure 4-6: Influence of load resistance on harmonic content (L_L = 10 mH).

4.3.3 Comparison with three-level inverter

Figure 4-7 illustrates the improved performance of a five-level inverter over a three-level inverter; there is a substantial reduction in harmonic content for the five-level inverter. This is a well-known feature of MLIs and it has been shown in previous papers that further improvement of THD levels is observed with increased number of voltage levels [37]. The advantages of increased levels of the inverter can be summarised as follows:

- Reduced voltage and current THD.
- Reduced size of load inductance.
- Reduced voltage stresses on switching devices.
- Higher switching redundancy allows for flexibility in balancing control algorithms

The benefits of higher level inverters are however restrained by a number of factors summarized below:

- Increased number of flying capacitors and switching devices.
- Practical implemntations becomes complex.

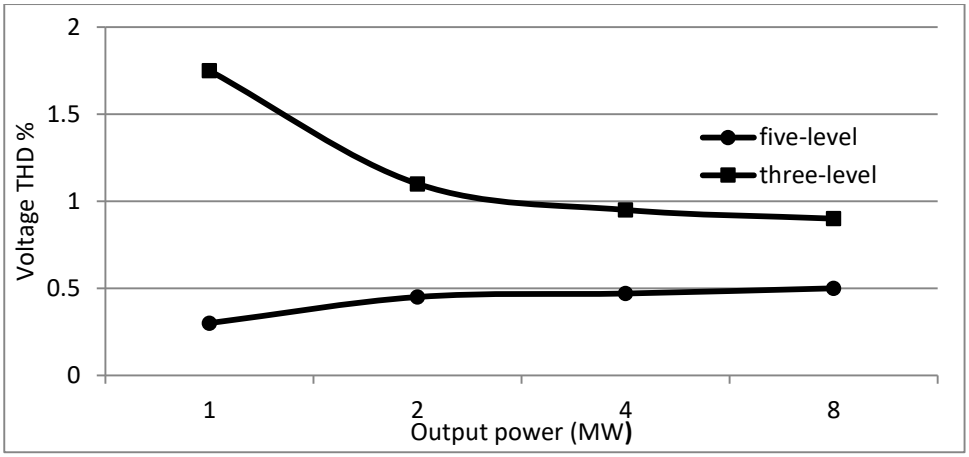
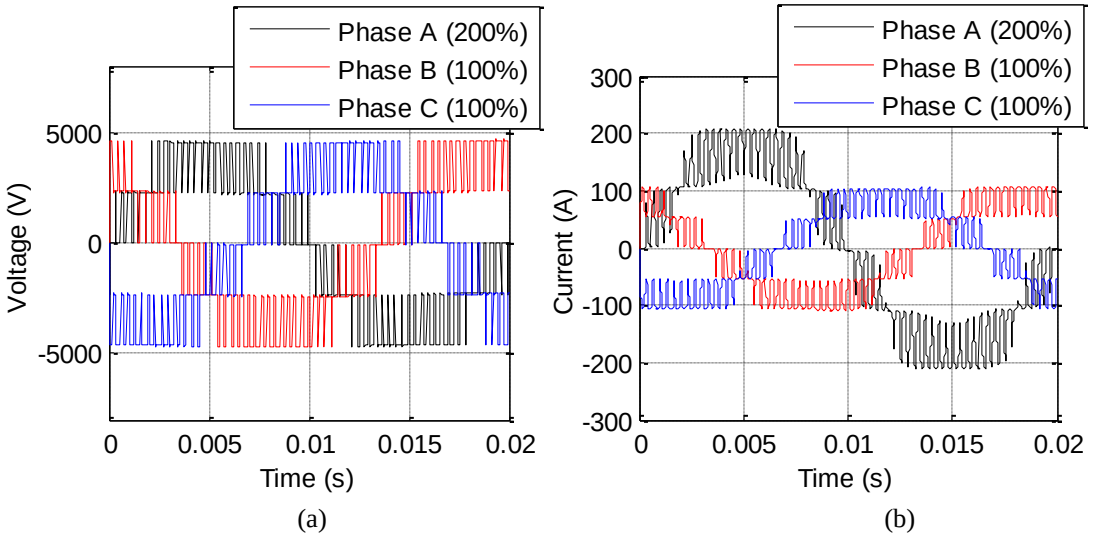
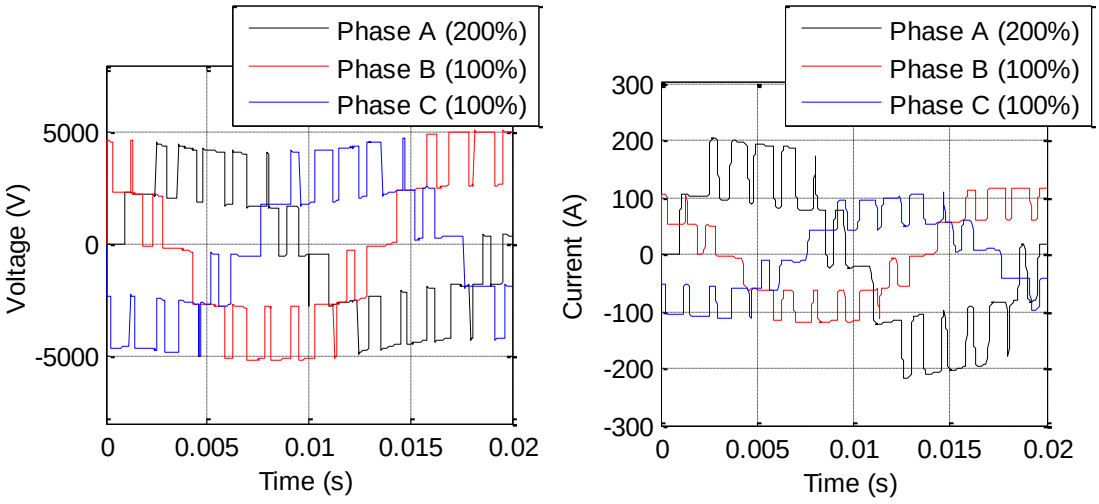


Figure 4-7: Comparison of harmonic content for five-level and three-level FCMLI (L_L = 100mH).

4.3.4 Unbalanced load

In real world applications it should be expected for the ac end of the inverter to be connected to unbalanced or nonlinear loads which can cause unexpected hindrances on the system. Therefore it is important to determine how each of the control strategies behaves under such conditions. This scenario was set up in simulation by means of an increased loading of 100% on a single phase of the inverter. Due to the stability of the PS-PWM strategy it is observed in figures 4-8 (a) and (b) that the three-phase waveforms remain unaffected by the unbalanced load, the load current is as expected increased on the unbalanced phases as the nature of power system dictates. Conversely PD-PWM exhibits a deterioration and fluctuation of the three-phase voltages and currents shown in figures 4-8 (c) and (d), a major repellent of this method as this puts strain on the connected device or utility. This is most likely the result of the unbalanced duty cycles of the PD-PWM strategy causing large fluctuation of the FC voltages. Finally since the harmonic magnitudes produced by the switching patterns are unaffected there was no apparent change in THD levels for both methods.





(c) (d)

Figure 4-8: Three-phase waveforms for unbalanced load conditions, (a) PS-PWM voltage, (b) PS-PWM current, (c) PD-PWM voltage, (d) PD-PWM current.

4.4 Natural flying capacitor balancing characteristics

As mentioned before an important aspect of PS-PWM is the natural balancing dynamics of the FC voltages which occurs in this technique, this in essence describes how the net current flowing in the capacitors over a switching period is zero and hence the floating voltage level remains constant [38]. The natural voltage balancing dynamic has been attributed to the losses causd by the current harmonics which is produced by the unbalanced capacitor voltages [39] [40] [41]. Authors in [21] describe how time-domain analysis of the FC voltages results in closed-form solutions to the time constants of the balancing dynamics. These equations show that balancing dynamics depend significantly on the inverter parameters, hence comparative results are a more appropriate tool. Figures 4-9 and 4-10 show the capacitor voltage balancing response of PS-PWM and PD-PWM respectively to a step change in DC supply voltage. The natural balancing dynamics of PS-PWM can be exhibited in figure 4-9, here the time constants of C_1 and C_3 are large and therefore the balancing takes extended time. In practical applications this slow balancing dynamic will be unable to overcome non-idealities of the system, such as power switching, voltage drops, deadtimes, finite rise and fall times, as well as nonlinearities. PD-PWM exhibits no voltage balancing dynamics as shown in figure 4-10, the constant change in flying capacitor voltage is a result of uneven charging and discharging pattern formed by the carriers of PD-PWM, hence this method requires some form of modification for FCMLI application.

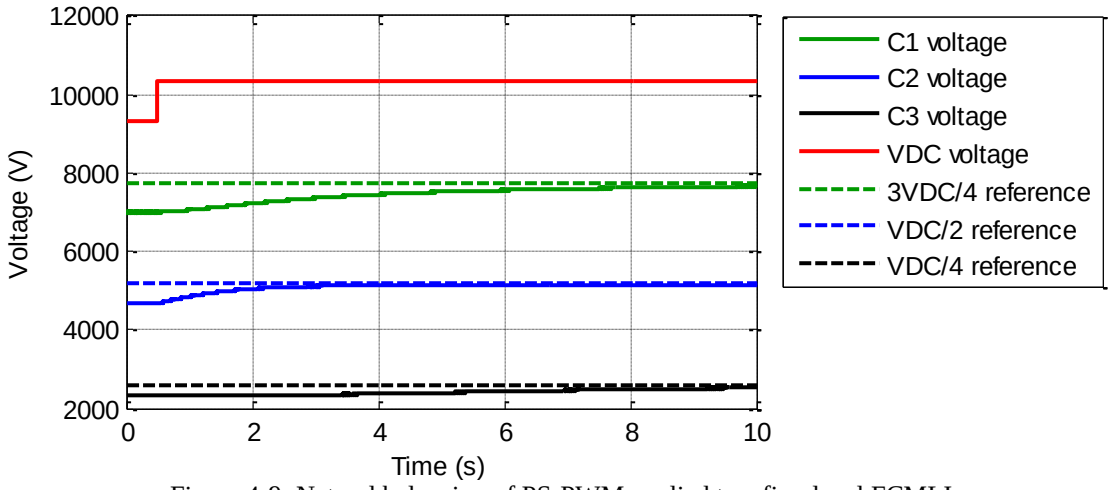


Figure 4-9: Natural balancing of PS-PWM applied to a five-level FCMLI

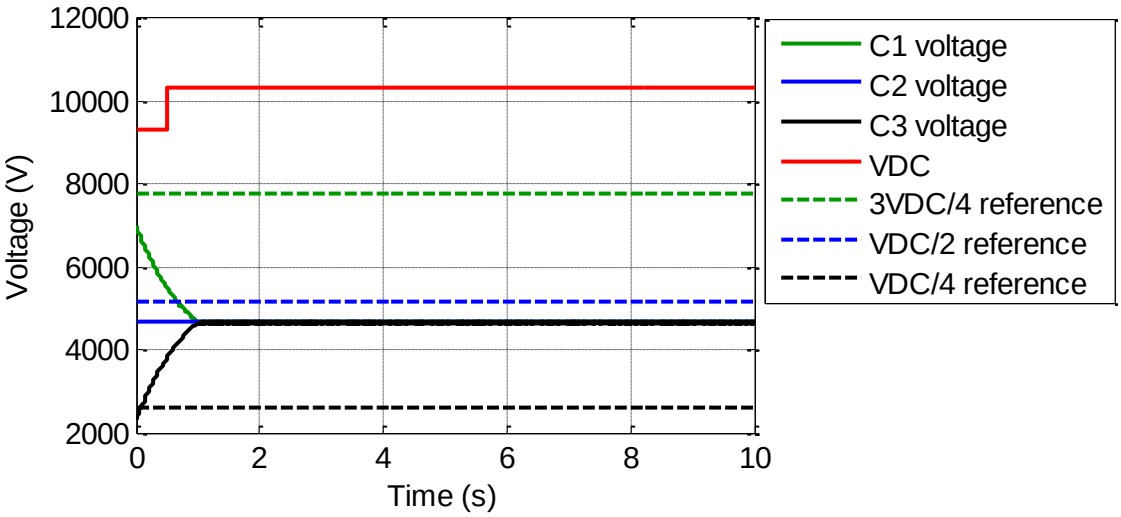


Figure 4-10: FC voltage collapse of PD-PWM applied to a five-level FCMLI

4.4.1 Natural balancing under fault conditions

To highlight some of the drawbacks of using open loop control, a five-level inverter using PS-PWM was simulated under fault conditions. After 0.1 seconds a short to ground was applied on a single phase of the inverter, the fault is removed after 0.5 seconds giving the system time to stabilize. Figure 4-11 illustrates the capacitor voltage rebalancing after the fault due to the balancing dynamics; again it is observed that the time constants are large due to the parameters of the inverter. Realistically these large time constants will make it difficult to implement this system in real world applications, hence methods such as modifying the PS-PWM switching pattern, active control algorithms which use feedback loops, optimal parameter selection or RLC balance boost circuits are required to improve the time constants to acceptable values.

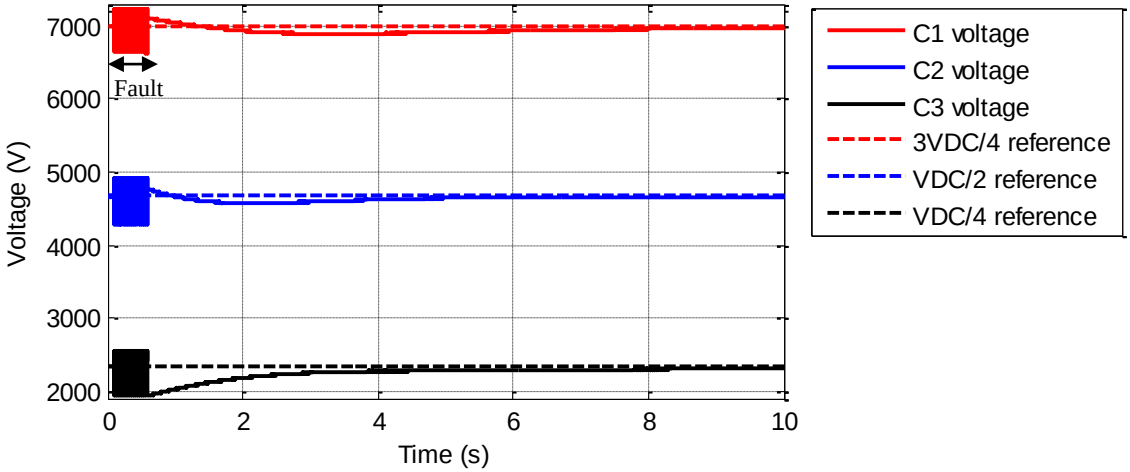


Figure 4-11: Voltage balancing after a fault.

4.5 Improved flying capacitor balancing with modified PS-PWM

A new method of active controlling FCs is proposed within this section which builds on theory of previous developments as discussed in the literature review. In this section a closed-loop modified PS-PWM control strategy focused primarily on restoring voltage balance is presented. The algorithm selects switching states bounded by times where no capacitor charging/discharging occurs to rebalance the FC voltages faster than the natural balancing of PS-PWM

The voltage control algorithm used is based on the proposed methods in [22] [23] [24], however it differs significantly in a number of ways. The algorithm in this section focuses on restoring voltage balance using PS-PWM with optimal settling time as the primary goal. Thereafter an investigation into harmonic injection is completed to determine the appropriateness of the strategy. This study is undertaken on the same five-level three-phase FCMLI summarized in table 4-1, however the techniques and findings can easily be applied to any level inverter. In order for the inverter to operate correctly the switching device voltage blocking stresses must be uniformly distributed at $V_{DC}/(N\text{-}1)$. Hence voltages V_{C1}, V_{C2} and V_{C3} must be maintained at $V_{DC}/4$, $2V_{DC}/4$, and $3V_{DC}/4$ respectively.

4.5.1 Algorithm fundamentals

The required switching states of the switches to obtain the desired voltage levels are shown in table 4-2; an attractive feature of the FC inverter is the flexibility in synthesising the output voltage. For a given voltage level, there are several switching states which will result in the same output waveform, but cause altered charging/discharging of the FCs.

Table 4-2: Switching states of five-level FCMLI.

V_o	Switching States				Charging/Discharging		
	S1	S2	S3	S4	C_1	C_2	C_3
V_{DC}	1	1	1	1	N	N	N
$V_{DC}/2$	1	1	1	0	+	N	N
	1	1	0	1	-	+	N
	1	0	1	1	N	-	+
	0	1	1	1	N	N	-
0	1	1	0	0	N	+	N
	1	0	1	0	+	-	+
	0	1	1	0	+	N	-
	1	0	0	1	-	N	+
	0	1	0	1	-	+	-
	0	0	1	1	N	-	N
$-V_{DC}/2$	1	0	0	0	N	N	+
	0	1	0	0	N	+	-
	0	0	1	0	+	-	N
	0	0	0	1	-	N	N
$-V_{DC}$	0	0	0	0	N	N	N

The core characteristic of the proposed algorithm is ensuring that when a FC voltage imbalance occurs the adjusted switching states only affects the imbalanced FC/s. This is achieved by the selecting adjustable switching states bounded by either the state 1111 or 0000 (periods where no charging/discharging of FCs occurs), in doing so this ensures that supplementary capacitor voltages remain unaffected by the injected pulse.

The voltage control block diagram is shown in figure 4-12, measurements of the actual capacitor voltages V_{C1}, V_{C2} and V_{C3} are compared with the reference values V_{C1}*, V_{C1}* and V_{C1}*. This forms the error signals which control the size of the pulses injected into the switching pattern to restore the voltage balance.

The balancing control algorithm can be summarised as follows:

Step 1: Selecting switching states bounded by the states 1111 or 0000 to compensate for the capacitor voltage imbalance.

Step 2: Scaling error signal dictated by switching frequency and voltage rating, and limiting the maximum change in switching period.

Step 3: Adjusting the switching period of the selected switching states.

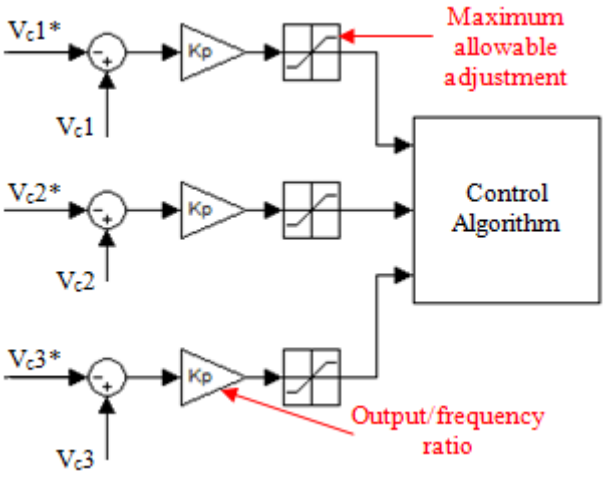


Figure 4-12: Voltage control block diagram.

4.5.2 Selecting switching states

Referring back to table 4-2, assuming for example, V_{C1} is below its reference signal and the only capacitor imbalanced, it is required to either increase the charging time or decrease the discharging time of capacitor C_1 without affecting V_{C2} and V_{C3}. The natural response is to increase the on time of the state 1110, in doing so the states within the pattern of the chosen PWM method next to the selected state will be decreased which may off balance a different capacitor voltage. The simplest solution is to ensure that the selected state 1110 is next to the states 1111 or 0000 since no capacitor charging/discharging occurs here, as in figure 4-13.

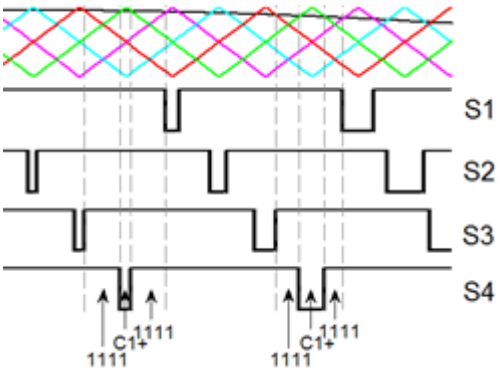


Figure 4-13: Switching state 1110 occurring next to 1111 within PS-PWM, $m_f = 15$, $m_a = 0.9$.

For the case of an imbalance in C_3 the same logical steps can be applied as mentioned before, except utilising the switching state 0111. For an imbalance in C_2, following the algorithm, the states 1100 and 0011 are required next to 1111 or 0000, however an inspection of figure 4-13 will show that this does not occur in the portion of a switching cycle where the state 1111 occurs and will not occur on the opposite half cycle since it is mirrored. Hence in order to increase the charging time of C_2 and adhere to the algorithm the period of 1101 and 1110 are

increased by the same amount. The increased period of the state 1101 will increase the charging times of C_2 but has the undesirable effect of increasing the discharging time of C_1, however this is compensated by the increased switching time of the state 1110 which will increase the charging time of C_1 leaving V_{C1} unaffected and only the voltage of V_{C2} is increased. A similar logic can be applied if V_{C2} is above the reference signal. The adjustable states and size of the adjustable areas in accordance to the algorithm for a five-level FCMLI inverter are shown in figure 4-14.

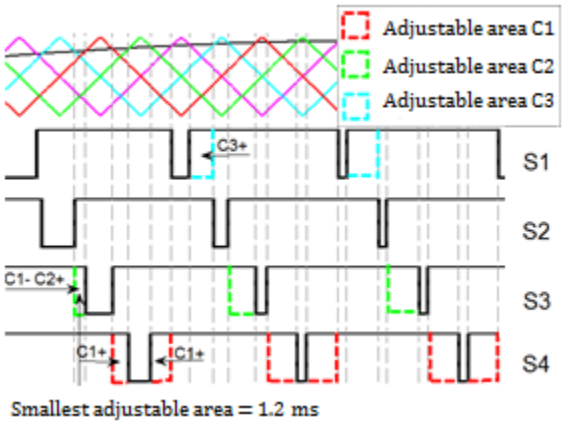


Figure 4-14: Selection of switching states and allowable adjustment areas, m_f = 15, m_a = 0.9.

4.5.3 Scaling error signal

The magnitude of the error signal in the given model may be in the kV range, whereas the switching period is in the ms range, hence the error signal requires some scaling which will be denoted as k_P, the output voltage switching frequency ratio. Decreasing the value of k_P to a small fraction is expected to reduce the resolution of the control loop i.e. increase the steady state error but has the desired effect of reducing the settling time of the system. Simulation trials found taking $k_P = V_{DC}/f_{CR}$ produced satisfactory results.

4.5.4 Maximum allowable adjustment

The maximum change in switching period is determined by the allowable adjustment areas as shown in figure 4-15. Although it is not the most optimal, for simplicity, and to ensure the system reaches a balanced state the maximum change is taken as the smallest adjustment area of the chosen states. For the selected switching states, modulation index and frequency modulation index it was found that the smallest allowable adjustment area was 1.2 ms, hence this is the maximum change in switching period.

4.5.5 Adjustment of switching states

Adjustment of the switching periods is accomplished through the injection of pulses. The pulse width is determined by the error signal and the pulse time by the selection of switching states, figure 4-15 shows an example of an injected pulse. Implementation is achieved through simple logical circuitry.

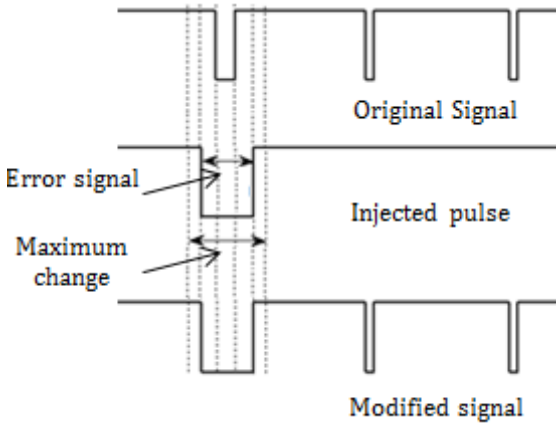


Figure 4-15: Adjustment of switching period.

4.6 Conclusion

The comparison of PS-PWM and PD-PWM driven by simulations on a five-level FCMLI has shown that PS-PWM has superior natural balancing mechanics and produces lower THD levels when reducing load inductance is the main focus. The simulations highlight the large natural balancing time constants which may not be feasible for real world applications hence an active control algorithm for PS-PWM has been proposed which will be investigated further in chapter 5.

Chapter 5. Voltage control and performance evaluation

5.1 Introduction

This chapter will investigate the viability of the active control algorithm proposed in chapter 4, hence comparing its performance to the currently considered optimal strategy of CRPWM. Also determining whether the addition of RLC balance boost circuits outweigh the benefits of conventional control strategies. Subsequently an analytical comparison of PS-PWM and PD-PWM is undertaken to identify the roots of the balancing characteristics. Finally a deeper understanding of the performance of FCMLI control strategies is provided by the evaluation of current ripple calculations.

5.2 Five-level FCMLI with voltage control

The capabilities of the two PWM strategies in terms of balancing dynamics of a FCMLI inverter can now be explored through simulative studies. The effectiveness of the control algorithm is verified through a step change in DC supply causing an imbalance in the FC voltages. The results are based on the balancing response of a five-level inverter with parameters given in table 4-1 and structure in figure 4-1, operating under both modified PS-PWM and CRPWM.

The simulated capacitor voltage response of C_1 for a 25% increase in DC supply is shown in figure 5-1, with the full set of settling times for the simulations undertaken given in table 5-1. The modified PS-PWM and CRPWM strategies can be seen to respond significantly faster to the change in DC supply compared to the natural response of PS-PWM. The overall decrease in settling times suggests that for this specific case the proposed modified PS-PWM strategy can outperform the CRPWM strategy.

Confirming previous research concepts, figure 5-2 shows CRPWM with substantially lower THD % levels than PS-PWM for purely resistive loads. However when the load inductance is considered as shown in figure 5-3, at the same carrier frequency and load inductance PS-PWM heavily out performs CRPWM.

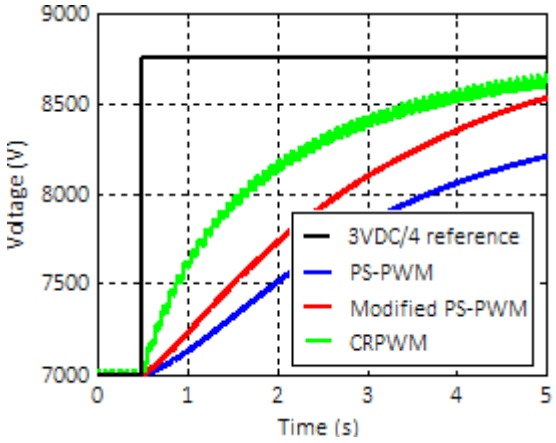


Figure 5-1: Response to step change in voltage of C_3.

Table 5-1: Summary of settling times.

Parameter	Settling time (s) - time taken to settle within 5% of final value		
	PS-PWM	Modified PS-PWM	CR-PWM
C_1	14.2	6.25	5.5
C_2	8.5	2.75	6.2
C_3	17	5.55	7.5
Average	13.23	4.85	6.4
% decrease	-	63.34 %	51.62 %

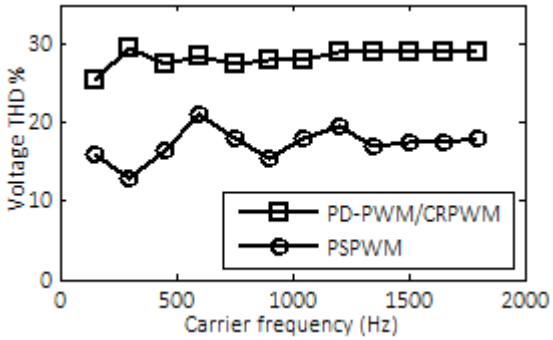


Figure 5-2: Purely resistive THD performance.

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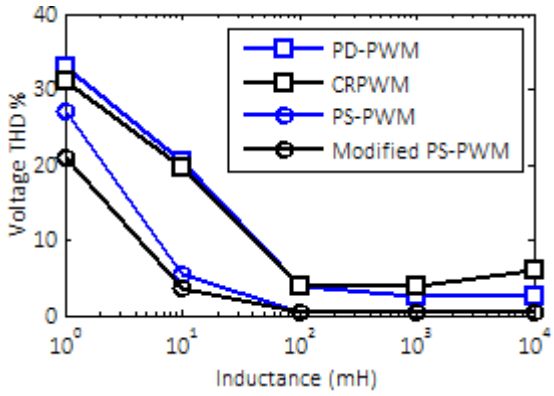
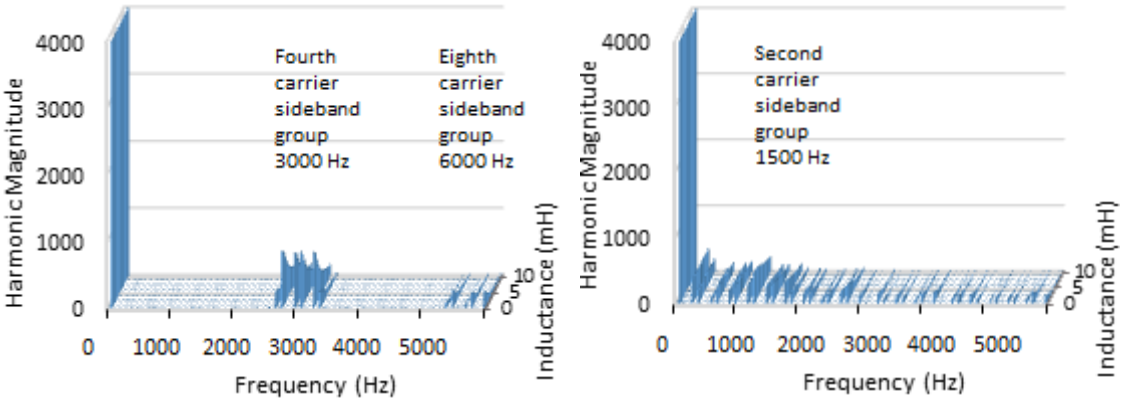


Figure 5-3: Harmonic performance of proposed method

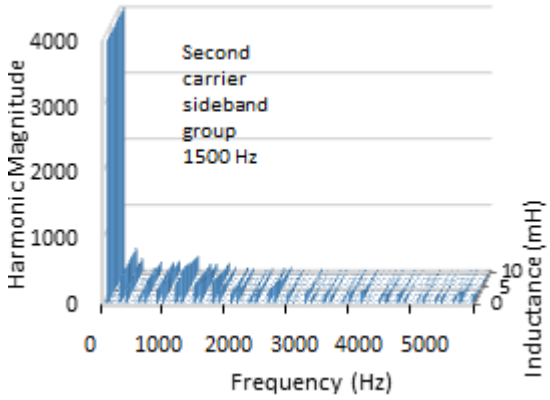
5.3 Comparative analysis of PS-PWM and PD-PWM

It is known that the cause of FCMLI's natural balancing properties is from nonzero harmonic currents flowing in the FCs. Equation 3-5 identifies that the current flowing in a FC is determined by the difference between adjacent cell switching functions multiplied by the phase leg output current. It has been proven analytically [20] that only the differences between high-frequency carrier and sideband switching harmonic components will cause nonzero currents to flow in the FCs. The load connection also plays a role in the balancing mechanics; the simulations conducted assume a neutral connection on the load if this were not the case, only differential output voltage harmonics between phase legs would produce the high-frequency harmonics required for voltage balancing [20].

With these concepts in mind a comparison of harmonic performance and balancing dynamics of PD-PWM, PS-PWM and CRPWM can be channelled. From chapter 4 it was concluded that PS-PWM had superior harmonic performance when minimising load inductance was the main criteria, whereas PD-PWM had superior harmonic performance for purely resistive loads. This is further confirmed in plots of output harmonic spectra as a function of load inductance as shown in figure 5-4. The high THD levels of PS-PWM are almost completely attributed to the $(N\text{-}1)^{th}$ carrier sideband groups which are heavily reduced with increased inductance. Whereas the distortion of PD-PWM is produced from the first carrier sideband harmonics and a spread of small harmonic magnitudes across the spectra, which remain large, even at higher inductance values as shown in figure 5-4 (b). It is important to note that the results shown in figure 5-4 (b) and (c) represent how the harmonic performance of PD-PWM and CRPWM are essentially identical; this has already been proven by time-based switching simulations.



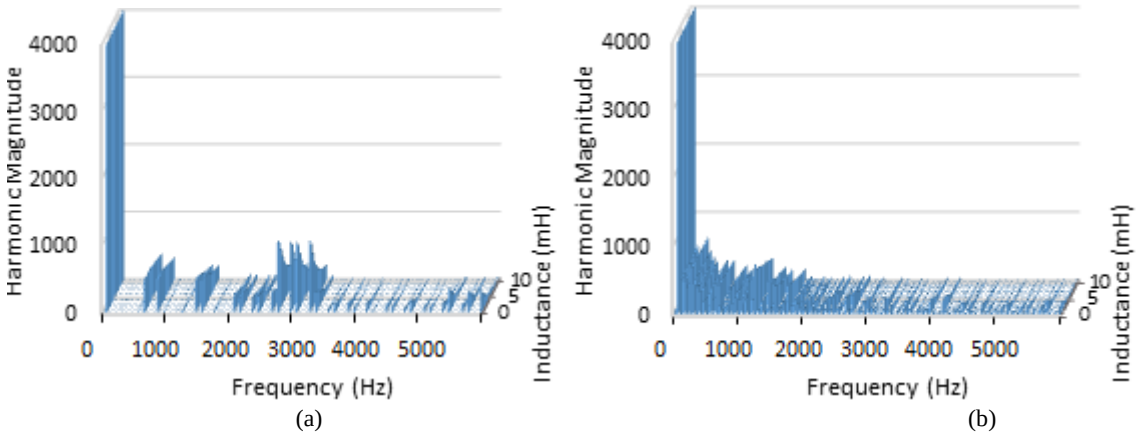
(a) (b)



(c)

Figure 5-4: Switching function harmonic spectra as a function of load inductance, m_a = 0.9, (a) PS-PWM, (b) PD-PWM, (c) CRPWM.

The harmonic spectra for unbalanced condition, shown in figure 5-5 identify the crucial aspect of the two strategies balancing performance. When the FC voltages are unbalanced large high frequency harmonic currents will flow through the FCs which will naturally rebalance the voltages. For CRPWM a heavy increase of high frequency harmonic currents especially focused around the first carrier sideband frequency appear, these will cause a strong natural rebalancing of the capacitor voltages. However for PS-PWM this increase in high frequency harmonics is not as profound. These findings identify that CRPWM will have superior natural balancing mechanics compared to PS-PWM, which is confirmed in the simulation results comparing the balancing response for a step change in DC voltage of 25%. However controlling the FC voltages through the proposed strategy it is shown that the PS-PWM method can achieve similar if not better results than CRPWM.



(a) (b)

Figure 5-5: Switching function harmonic spectra for unbalanced FC voltage, m_a = 0.9, (a) PS-PWM, (b) CRPWM/PD-PWM,

The confirmation of the high frequency carrier sideband groups in the analysis can effectively explain the improvements observed in balancing dynamics with the addition of balance booster filters in FCMLI. These filters are usually tuned around the first carrier sideband group harmonic frequency according to equation (5-2). This will produce a small impedance across

the load at the tuned frequency, sinking increased harmonic currents when the capacitor voltage imbalance occurs and strengthening the balancing dynamics. With the presence of the large second carrier sideband harmonics found in PS-PWM it should be possible to tune the filter around this frequency [20], this is in part confirmed in the example simulation shown in figure 5-6.

$$\sqrt{L_b C_b} = \frac{1}{2\pi f_{sw}} \tag{5-2}$$

Where L_b and C_b are the series connected inductance and capacitance of the filter per phase.

With the addition of the balance boost filter it is clear this method will produce significantly improved balancing responses, both PS-PWM and CPWM have approximately equal decreases in settling time around 88%. This example is however too arbitrary to facilitate any hard conclusions, however it does highlight a number of important aspects. Firstly, the balancing dynamic of FC inverters is chaotic and difficult to explicitly determine. There is an immense amount of factors at play which makes fine tuning the balancing properties in an ideal world complex, and in the real world unmanageable.

Secondly there are specific benefits for each method signifying that no method is concretely superior but rather there are circumstances where one method may be more beneficial than another. For instance, the addition of a balance boost circuit in the above example significantly improves settling times but the added circuit components are costly, while the modified PS-PWM method has inferior settling times but the cost of this method (voltage sensors) would be significantly less. If PS-PWM can achieve similar settling times to CRPWM, as the experiments suggest and achieve lower THD levels at the same load inductance and switching frequency as shown in figure 5-3, it would suggest that in-fact PS-PWM may be the superior PWM strategy for this case which is in contrast to previous research findings.

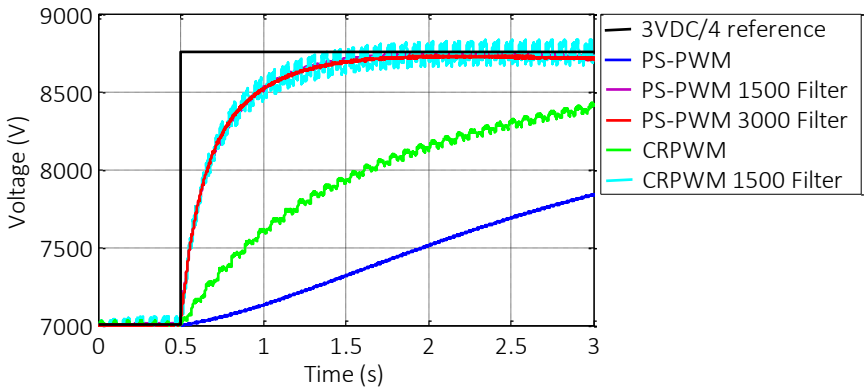


Figure 5-6: Response to step change in voltage of C_1 with balance boost filter.

Table 5-2: Summary of settling times with balance boost filter

Parameter	Settling time (s) - time taken to settle within 5% of final value				
	PS-PWM	PS-PWM 1500- Hz tuned filter	PS- PWM 3000- Hz tuned filter	CRPWM	CRPWM 1500- Hz tuned filter
C_1	14.2	1.32	1.32	5.5	1.32
C_2	8.5	1.4	1.62	6.2	1.4
C_3	17	1.48	1.66	7.5	1.7
Average	13.23	1.4	1.53	6.4	1.47
% decrease	-	89.41 %	88.44 %	51.63 %	88.89

5.4 Self-precharge applications

A useful application of the improved voltage balancing is in the self –precharging of the FCs [21] [42]. During the self-precharging process the DC supply voltage is increased at a slow steady rate to reduce the voltage stresses on the switches. The voltage stresses of the respective switching pairs are equal to the difference between the consecutive FCs. By ensuring that the FC voltages all increase at a similar rate through the application of the proposed methods, the overall stresses can be reduced.

The improvement the modified PS-PWM method has on self-precharge is exemplified in figure 5-7. In this example the capacitors are precharged to its desired voltage relatively instantaneously as the voltage increases, whereas the unmodified method lags behind. The lagging effect will cause additional stresses on the switching devices, creating unnecessary need for higher rated specifications of the inverter. The modified PS-PWM method provides a more robust and reliable self-precharge process.

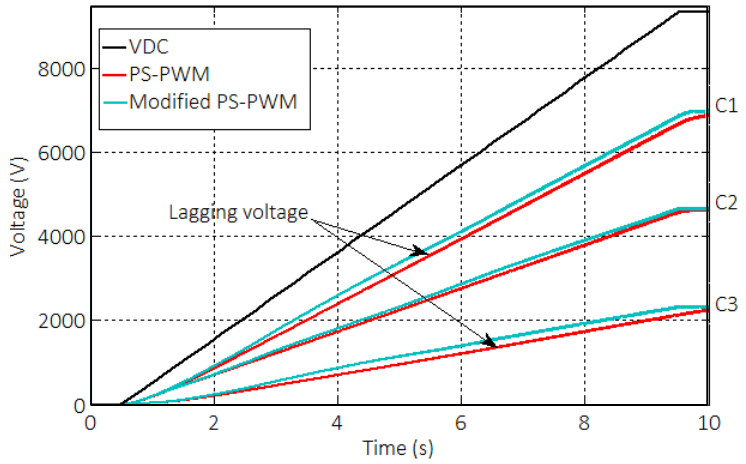
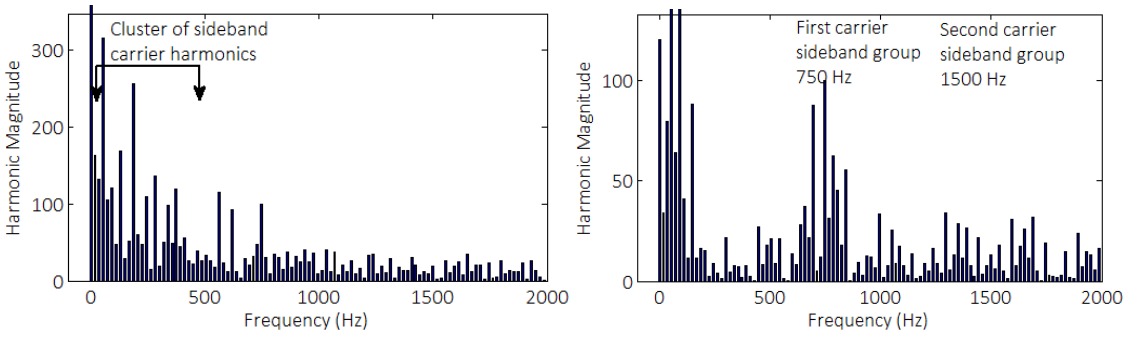


Figure 5.7: Self-precharge example (C_{DC} equal to 360 uF)

5.5 Effective switching frequency

It is of particular importance to determine the effective switching frequencies of the modulation methods of interest as one major limitation is the capabilities of present day semiconductor technology [1]. The limitations appear due to the finite time a switching device takes to be turned “on” or “off” which becomes increasing large as the power rating of the device goes up.

CRPWM and PD-PWM may have essentially identical output harmonic spectra’s as mentioned before which is expected on the bases of CRPWM being derived from PD-PWM, however carrier signals are reallocating more evenly within CRPWM which suggests that the effective switching frequency of individual cells will be lower. Figure 5-8 shows the individual cell switching harmonics magnitudes for the two methods, and as expected for PD-PWM the first carrier sideband group lies around the carrier frequency (750 Hz region), this is the frequency where majority of the switching of the semiconductor device will occur. Now considering CRPWM, the majority of switching occurs at a lower cluster frequency of approximately 250 Hz, with this finding in mind it is appropriate to assume that the carrier frequency of CRPWM can be at least tripled before reaching similar effective cell switching frequencies of PD-PWM



(a) (b)

Figure 5-8: Individual cell switching spectra f_c = 750 Hz. (a) CRPWM. (b) PD-PWM

5.6 Analysis of ripple current in PWM methods

The need to consider the degree to which undesirable harmonics exist is usually the basis for performance indicators such as THD, however I_{PP} also provides a respectable indicator of waveform distortion [28] [34]. It is useful to derive closed-form solutions to I_{PP} and consequential losses, in order to form a basis of comparison between different modulation techniques.

5.6.1 Simplified calculation

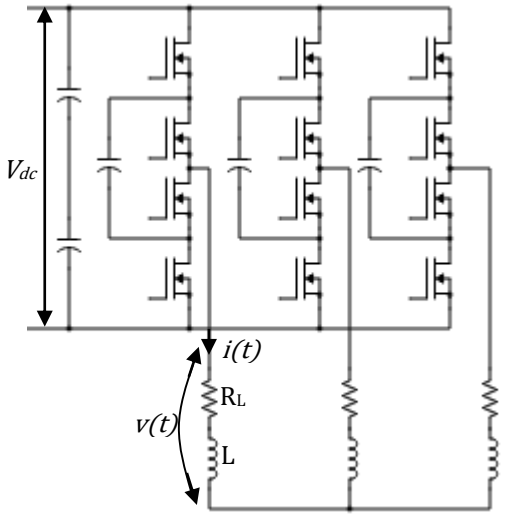


Figure 5-9: FC Inverter with RL load

The circuit schematic of a three-level FCMLI connected to an RL load is shown in figure 5-9 ,the voltage equation per phase is given as [28]:

$$v(t) = Ri(t) + L\frac{di}{dt} \tag{5.3}$$

In order to determine these closed formed solutions it is useful to simplify the calculation by assuming that the switching times of the inverter remain constant, in essence supposing that the modulation signal is constant, in this way the output voltage is a constant switching square wave. It is also not unreasonable to assume that the average voltage produced at the load over an arbitrary switching interval t_p is constant. Now considering the load is subjected to a swicthed voltage according to figure 5-10, the expected current waveform is shown.

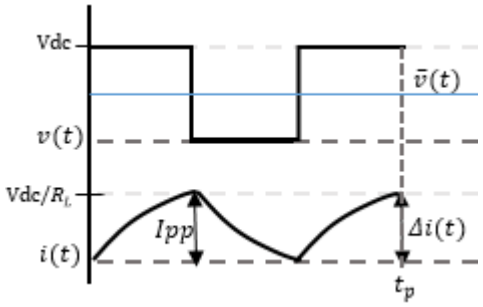


Figure 5-10: Load waveforms

The instantaneous voltage ripple $\tilde{v}_t$ is defined as the difference between the instantaneous voltage and average voltage which can be written as [28]:

$$\tilde{v}(t) = v(t) - \bar{v}(t_p)$$

$$\tilde{v}(t) = Ri(t) + L\frac{di}{dt} - R\bar{\imath}(t_p) + L\frac{\Delta i}{t_p}$$

$$\tilde{v}(t) = R[i(t) - \bar{\imath}(t_p)] + L[\frac{di}{dt} - \frac{\Delta i}{t_p}] \tag{5.4}$$

Where $\bar{v}(t_p)$ and $\bar{\imath}(t_p)$ are the average voltage and current across the period t_p respectively. Assuming that the resistive voltage drop of the current ripple will be small, equation 5-4 can be solved to give the current ripple over a period from (0, t):

$$\Delta i(t) \cong \frac{1}{L}\left[\int_0^t \tilde{v}(t)dt + \frac{\Delta i}{t_p}t\right] \tag{5.5}$$

Hence the instantaneous current ripple becomes [28]:

$$\tilde{\imath}(t) = \Delta i(t) - \frac{\Delta i}{t_p}t \cong \frac{1}{L}\int_0^t \tilde{v}(t)dt \cong \frac{1}{L}\int_0^t \left(v(t) - \bar{v}(t_p)\right)dt \tag{5.6}$$

Assuming the effective switching frequency for a *N*-level PS-PWM controlled inverter is (*N*-1) times greater than that of PD-PWM, an assumption which is not unreasonable since PS-PWM has (*N*-1) more carriers, and applying equation 5-6 to a constant switching square-wave, an estimation of I_{PP} for the two methods can be seen in figure 5-11. This provides a clear explanation of the improved harmonic performance of PS-PWM over PD-PWM with respect to load inductance, due to the greater effective switching frequency of PS-PWM the current will have less variation from the desired sinusoidal wave as depicted in figures 5-12, hence require a smaller load inductance to smoothen the waveform. This also identifies why PD-PWM produces superior THD levels at purely resistive loads. As the inductance of the load approaches zero the current ripple of the two methods become equal and it is the greater amount of switching within PS-PWM which constitutes the increased distortion of the waveform rather than the magnitude of the harmonics.

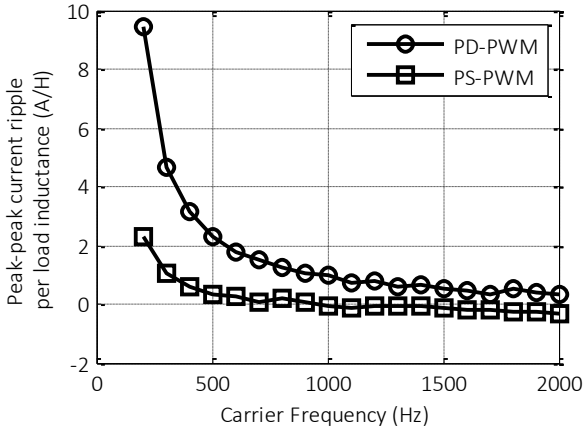


Figure 5-11 I_{PP} proportional to load inductance, comparison of PS-PWM and PD-PWM (five-level)

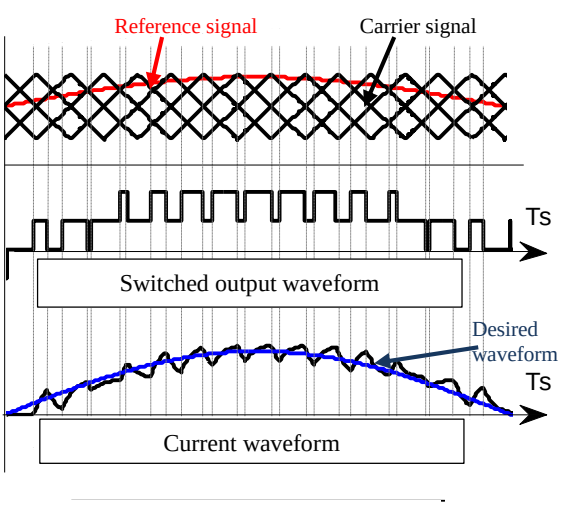


Figure 5-12: Switching waveform PS-PWM f_c = 750 Hz

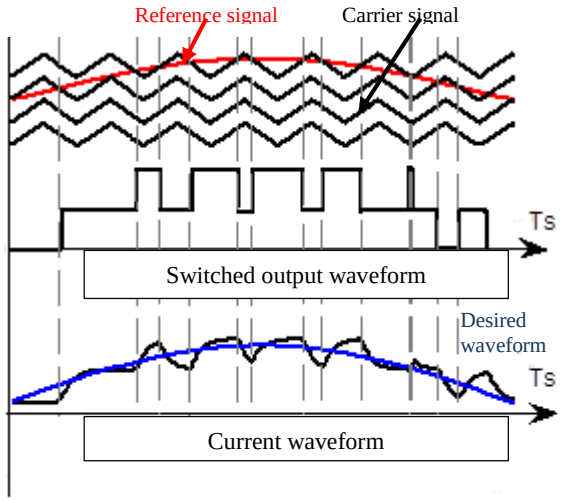


Figure 5-13: Switching waveform PD-PWM f_c = 750 Hz

5.6.2 Current ripple calculation by means of switching functions

To obtain the full closed form solutions the non-constant switching times of the inverter which are dictated by the carrier waveforms of the respective modulation method are required, these were derived in chapter 3 and given by equation 3.1. The individual cell switching functions of a multilevel inverter can be described by a double Fourier harmonic series and the switched output voltage of each phase can be found by applying Kirchhoff's voltage law to sum the contributions of the adjacent two-level switching cells to give equation 3.6. Now, substituting equation 3.6 into equation 5.6 where the average voltage $\bar{v}(t_p)$ is the modulation signal $Mcos(wt)$, hence we obtain the fully described instantaneous current ripple for an N-level inverter given by:

$$\tilde{\imath}(t) \cong \frac{1}{L}\int_0^T \left(\left[2S_{q,N-1}(t) - 1\right]\frac{V_{dc}}{2} - \sum_{k=1}^{N-2}[S_{q,k+1}(t) - S_{q,k}(t)]v_{q,k(t)} - Mcos(wt) \right) dt \quad (5.7)$$

It is apparent that further simplification of equation 5-7 will be complex and it becomes beneficial to solve it using a computer program with step increments in time to obtain the desired plots. For example applying equation 5-7 over one cycle of the modulation signal with calculations of current done at step time increments the output current waveform can be produced as shown in figure 5-14. As expected, this method closely resembles that of the simulated waveform, using MATLAB, under the same conditions.

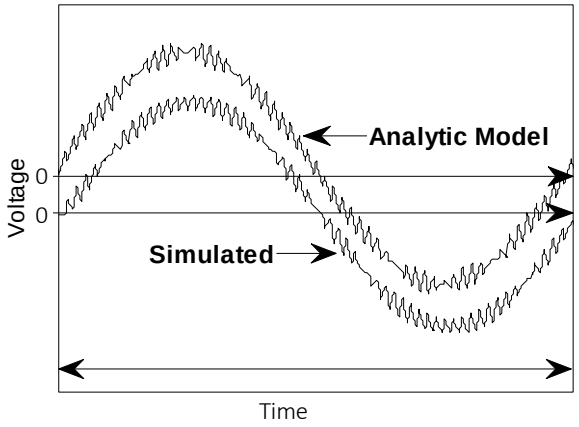


Figure 5-14: Comparison of analytic model and simulated model for PS-PWM.

5.6.2.1 Accurate ripple calculation

The process of calculations done at step time increments is applied for all equations containing the individual cell switching functions. Solving equation 5-7 against load inductance as shown in figure 5-15, it is proven analytically that PS-PWM will produce substantially less peak-peak current ripples over PD-PWM. Due to the observed trend there appears to be a (*N*-1) correlation when comparing PS-PWM and PD-PWM for inductor requirements, this phenomenon is attributed to the (*N*-1) increased output switching frequency of PS-PWM as mentioned before. Hence multiplying the values of PS-PWM by (*N*-1) this correlation can be more clearly illustrated. This can be mathematically shown as:

$$I_{pp,PSPWM} = \frac{1}{(N-1)} I_{pp,PDPWM} \tag{5-8}$$

The same reciprocal graph shape is seen in figure 5-16 for peak-peak current vs frequency, emphasising equation 5-8.

It is of course expected that a higher carrier frequency will produce smaller current ripples however current high power semiconductor technology draw a limitation on this aspect since the switching frequency of these devices can only go so high. This clarifies the benefits of PS-PWM, higher level inverters will see further reduction in peak-peak current, consequently minimising inductive filter requirements and lowering switching device limitations.

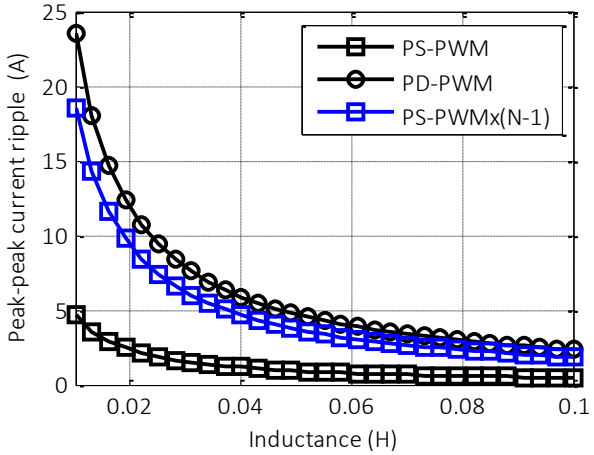


Figure 5-15: I_{pp} vs Inductance (five-level).

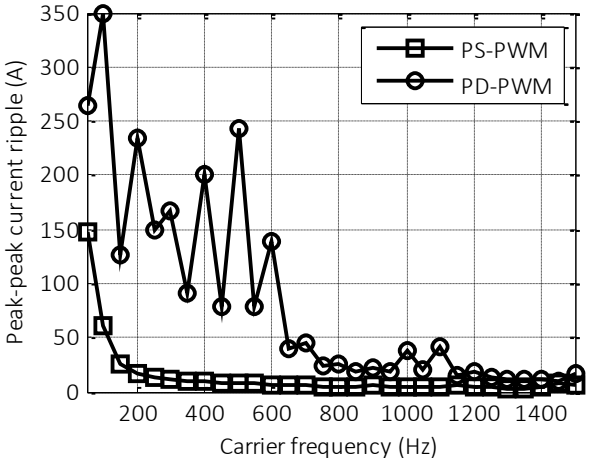


Figure 5-16: I_{pp} vs Carrier frequency (five-level).

5.6.2.2 Harmonic power loss

To determine the accumulative effect that the peak-peak current has on in terms of efficiency the harmonic power loss is considered. This is proportional to equivalent load resistance times the square of the DC equivalent of the peak-peak current ripple ($I_{pp,rms}$) [6].

$$I_{pp,rms} = \sqrt{\frac{1}{T}\int_0^T \Delta i(t)^2 dt)}$$

$$= \sqrt{\frac{1}{T}\int_0^T \left(\frac{1}{L}\int_0^T (v(t) - \bar{v}(t_p))dt\right)^2 dt)}$$

$$= \sqrt{\frac{1}{TL^2}\int_0^T \left\{\int_0^T \left([2S_{q,N-1}(t) - 1]\frac{V_{dc}}{2} - \Sigma_{k=1}^{N-2}[S_{q,k+1}(t) - S_{q,k}(t)]v_{q,k(t)} - Mcos(wt)\right)dt\right\}^2 dt)} \quad (5.9)$$

$$P_{h,cu} = R_e {I_{pp,rms}}^2 \quad (5.10)$$

Considering the plot of harmonic power loss shown in figure 5-17 the percentage power loss for a 1 MW five-level inverter at a load inductance of 0.01 H is 0.0094% for PS-PWM and 0.24% for PD-PWM. Multiplying the PS-PWM data points by $(N-1)^2$ to obtain the reciprocal shape again it is shown that equation 5-8 holds some truth between the relationship between PS-PWM and PD-PWM. Under the same process the three-level analytical model presents an almost identical graph shape shown in figure 5-18.

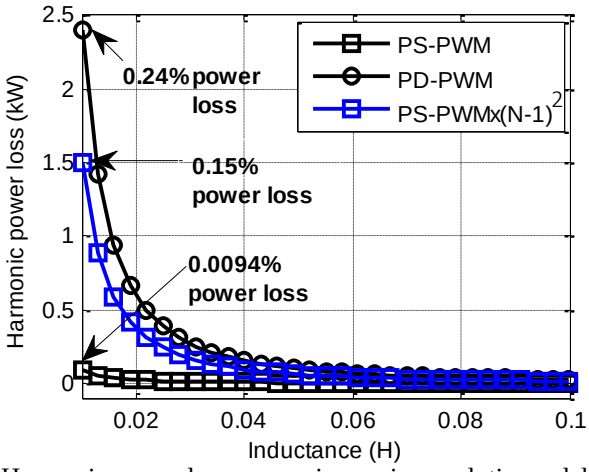


Figure 5-17: Harmonic power loss comparison using analytic model (five-level).

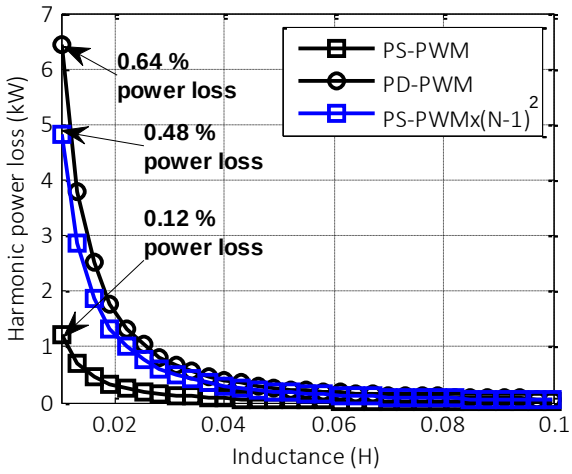


Figure 5-18: Harmonic power loss comparison using analytic model (three-level).

5.6.2.3 Evaluation of carrier redistribution pulsewidth modulation

The Fourier representation of CRPWM is completed using the previously discussed methods with a full derivation of the coefficients of equation 3-1 given in [20]. Applying equation 5-7 to the CRPWM strategy the peak-peak current ripple is illustrated in figure 5-19. It is clear that this heavily improves the PD-PWM strategy in this regard. Furthermore applying equation 5-10 to the strategy as shown in figure 5-20 the same improvements to harmonic power loss are shown. It is apparent from these results that the CRPWM strategy works effectively at

distributing switching states in FCMLIs hence reinforcing the practice of CRPWM for this topology.

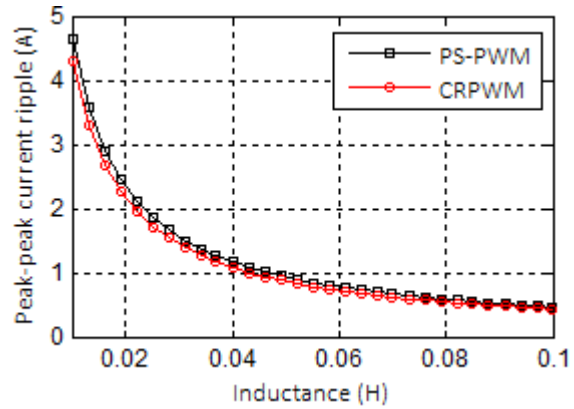


Figure 5-19: I_{pp} vs Inductance (CRPWM, five-level).

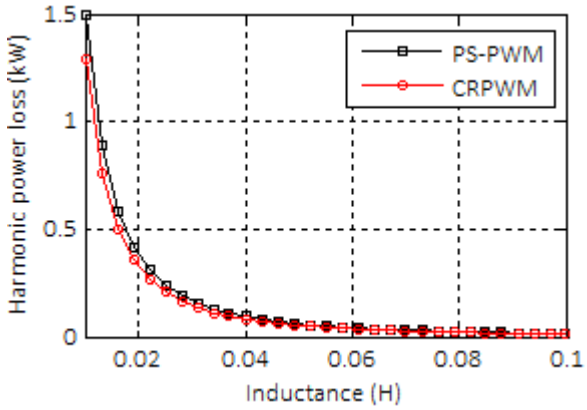


Figure 5-20: Harmonic power loss comparison using analytic model (CRPWM five-level).

5.7 Conclusion

The critical question, which carrier-PWM methodology intended for FCMLI's is superior, does not have a simple answer. If the aim is reduced filter requirements then the answer is PS-PWM, especially when one considers the limitation on switching devices. Furthermore, the IEEE standard 519-1992 which sets a limit for the voltage and current harmonic level at 5% for utilities ties a tenfold increase in load inductor requirement to the PD-PWM strategy as shown in figure 5-3. This increase equates to an approximate decrease in efficiency of 4% for the given system. Alternatively, if the aim is improved balancing mechanics without the complexity of active controls or additional filters then the answer is PD-PWM. Ultimately when comparing PD-PWM and PS-PWM taking effective switching frequencies, carrier redistribution of PD-PWM and external balance boost filters into account the two methods will produce approximately equivalent results.

Chapter 6. Conclusion and Recommendations

6.1 Conclusion

This research work ultimately aimed at refining the fundamentals of FCMLI control strategies, ergo shedding some light on the inconsistencies that present day literature contains and providing improved solutions. The preferred method of synthesising the sinusoidal output waveform is through decoded PD-PWM/CRPWM, where carriers are place one atop the other, and switching states are reallocated to distribute duty cycles and balance switching losses. This method generates the lowest level of harmonic distortion in the switched output waveform; however the preliminary research findings of this study suggested there may be some intrinsic benefits to using the PS-PWM strategy, where carriers are placed one besides the other, in reducing filter requirements.

On the bases of the increased effective switching frequency of PS-PWM the hypothesis that this strategy has reduced load inductance requirements over PD-PWM was formed. Using well-known methods for calculating current ripple in two-level inverters [28] combined with the works of McGrath and Holmes [20] for analytical models of representing FCMLIs, it was proven that the PD and PS modulation strategies had approximately a (N-1) and (N-1)^2 reciprocal relationship for current ripple and switching losses respectively. The reduced current ripple is the attributing factor in the improved harmonic performance of PS-PWM, for the reason that at the same carrier frequency the method requires a smaller load inductance to smoothen the waveform. Since there is a limitation on the maximum switching frequency of a switching device, the PD strategy cannot indefinitely increase its carrier frequency to match the performance of the PS strategy. The principles and findings can easily be adapted to the alternative MLI topologies and furthermore do not conflict with the previous notion that PD-PWM has superior harmonic performance, but rather identified conditions where it may be beneficial to select the unmodified PS strategy over the unmodified PD strategy.

FC balancing mechanics is the second crucial aspect which this research work set out to improve. A new modified PS-PWM control algorithm was presented and the effectiveness of the strategy compared to the previously believed superior method of CRPWM, was shown to be noteworthy. The critical question, which carrier-PWM methodology intended for FCMLIs is superior, was shown to have a complex answer. The CRPWM strategy, which is specific to FCMLIs, is an effective solution to the drawbacks of PD-PWM, producing similar if not

identical harmonic performance to that of PS-PWM. Hence there is no exclusively superior method but rather there are circumstances where one method may be more beneficial than another. If PS-PWM can achieve similar balancing mechanics to CRPWM, which the simulations demonstrated, with a 63.34% decreased settling time in the FC voltage when a disturbance occurred at the input for PS-PWM and 51.62 % for CRPWM, and achieve identical THD levels at the same load inductance and switching frequency, it would suggest that PS-PWM may be a viable strategy for FCMLI control. However if the aim is improved balancing mechanics without the complexity of active controls or additional filters, then the previous research findings holds true and PD-PWM is the answer.

Finally it was shown that sinking load currents at the carrier frequency proofs to be an effective strategy at reducing settling times, demonstrated by the use of a balance boost filter, which provided an 88% improved settling time in the simulations conducted. If the additional costs of these filters can be ignored and minimal settling time is the main criterial then this is the optimal of the considered strategies.

6.2 Recommendations

Traditionally the problem of balancing the FC voltages is the greatest restriction of FCMLIs, in order to develop robust systems where this topology will see more industrial applications active control strategies such as the new proposed algorithm within this research work are an attractive solution over natural balancing.

6.3 Scope for future work

There is still much research required in this field, the findings of this work are not enough to validate a switch in the preferred control strategy of CRPWM. The work holds its ground only in a theoretical and simulative world; the findings need to be confirmed through experimental studies. This would require construction of a FCMLI controlled by each of the methods discussed in this thesis and thorough experiments conducted to confirm the proposed strategy can perform as the simulations suggest.

Analytical models of the CHB and the NPC inverter topologies should also be developed with the same principles of current ripple calculation applied in order to develop the little information in the field of multilevel current ripple modelling. Doing so will provide researchers additional methods for comparing and optimising control strategies.

References

[1] Kouro, S., Malinowski., M., Gopakumar, K., et al.: 'Recent advances and industrial applications of multilevel converters' *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, Aug. 2010, pp. 2553–2580

[2] Kouro, S., Rodriguez, J., Wu, B., et al.: 'Power the future of industry' *IEEE Trans. Ind. Electron.*, July/Aug 2012, pp. 26–38

[3] J. Rodríguez, B. Wu, S. Bernet, J. Pontt and S. Kouro, "Multilevel voltage source converter topologies for industrial medium voltage drives," *IEEE Transactions on Industrial Electronics, Special Section on High Power Drives*, Vol. 54, No. 6, pp. 2930–2945, December 2007.

[4] L. G. Franquelo, J. Rodríguez, J. I. Leon, S. Kouro, R. Portillo, M. A. M. Prats, "The Age of Multilevel Converters Arrives", *IEEE Industrial Electronics Magazine*, pp. 28-39, June 2008.

[5] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications", Industrial Electronics, IEEE Transactions on, Volume 49, no. 4, pp. 724 - 738, Aug. 2002.

[6] D. G. Holmes and T. A. Lipo, "*Pulse width modulation for power converters*. Piscataway," NJ: IEEE Press, 2003.

[7] B.McGrath and D. G. Holmes, "Analytical determination of the capacitor voltage balancing dynamics for three phase flying capacitor converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1425–1433, Jul./Aug. 2009.

[8] T. Meynard, M. Fadel, and N. Aouda, "Modelling of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 356–364, Jan. 1997.

[9] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858– 867, Aug. 2002.

[10] Xiaojie Shi, Zhiqiang Wang, Leon M. Tolbert and Fred Wang "A Comparison of Phase Disposition and Phase Shift PWM Strategies for Modular Multilevel Converter," Energy Conversion Congress and Exposition (ECCE), IEEE, pp. 4089-4096, Sep. 2013.

[11] D.-W. Kang, B.-K. Lee, J.-H. Jeon, T.-J. Kim, and D.-S. Hyun, "A symmetric carrier technique of CRPWM for voltage balance method of flying capacitor multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 879–888, Jun. 2005.

[12] B. McGrath, T. A. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[13] T. Meynard and H. Foch, "Dispositif e´lectronique de conversiond'e´nergie e´lectrique," French Patent 267 971 5B1, Jan. 29, 1993.

[14] Alstom.. *www.alstom.com/*. [ONLINE] Available at : http://power-conversion.enseeiht.fr/DCAC/Xlevel_Technology_with_VDM6000.pdf. [Accessed 23 November 2017].

[15] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): Properties and design," in *Proc. IEEE 32nd Power Electron. Spec. Conf.*, Jun. 17–21, 2001, vol. 3, pp. 1583–1588.

[16] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[17] M. Tariq, M. T. Iqbal, A. Iqbal, M. Meraj, M. Roomi and M. S. Khan, "Comparative analysis of carrier schemes for PWM in multilevel PUC inverter for PV applications," 4th International Conference on Dev. Ren. Energy Tech, Jan. 2016.

[18] S. G. Lee, D. W. Kang, Y. H. Lee, and D. S. Hyun, "The carrier-based PWM method for voltage balancing of flying capacitor multilevel inverter," in *Proc. IEEE PESC'00*, vol. 1, 2001, pp. 126–131.

[19] Y. Lei, S. Qin, I. Moon, Z. Ye, and R.C.N. Pilawa-Podgurski, “A 2 kW, single-phase, 7-level flying capacitor multilevel inverter with an active energy buffer,” *IEEE Trans. Power Electro*., vol. 32, no. 11, Nov. 2017.

[20] B. McGrath and D. G. Holmes, “Enhanced Voltage Balancing of a Flying Capacitor Multilevel Converter Using Phase Disposition (PD) Modulation,” *IEEE Trans. Power Electron*., vol. 26, no. 7, July 2011.

[21] S, Thielemans and J. Melkebeek “Improved natural balancing with modified phase-shifted PWM for single-leg five-level flying-capacitor converters,” *IEEE Trans. Power Electron*., vol. 27, no. 4, pp. 1658- 1667, April 2012

[22] B. M. Song, J. S. Lai, C. Y. Jeong, and D. W. Yoo, “A soft-switching high-voltage active power filter with flying capacitors for urban Maglev system applications,” in *Proc. IEEE/IAS Annu. Meeting*,Chicago, IL, vol. 3, pp. 1461–1468, 2001.

[23] C. Feng, J. Liang, and V. G. Agilidis, “Modified phase-shifted PWM control for flying capacitor multilevel converters,” *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178-185, Jan. 2007.

[24] L. Xu and V. G. Agelidis, “Active capacitor voltage control of flying capacitor multilevel converters,” Proc. Inst. Elect. Eng., vol. 151, no. 3, pp. 313–320, May 2004.

[25] N. Celanovic and D. Boroyevich, “A fast space-vector modulation algorithm for multilevel three-phase converters,” *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

[26] J. Amini, “An Effortless Space-Vector-Based Modulation for *N*-level Flying Capacitor Multilevel Inverter with Capacitor Voltage Balancing Capability,” *IEEE Trans. Power Eectron.*, vol. 29, No. 11, pp. 6188-6195, Nov. 2014.

[27] D. Jiang, and F Wang, “Study of analytical current ripple of three-phase PWM converter,” *IEEE Trans*. APEC, Feb. 2012

[28] D. Grandi, and J. Loncarski, “Evaluation of current ripple amplitude in three-phase PWM voltage source inverters,” 8th IEEE International Conference on Compatibility and Power Electronics, CPE, June. 2013.

[29] K. Sekhar, and S. Srinivas, “Discontinuous decoupled PWMs for reduced current ripple in a dual two-level inverter fed open-end winding induction motor drive,” *IEEE Trans. Power Electron*., vol. 28, no. 5, pp. 2493-2501, May 2013.

[30] C. Charumit, and V. Kinnares, “Discontinuous SVPWM techniques of three-leg VSI-fed balanced two-phase loads for reduced switching losses and current ripple,” *IEEE Trans. Power Electron*., vol. 30, no. 4, pp. 2191-2204, May 2015.

[31] I. Fadlika, and P. A. Dahano, “A new approach to reduce current ripple of PWM inverters by variable switching period,” 8th IEEE International conference on Power Electronics and Motion Control, 2016

[32] H. Kubo, and Y. Yamamoto, “Variable carrier frequency mixed PWM technique based on current ripple prediction for reduced switching loss,” Power Electronics Conference IPEC-Hiroshima, 2014

[33] M. Jones, and J. Prieto, “Switching ripple characteristics of space Vvctor PWM schemes for five-phase two-level voltage source inverters—part 2: current ripple,” *IEEE Trans. Ind. Electron*, vol. 58, no. 7, July 2011

[34] I Afandi, and P. Dahono, “Variable switching period to achieve minimum output current ripple of discontinuous PWM three-phase voltage source inverters,” The 3rd IEEE Conference on Power Engineering and Renewable Energy, ICPERE 2016

[35] T. Bhavsar, and G. Narayanan, “Harmonic Analysis of Advanced Bus-Clamping PWM Techniques,” *IEEE Trans. Power Electron*., vol. 24, no. 10, Oct. 2009, pp. 2347 –2352

[36] P.B. McGrath, and D.G. Holmes, “Analytical modelling of voltage balance dynamics for a flying-capacitor multilevel converter,” *IEEE Trans. Power Electron.*, vol. 23, no. 2, Mar. 2008, pp. 543–550

[37] K. Ramani and A. Krishnan, “High performance flying capacitor based multilevel inverter fed induction motor,” International Journal of Recent Trends in Engineering, vol. 1, no. 24, pp. 98-102, Nov. 2010.

[38] K. Hemicia, A. Zegaouib, A. Aissa Bokhtache, M.O. Mahmoudia, M. Ailleriec,"Three-phases flying-capacitor multilevel inverter with proportional natural PWM control," Energy Procedia, vol. 74, pp. 1061-1070, August 2015,

[39] A. Ruderman, B. Reznikov, and M. Margaliot, "Simple analysis of a flying-capacitor converter voltage balance dynamics for dc modulation," in *Proc. Power Electron. Motion Control Conf.*, Sep. 13, 2008, pp. 260–267.

[40] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Simple time-domain analysis of a 4-levelH-bridge flying-capacitor converter voltage balancing," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2010, pp. 818–823.

[41] A. Ruderman and B. Reznikov, "Five-level single-leg flying-capacitor converter voltage balance dynamics analysis," in *Proc. IEEE 35th Annu. Conf. Proc. Ind. Electron.*, Nov. 2009, pp. 486–491.

[42] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Selfprecharge for single-leg odd-level multilevel converter," in *Proc. IET 5th Int. Conf. Proc. Power Electron., Mach. Drives*, Apr. 2010, pp. 1–6.