Computer-aided design

of

RF MOSFET power amplifiers

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Abstract

The process of designing high power RF amplifiers has in the past relied heavily on measurements, in conjunction with simple linear theory. With the advent of the harmonic balance method and increasingly faster computers, CAD techniques can be of great value in designing these nonlinear circuits.

Relatively little work has been done in modelling RF power MOSFETs. The methods described in numerous papers for the nonlinear modelling of microwave GaAsFETs cannot be applied easily to these high power devices. This thesis describes a modelling procedure applicable to RF MOSFETs rated at over 100 W . This is achieved by the use of cold S parameters and pulsed drain current measurements taken at controlled temperatures. A method of determining the required device thermal impedance is given.

A complete nonlinear equivalent circuit model is extracted for an MRF136 MOSFET, a 28 V, 15 W device. This includes two nonlinear capacitors. An equation is developed to describe accurately the drain current as a function of the internal gate and drain voltages. The model parameters are found by computer optimisation with measured data. Techniques for modelling the passive components in RF power amplifiers are given. These include resistors, inductors, capacitors, and ferrite transformers. Although linear ferrite transformer models are used, nonlinear forms are also investigated.

The accuracy of the MOSFET model is verified by comparison to large signal measurements in a 50 Ω system. A complete power amplifier using the MRF136, operating from 118 MHz to 175 MHz is built and analysed. The accuracy of predictions is generally within 10 % for output power and DC supply current, and around 30 % for input impedance. An amplifier is designed using the CAD package, and then built, requiring only a small final adjustment of the input matching circuit.

The computer based methods described lead quickly to a near-optimal design and reduce the need for extensive high power measurements. The use of nonlinear analysis programs is thus established as a valuable design tool for engineers working with RF power amplifiers.

Preface

The idea for this research project originated from Mr R. Piper of Barcom Electronics, Durban. Having made full use of the empirical methods of designing RF power amplifiers, it became apparent to him that these methods were unable to explain many observed phenomena. The success of computer-aided techniques, when applied to small signal circuits, enhanced the belief that theoretical methods might provide some of these answers.

Mr Piper has been involved in RF power amplifier design at Barcom Electronics for many years, largely with wideband HF and VHF radios. In a subject which must often be discovered piecemeal from numerous articles and application notes, his experience represents a wealth of knowledge. A number of important techniques, such as the high power impedance measurement, and many other items of practical information, have been learnt from Mr Piper. The excellent results which he has obtained, using largely empirical methods, represent a standard against which theoretical techniques can be measured.

This research began in March 1990, at the University of Natal, under the supervision of Dr H.C. Reader. Unless specifically indicated to the contrary, this thesis is the author's own work, and has not been submitted in part, or in whole, to any university other than the University of Natal.

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Mr R. Piper originated this research program and supported it throughout its duration, providing invaluable experience and advice. His help on numerous occasions is also gratefully acknowledged.

My supervisor, Dr H.C. Reader, is thanked for his excellent guidance and management of the research program, as well as his enthusiasm and approachability. His active interest and help played a large part in the successes of the program.

Barcom Electronics sponsored the research, generously allowing additional time for further work. The company also provided a PC and hardware, and the extensive use of RF equipment. The Industrial Development Corporation is thanked for computing facilities, without which the research would not have been possible. Many individuals within the Department of Electronic Engineering at the University of Natal helped in various ways. The hardware interface for the computer-controlled drain current measurement system was built by Mr G. Väth. Mr C. Johnson machined parts for the S parameter test fixture. Mr R. Peplow and Mr R. Brain helped solve many computer-related problems. Mr D. Long and Mr P. Facoline are thanked for drawings and Mrs S. Wright for the typing of papers. The typing of this thesis by Mrs C. Brain is gratefully acknowledged. A number of other people within the Department of Electronic Engineering and at Barcom Electronics are thanked for their encouragement and help.

My family played a vital role during the research program. In particular, I would like to acknowledge the contribution of my parents, who have helped enormously. I also thank my wife, Kirsty, for her help, particularly during the writing of this thesis, which she proofread, and for her much appreciated support.

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Abbreviations

ANA	-	Automatic network analyser
CAL	-	Calibration
TSP	-	Temperature sensitive parameter

Introduction

RF power amplifiers are used in a variety of radio communications equipment, a typical application being commercial AM aircraft radios. These cover the frequency band 118 MHz to 136 MHz, with peak envelope powers of about 100 W. Small commercial FM broadcast stations, with carrier powers of several hundred watts, also represent a market for these systems. Although more expensive than bipolar devices, MOSFETs have a number of technical advantages [Motorola AN-878, 1986 and Motorola AN-860, 1986]. A smaller feedback capacitance results in better stability and less variation of input impedance with drive level. MOSFETs also have simpler biasing requirements, lower noise figures and less high-order intermodulation distortion. RF power MOSFETs are therefore used more widely than bipolar devices, except in some low cost applications.

For many years, small-signal circuits have been successfully designed using computer programs, employing various linear circuit representations, such as S parameters. In contrast to this, the design of high power RF amplifiers has largely been based on empirical methods, with simple linear theory to obtain approximate initial values. Computer-aided design techniques were not readily applied to these nonlinear circuits, due to the slowness of time-domain analysis. Also, while the nonlinear modelling of active devices, such as microwave GaAsFETs, is well established, high power active devices present a number of unique difficulties.

Computer-aided design offers several advantages over empirical methods. Firstly, different circuit topologies are quickly evaluated, for a range of operating conditions, without the danger of damaging the active device. Secondly, any circuit voltages and currents may be displayed in the time or frequency domains, which is not practical with physical circuits. This allows insight to be gained into various circuit problems and their solutions. Thirdly, computer-based circuit synthesis and optimisation are powerful techniques which should result in better performance than is obtained by empirical methods only. The scope for physical optimisation of circuits is limited by the range of circuit parameters which may be varied, since many components, such as microstriplines, are not easily adjusted.

Introduction

The computer-aided design of high power RF amplifiers in a commercial environment has been made feasible by the introduction of analysis methods, such as harmonic balance, which are over one hundred times faster than the time-domain approach. Although suffering from some limitations, such as the inability to analyse circuit transients, the harmonic balance method is ideally suited to the analysis and design of RF power amplifiers. Several popular harmonic balance programs have been introduced in recent years, aided by the widespread availability of relatively powerful computers.

In order to analyse RF power amplifiers, component models must be constructed. These include the active MOSFET devices, as well as passive components, such as resistors, inductors, capacitors, microstriplines and ferrite transformers. The principal difficulty in modelling RF MOSFETs with power ratings above about 15 W lies with the required measurements. Firstly, in measuring the S parameters of a biased-on MOSFET, instruments must be protected against possible damage caused by device instabilities. Secondly, during the measurement of drain current characteristics or active S parameters, considerable variation in device internal temperature can occur. Apart from the possibility of the device being destroyed, a MOSFET's characteristics are temperature dependent. The measurements for modelling purposes should therefore be taken near to the device RF operating temperature. Passive component models must yield an acceptable compromise between accuracy and complexity, which affects the time required for a computer-aided design. This implies the selection of appropriate model topologies and, in some cases, such as ferrite transformers, nonlinearities may be considered.

Stability analysis and circuit optimisation are well-established concepts for small-signal design. With nonlinear circuits, however, these operations must be approached differently. Nonlinear design procedures also require special attention.

The thesis has two main topics. Chapters 1 to 4 discuss the component models required for computer-aided analysis, namely the RF power MOSFET, resistors, inductors, capacitors and ferrite transformers. Chapters 5 and 6 describe theoretical and practical aspects of computer-aided analysis and design.

Chapter 1 investigates the modelling procedures which have been applied to active devices such as GaAsFETs, bipolar junction transistors and power MOSFETs. It is found that existing models cannot be applied easily to very high power RF MOSFETs. A new modelling procedure is therefore proposed which is applicable to RF power MOSFETs rated at over 100 W. Chapter 2 describes the S parameter and drain current measurements which are required for the model, while Chapter 3 discusses the extraction of model parameters. This includes an S parameter fitting procedure and an equation to describe the MOSFET drain current characteristics. Chapter 4 deals with model topologies and parameter identification for passive components such as resistors, inductors, capacitors and ferrite transformers. This includes a section on the impedance errors which may occur when complete matching networks are analysed.

Chapter 5 outlines some empirical design techniques and discusses the advantages which may be gained by the use of computer-aided design. The chapter goes on to describe two nonlinear CAD programs, the creation of user-defined nonlinear elements for the proposed MOSFET model, and ends with a discussion of computer-aided design techniques. Finally, Chapter 6 gives two practical examples involving nonlinear CAD packages. These are the analysis of an empirically-designed amplifier and a detailed account of the computer-aided design of an RF power amplifier.

Chapter 1

Nonlinear FET modelling

The large-signal modelling of high power RF MOSFETs has not received nearly as much attention as bipolar and GaAsFET devices. Related examples which were found consider low power amplifiers (5 W) [EEsof's Fables, 1992 and Everard and King, 1987] or deal with switching characteristics [Minasian, 1983 and Nienhaus *et al*, 1980]. Although not directly applicable, reference is made to a number of useful papers on the large signal modelling of microwave GaAsFETs. These provide a level of detail on equivalent circuit modelling which is not found specifically for RF power MOSFETs.

1.1 Model types

A number of different types of transistor models exist and include physical, black box and equivalent circuit models. Physical models are based on the solution of nonlinear differential equations describing electron transport within the FET channel, in two or three dimensions. Either numerical or analytic methods can be used. Accurate solutions are obtained numerically by finite-difference or finite-element analysis [Fichtner *et al*, 1983]. Analytic models solve simplified equations which are obtained by making a number of approximations [Madjar, 1988]. Physical models are used to improve the design of semiconductor devices by computing the effects of various manufacturing parameters such as doping profile and channel dimensions. However, due to long numerical analysis times and the need for access to the device physical parameters, these models are not commonly employed in circuit design.

Black box modelling [Filicori *et al*, 1986], includes large signal S parameter methods [Umeda and Nakajima, 1988]. These allow only a limited range of circuit analyses, such as determination of optimum load impedance and gain compression characteristics, but have the advantage of simplicity.

Equivalent circuit models [Willing *et al*, 1978, Materka and Kacprzak, 1985 and Hoile and Reader, 1992] describe devices using lumped components such as capacitors and voltage controlled current sources. Accuracy over a wide range of conditions is possible. Model parameters can be extracted for any particular device, using ANA and drain current measurements, and inexpensive computing facilities. The models are easily incorporated into commonly available nonlinear CAD packages and allow rapid analysis of large circuits. Equivalent circuit models are therefore the most suitable for the design of RF power amplifiers in a commercial environment.

1.2 Equivalent circuit modelling

The basis of the commonly used modelling procedure, an early example of which is Willing *et al* [1978], is to fit the linearised device model to S parameters measured at a number of bias points. This gives the values of the linear model elements and those of the nonlinear components, such as capacitors, at each bias point. The bias dependent characteristics of the nonlinear components can be described by an equation or look-up table. The drain current element is characterised either by DC measurements or the fitted bias-dependent values of transconductance g_m and output conductance R_{ds}.

A problem with model parameter extraction is that complex models contain too many variables to be determined uniquely by sets of measured S parameters. A solution to this difficulty is to reduce the number of unknowns in the S parameter fitting procedure by calculating some element values through other means. The method of iteratively optimising the model to fit measured data is important in extracting unique and consistent model parameters. This topic is discussed in chapter 3.

1.2.1 GaAs MESFETs and bipolar transistors

A typical example of a linearised large-signal GaAsFET model, including packaging elements, is shown in Figure 1.1. In most cases, models are fitted to S parameters over a wide range of frequencies. Good results are reported by Bunting [1989] using just one frequency. Active S parameters are commonly measured with a number of different gate and drain voltages in the operating region, usually centred around the quiescent point. The model of Materka and Kacprzak [1985] has only one nonlinear capacitor, described by a simple analytic equation with two variables. The value of the first variable is estimated. The second can thus be obtained by fitting the model to S parameters measured at only one bias point, corresponding to the maximum power added efficiency.

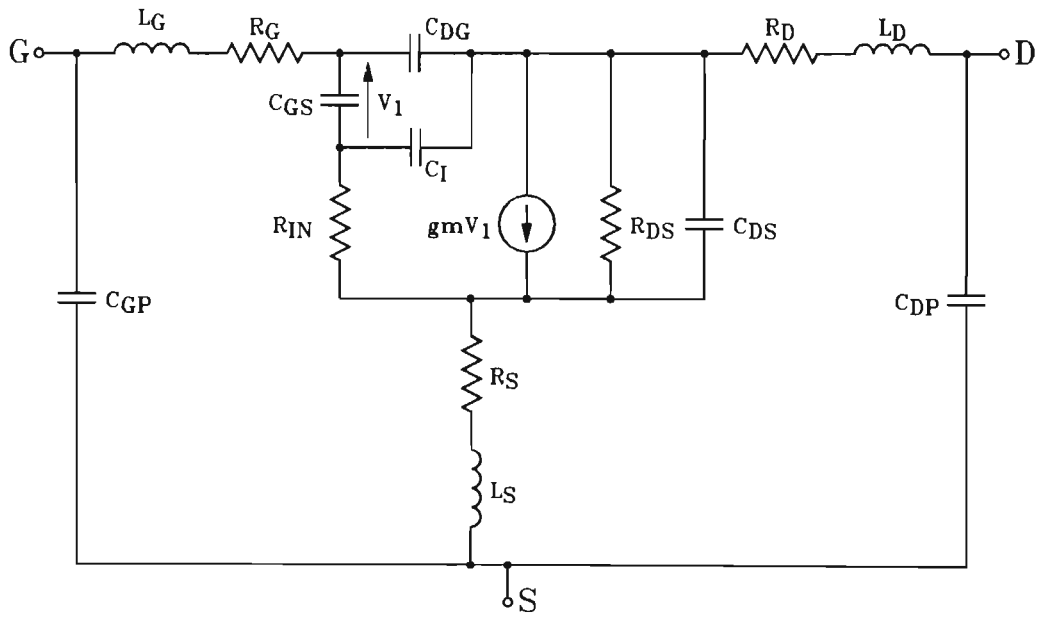


Figure 1.1 A linearised large-signal GaAsFET model

When fitting a model to active S parameters, the voltage-controlled current source exerts a powerful influence. Its linear parameters, g_m and R_{DS} can be obtained from the partial derivatives of an equation fitted to DC drain current measurements [Materka and Kacprzak, 1985]. Another method, which inevitably results in a closer

fit to the S parameters, treats g_m and R_{DS} as variables to be optimised [Bunting, 1989]. These fitted values often conflict with the partial derivatives of the DC drain current equation [Willing *et al*, 1978]. A possible reason for this, given by Smith *et al* [1986], is that the output resistance of GaAsFETs is a function of the measurement frequency. The proposed solution is to map the entire operating region by applying correctly phased 1 MHz half-sinewaves to the gate and drain whilst measuring the drain current. A danger with optimising g_m and R_{DS} is that they may compensate for other aspects of the model, yielding non-physical values.

It is important that a model be unique and consistent with the physical device. Curtice [1988] shows that if all parasitics are included in the optimisation, the final values of model parameters can vary greatly, given different optimisation methods and initial values. The problem is alleviated by determining the model resistances using the methods of Fukui [1979] (DC measurements). The remaining parasitics such as bond wire inductances and package capacitances are obtained by optimisation with cold S parameter data. It is reasoned that the device model is simpler with $V_{DS} = 0$, allowing the parasitics to be identified more accurately. The number of variables in the final optimisation is thus reduced from 16 to 8, making it easier to extract a unique and accurate model. Similarly, Materka and Kacprzak [1985] gives details of the measurement of R_S, R_D and R_G by forward biasing the gate-source and gate-drain junctions. However, the parasitic inductances are extracted with the other elements in a final optimisation.

Lerner and McGuire [EEsof AN14] calculate all the parasitics and uses these to de-embed the intrinsic FET model, which is then optimised. The parasitic component calculations are based on the works of Fukui [1979] and Diamand and Laviron [1982]. Peterson *et al* [1984] determine the parasitic resistances by unspecified physical measurements and the bond wire inductance by analytic means. The remaining model elements are fitted to measured S parameters.

A new method of modelling the package elements is presented by Rodriguez-Tellez and Baloch [1991]. This involves measuring the device chip and package together

and then measuring the S parameters of the chip by itself. A special probe is designed for the second procedure. The package parameters are optimised such that the model of chip and package fits the measured characteristics.

Intrinsic model elements may be nonlinear bias-dependent components described as a function of one or two voltages. Alternatively, they may be assumed to be linear. Various combinations of these three levels of complexity are found in the literature. Materka and Kacprzak [1985] treats C_{GS} as a function of the voltage across it, and makes the assumption that C_{DG} and C_{DS} are linear. Curtice [1988] uses $C_{GS}(V_{GS})$, $C_{DG}(V_{DG})$ and a linear C_{DS}. In the model of Bunting [1989], R_I, C_{GS} and C_{DG} are nonlinear elements, each represented by two-dimensional functions of V_{GS} and V_{DS}.

1.2.2 Power MOSFETs

High power MOSFETs present a number of difficulties which rule out the direct use of many methods which have been successfully applied to other devices. The heat dissipation and power capabilities of the larger RF MOSFETs restricts the type of measurements that can be made for modelling purposes. The primary danger when measuring active S parameters is that of device instability causing instrument damage. Additionally, high heat dissipation can result in considerable variations in channel temperature. Only a limited range of bias points can be measured under steady state conditions without destroying the device. Since MOSFET characteristics are temperature dependent, the modelling measurements should be taken with the channel near to the RF operating temperature. None of the papers on equivalent circuit modelling which were reviewed, dealt with the question of device temperature. Measuring drain current characteristics with a curve tracer will prevent excessive device temperature. The actual temperature, however, will be unknown and different for the various curves.

With a 5 W MOSFET, an ANA could be protected by placing attenuators between its ports and the test jig. However, with an MRF136 15 W device and an HP8510B ANA, attenuators of 13 dB and 26 dB would be required in the gate and drain paths

respectively. The resulting loss of dynamic range prevents a satisfactory calibration from being made. A possible solution might be to construct a rugged low cost test-set so that protection would not be required. Even if this problem were overcome, it would nevertheless be desirable to control the device temperature through the use of pulsed S parameter measurements. With an ANA, it is impractical to measure the S parameters of a FET with the bias pulsed for less that 1 ms. However, thermal data indicates that pulse times of less than 100 μs are required to sufficiently limit the temperature rise during high dissipation measurements.

The technique used for GaAsFETs where model resistances are determined by forward biasing various junctions is not applicable to power MOSFETs. For these devices, the gate is insulated and only the drain and source terminals connect through a p-n junction.

Existing models for RF power MOSFETs reflect the restrictions which are described. Simple methods are used and power ratings are low. Examples of these models are given in the remainder of this section, and since they are closely related to the RF power types, switching MOSFET models are included.

A simple equivalent circuit model for a 5 W RF power MOSFET is used by Everard and King [1987] to analyse a class E amplifier. The drain current characteristics of the device are measured using a curve tracer, an instrument which typically sweeps each gate voltage in an 80 μs pulse. Active S parameters are measured for various gate-source and gate-drain voltages, although it is not clear what dissipation levels are reached. The S parameters are converted to Y parameters and the intrinsic capacitors obtained from the following equations:

$$C_{DG} = -I_M(Y_{12}) / \omega \quad \textbf{(1.1)}$$

$$C_{DS} = I_M(Y_{22}) / \omega - C_{DG} \quad \textbf{(1.2)}$$

$$C_{GS} = I_M(Y_{11}) / \omega - C_{DG} \quad \textbf{(1.3)}$$

These equations are approximate since the package inductances and device series resistances are not considered. Parasitic packaging components are specified but their origins are not described. The model is verified at 155 MHz where the measured efficiency is 65% with a calculated value or 75%. The amplifier output power is predicted to within a few percent.

The intrinsic capacitances of an IRF130 switching MOSFET are determined by Minasian [1983] using the same equations as **(1.1), (1.2) and (1.3).** However, the Y parameters are measured directly at 1 MHz in the cutoff, pinchoff and ohmic regions of operation. It should be noted that, since Y parameter measurements require a short circuit to be applied to one device port, instability would almost certainly result with an RF power MOSFET. The series package inductances are assumed to be negligible but those of the external connecting wires are calculated using an analytic expression. Equations from a SPICE MOSFET model, with square-law relationships, describe the drain current characteristics using only four parameters. Three of these, V_T, B and R_S, are determined from the I_D curves in the pinchoff region, while the fourth, R_D, is determined in the ohmic region using a value of R_{DSon} from the device data sheet. The gate resistance R_G is found by measuring the time constant of the step response when a small pulse is applied to the gate. For this, the MOSFET should remain in the cutoff region with a large drain-source voltage. To calculate R_G, the values of C_{GS}, C_{DG} and the generator impedance must be known. The model is verified by analysing the switching of a resistive load. Good agreement is obtained for the turn-on and turn-off switching waveforms.

A notable feature of Nienhaus *et al* [1980] is that all the model parameters are obtained from the standard device data sheet. The parameters, including R_S and R_D, which define the static characteristics, are determined from different regions of the drain current curves. It is pointed out that the well established models applicable to low power MOSFETs are not appropriate for high power devices. The theoretical square-law relationship between drain current and gate-source voltage in the pinchoff region does not accurately describe the power MOSFET's characteristics which become more linear at high current levels. The underlying phenomena such as

surface scattering can be lumped together and modelled by a parasitic source resistance. The three intrinsic capacitors are calculated from the data sheet values of C_{rss}, C_{iss} and C_{oss}, using the equations:

$$C_{DG} = C_{rss} \quad \textbf{(1.4)}$$

$$C_{GS} = C_{iss} - C_{rss} \quad \textbf{(1.5)}$$

$$C_{DS} = C_{oss} - C_{rss} \quad \textbf{(1.6)}$$

The gate resistance R_G is calculated from the specified device turn-on and turn-off delay times. Series inductances are not included in the model. The accuracy of the model's switching waveforms is reasonable but not as good as that demonstrated by Minasian [1983].

With the exception of the Y parameter measurements and the use of data sheet transient delay times, the methods described for switching MOSFETs are applicable to RF power MOSFETs.

It is seen that the modelling techniques available for RF power MOSFETs are less sophisticated than those for GaAsFETs. As a consequence of the described measurement difficulties, relatively simple methods have been used which apply only to low power devices.

1.2.3 MOSFET model topologies

The basic device structure currently employed with RF power MOSFETs is the n channel enhancement double-diffused vertical DMOS. A chip in a single packaged device commonly consists of numerous cells. Although different cell shapes under various tradenames are used, the essential structure remains the same. With the exception of very detailed examples, model topologies are therefore universal.

It is preferable to use the simplest model topology which describes the device characteristics adequately. A model with too few elements will inevitably yield poor results. However there are several dangers attached to the use of a complex model. Although a closer fit to measured S parameters is likely, this may simply be the result of adding more degrees of freedom. A better device description is not necessarily implied. Even if a complex model corresponds well to the device physics, the limitations of the optimisation process may yield non-physical element values. This would probably affect the model accuracy in some regions of nonlinear operation more than others, and might not be apparent.

The suitability of a model can be gauged by how closely it replicates measured S parameters. A linearised version of the large-signal model is used to do this. It should be noted that the linear parameters apply for one particular bias point only. A good fit to the S parameters at one bias point does not guarantee accuracy over the entire operating region, which a large signal model topology should be able to achieve.

The following model topologies are evaluated by fitting them to common-source S parameter values obtained from the data sheet of an MRF174 MOSFET. This is a 28 V device with a power rating of 125 W at 100 MHz. The S parameters are measured in the pinchoff region with V_{DS} = 28 V and I_D = 3 A, from 20 MHz to 300 MHz.

A topology which includes only the essential characteristics of the MOSFET is given in Figure 1.2. The capacitors C_{GS}, C_{DG} and C_{DS} may be related to the data sheet values of short circuit input, transfer and output capacitances by equations **(1.4)** - **(1.6)**. The channel current is represented by a voltage-controlled current source, dependent on V_{CGS}, and an output conductance G_D. In the pinchoff region the output conductance is low and this element can be omitted with little change in accuracy. With the exception of S_{12}, the S parameters of the fitted model are close to the data sheet values. The angle of S_{12} incorrectly decreases with frequency and at 300 MHz is in error by over 50 °.

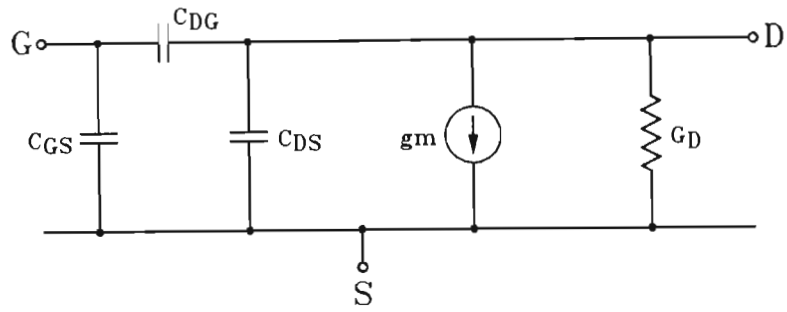


Figure 1.2 Basic MOSFET model

The addition of a single inductor to the source, as in Figure 1.3, corrects the large error in S_{12}. The magnitude errors of all four S parameters are less than 10 % and the angles are within 10 ° of the data sheet values from 20 MHz to 300 MHz.

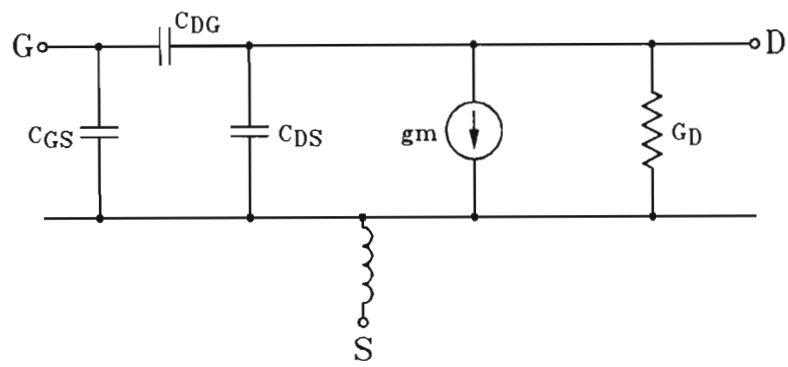


Figure 1.3 MOSFET model with source inductor

A detailed physical structure, Figure 1.4, and its equivalent circuit, Figure 1.5, is now discussed. This has been compiled from Minasian [1983] and [M/A COM PHI AN80-2, 1986]. The intrinsic device is represented more accurately and the major package elements are included. An initial optimisation shows a much closer fit of S_{12} than the model of Figure 1.3, with the other S parameters largely unchanged.

The MOSFET device is formed on an n^+ region with a layer of n^- material above. An ohmic contact joins the drain lead to the n^+ layer. Areas of p and n^+ material are diffused into the n^- layer. The metallic gate lies above the silicon structure, insulated

by an oxide layer. Finally, a metal overlay connects to the p and n^+ source regions. Bond wires connect the gate and source to their respective package leads.

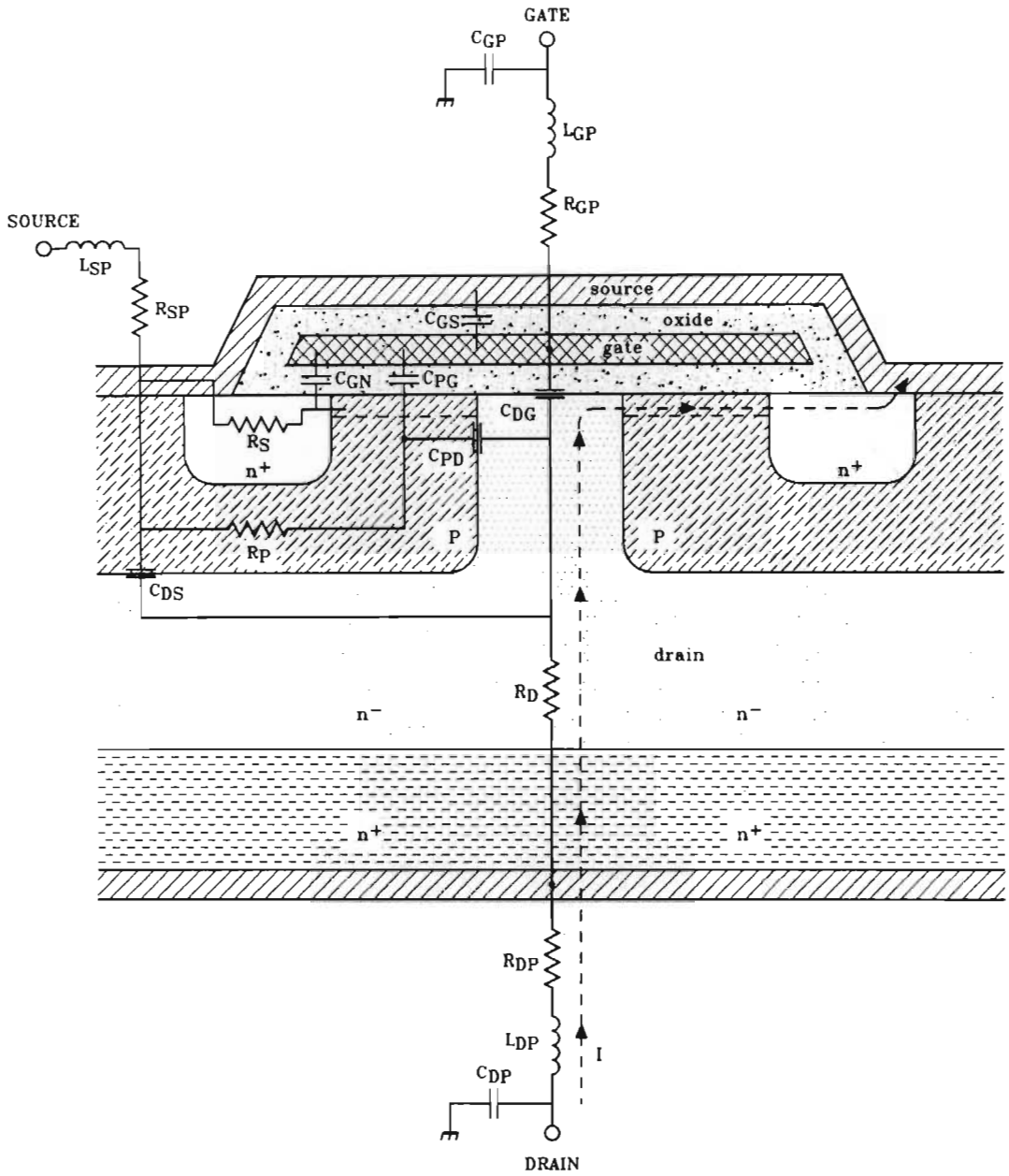


Figure 1.4 Detailed power MOSFET model (physical)

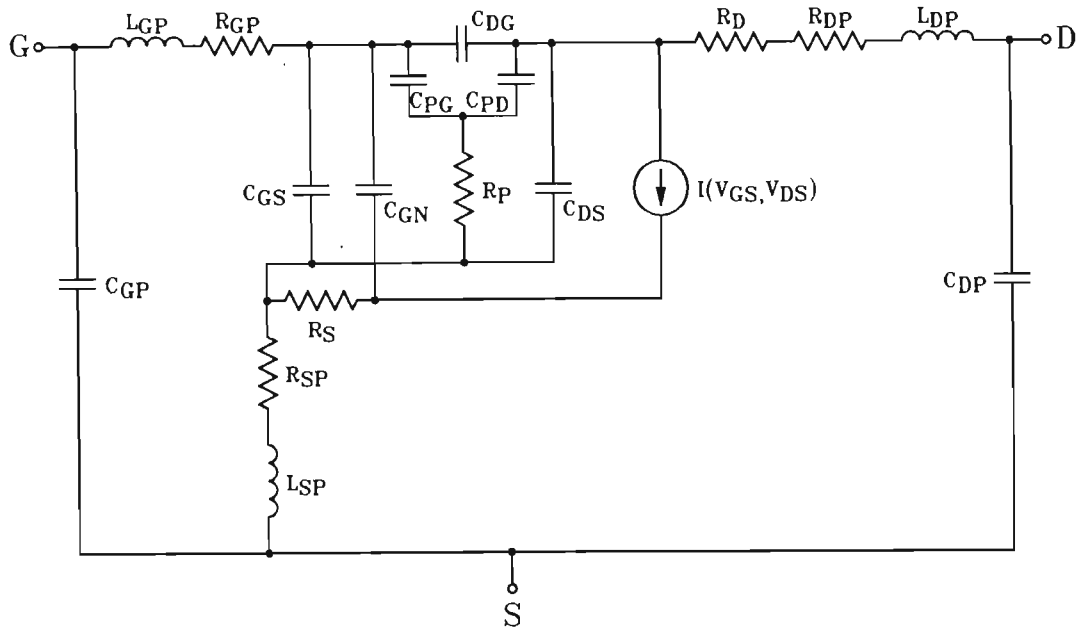


Figure 1.5 Detailed power MOSFET model (equivalent circuit)

The MOSFET is normally operated with positive gate-source and drain-source voltages. Gate-source voltages greater than the threshold value create an inversion layer in the p^+ region under the gate. Current can thus flow through the channel from drain to source. The resistance of the n^- drift region, modelled by R_D, is the most significant along this path. Due to varying constriction of current between the p regions, and other effects, R_D is slightly bias dependent. The DC path also includes R_S in the n^+ region, and the bond wire and contact resistances, R_{SP} and R_{DP}.

The n^-, p and n^+ source regions form a parasitic npn bipolar transistor. Although the base (p) is shorted to the emitter (n^+), a transient drain voltage can couple through C_{PD} and cause a sufficient potential difference across R_P to turn the transistor on . Correct design, however, prevents this.

The p-n^- junction, corresponding to the base collector junction of the parasitic bipolar transistor, is normally reverse biased. Negative drain source voltages will, however, result in a current flowing through this junction.

There are two important nonlinear capacitors in the model of Figure 1.5. Firstly, C_{DS} represents the capacitance of the reverse biased p-n^- junction. For high drain-source voltages, the width of the depletion region increases and the capacitance becomes small. Secondly, C_{DG} models the capacitance from the gate to the drift region between the p structures, as well as to the drain ends of the channels. The nonlinearity of C_{DG} is due, in part, to the depletion region width varying with bias.

The gate-source capacitance C_{GS} occurs between two metallic layers and is therefore linear. The capacitance from the gate to the n^+ source region is modelled by C_{GN}. The element C_{PG} represents the charge stored in the inversion layer and the underlying p region due to the gate voltage. Also near to the channel is C_{PD}, which is similar to C_{DS}, but separated by R_P. The package model includes series resistance and inductance for all three terminals with shunt capacitances on the gate and drain.

The relatively simple model of Figure 1.3 shows that a good fit to S parameters can be obtained without resorting to complex topologies. A model with the level of detail shown in Figure 1.5 would not generally be used, due to the difficulty of extracting physically consistent model parameters. As a result, many circuit oriented modelling programs employ uncomplicated intrinsic models, which nevertheless can provide good results. In the following section, such a model is developed from the topology of Figure 1.5.

1.3 RF power MOSFET model

A modelling procedure for high power RF MOSFETs is now outlined. The model is intended for circuit analysis and can be incorporated readily into suitable nonlinear CAD programs. The required device measurements are made without difficulty and the model parameters are extracted by optimisation using a PC.

Figure 1.6 shows the topology of the proposed model, which consists of the intrinsic device and package elements. With reference to Figure 1.4 and Figure 1.5, it is seen that the full package model is retained. However, the intrinsic model is reduced to four major elements, a gate-source, feedback and drain-source capacitor, and a voltage-controlled current source. This intrinsic model is obtained from Figure 1.4 and Figure 1.5 as follows. The resistances R_D and R_{DP} are in series and can be shown as a single element R_{DP}, in Figure 1.6. The impedance of R_P is low compared to that of the adjacent capacitances and can be assumed to be negligible. Accordingly, C_{PD} is partly absorbed into C_{DS} and C_{PG} into C_{GS}. The remaining series combination of C_{PG} and C_{PD} is added to C_{DG}. Similarly, R_S can be omitted and C_{GN} combined with C_{GS}.

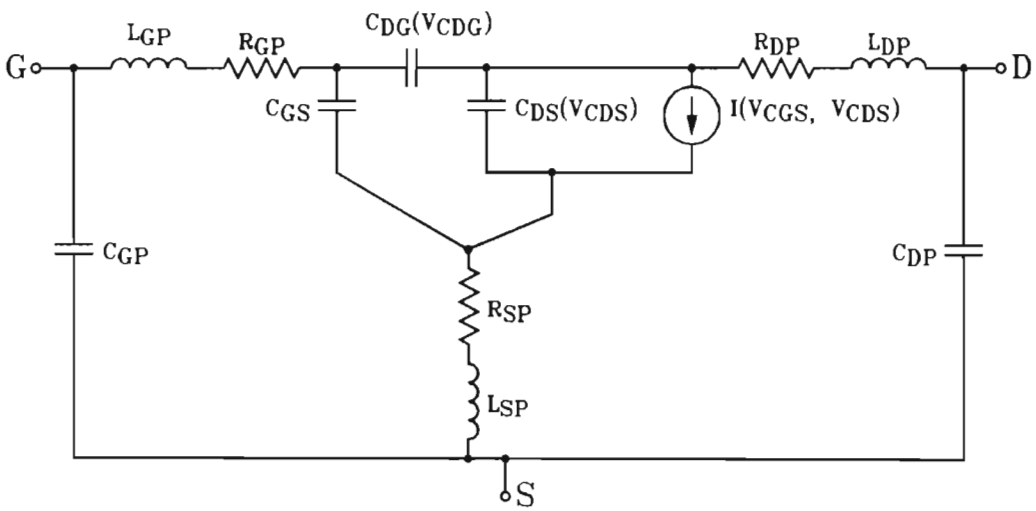


Figure 1.6 RF power MOSFET model

The clear physical significance of many elements in the detailed model is lost when they are combined into the model of Figure 1.6. For example, R_{DP} in Figure 1.6 may be found to be slightly bias dependent due to inclusion of the resistance of n^- material between the p regions. The element C_{DS} is no longer the capacitance of a reverse biased junction only, but is modified by the addition of C_{PD}. The nonlinear capacitor C_{DG} is similarly affected. Due to the dominance of the capacitance between gate and source metallisations, C_{GS} remains a linear component in Figure 1.6. The equation used to describe the drain current characteristics of the model in Figure 1.6 would

necessarily be different in form from that applicable to the detailed model. As a result of R_S not being included, the control voltages for the current source are changed.

The RF power MOSFET model in Figure 1.6 contains two nonlinear capacitors, C_{DS} and C_{DG}. Each of these capacitors is taken to be a function of the voltage across itself. The current source is a function of the voltages across C_{GS} and C_{DS}. All other elements in the model are considered to be linear. The nonlinear components are functions of their instantaneous control voltages, i.e. the quasi-static assumption. In particular, the current source contains no time delay element of the form seen in some large-signal GaAsFET models [Bunting, 1989].

The model parameters are extracted in two separate procedures based on cold S parameters and pulsed drain current measurements. The cold S parameters are measured over a wide frequency range with zero gate voltage, for a number of drain-source voltages from zero up to the safe device limit. The drain current is measured for a variety of gate-source and drain-source voltages. The measurement is made at the end of a fixed-length pulse, allowing the measurement temperature to be controlled.

The exclusive use of cold FET measurements is proposed to solve the problem of ANA protection and device heating. With $V_{GS} = 0$, zero DC drain current flows. Under these conditions, destructive oscillations are prevented and the device can be safely connected to a standard ANA directly. Also, with the heat dissipation equal to zero, the entire device merely has to be maintained at the required measurement temperature. A disadvantage of these cold FET measurements is that the device is measured under voltage and current conditions far removed from those under which it normally operates. Information about the device is therefore lost. Firstly, some nonlinear elements within a MOSFET show a current dependence, which cannot be determined from cold measurements. Secondly, the intrinsic capacitances must be described as functions of a single voltage. Thirdly, the bias dependence of C_{GS}, if any, cannot be determined, and a linear element must be used. However, it appears that the nonlinear elements in the MOSFET model are only weak functions of current

and are well described by a single voltage variable. The accuracy of the assumed voltage dependencies of C_{GS}, C_{DG} and C_{DS} is confirmed in Everard and King [1987] and Minasian [1983].

A measurement technique is developed, whereby the device drain current is determined under pulsed conditions, with a fixed pulse length and low duty cycle. An initial temperature is calculated for each bias point such that the channel temperature rises to the desired value at the end of the pulse, when the measurement is taken.

The model parameters are identified in two consecutive operations. Firstly, the model is fitted to the cold S parameters. Since these are measured with $V_{GS} = 0$, the voltage-controlled current source in the model is inactive. The drain current measurements are therefore not used in the S parameter fitting procedure. Typically, the S parameters are measured for ten different drain-source voltages. The model is fitted simultaneously to all these sets, using common variables for the linear elements and equations to describe the bias dependent capacitances. This method leads to the extraction of physically consistent package element values. Secondly, an equation is fitted to the measured values of drain current, describing the current as a function of the two voltages, V_{CGS} and V_{CDS}. As a result of the assumptions made, this equation need not be physically significant. The values of R_{SP} and R_{DP} are required from the S parameter fitting procedure for this step, since the current flow causes a voltage drop across the two resistors.

For the CAD programs, the nonlinear capacitances must be described in terms of charge and the derivative of this with respect to voltage. The derivative of charge is the capacitance obtained from the S parameter fitting procedure. The drain current element description requires the instantaneous current as a function of V_{CGS} and V_{CDS}, as well as the partial derivatives of current with respect to the two voltages.

The procedure which is presented solves a number of existing problems regarding the modelling of high power RF MOSFETs and can be applied to devices rated at over 100 W. Cold S parameter measurements obviate the need to protect the ANA and can be made under steady-state conditions with the device held at the RF operating temperature. Drain current characteristics are determined under pulsed conditions, enabling the measurements to be taken at a particular channel temperature. The model parameters are determined in two separate optimisations, fitting the linearised model to the S parameters and an equation to the drain current measurements. The modelling technique does not require any knowledge of the device physics and can be employed by non-specialists in an engineering environment.

Chapter 2

Device measurements for MOSFET modelling

The MOSFET model proposed in chapter 1 requires the measurement of drain current characteristics and S parameters. The drain current measurements to be described are pulsed. Using the concept of thermal impedance, this technique allows the device temperature to be controlled. Cold S parameters, with $V_{GS} = 0$, are measured for a number of drain voltages.

2.1 Drain current

As a result of high heat dissipation, RF power MOSFETs typically operate at elevated temperatures. Since the drain current characteristics are temperature dependent, large errors can occur if thermal aspects are not considered. To limit the device temperature to safe levels, power MOSFETs are commonly measured using a curve tracer, which repeatedly applies pulses of fixed length. However, due to the wide range of heat dissipation in the operating region, the measurements are taken at differing channel temperatures. The low dissipation measurements will be near room temperature whilst high dissipation measurements reach greater temperatures, depending on the pulse length. An important objective is thus to measure the drain current characteristics under thermal conditions similar to those experienced in RF operation.

2.1.1 Temperature control

It is commonly assumed that the temperature differential between a transistor junction and some reference point, such as its case, is proportional to the heat dissipation and a device constant known as thermal resistance. This is, however, a simplification. Firstly, an RF power MOSFET consists of a parallel combination of many small MOSFET structures, each with different thermal paths. Secondly, the region of heat dissipation is not fixed but varies with voltage and current. This phenomenon is

described for bipolar transistors by Oettinger *et al* [1976] and Webb [1983]. A similar situation is expected with power MOSFETs, due to their drain current temperature coefficients which vary from positive to negative with increasing current. Thirdly, the heat capacity and thermal resistivity of materials in the device, such as silicon, vary with temperature. The heat capacity of silicon increases with temperature [Lovell *et al*, 1976, p109], together with its thermal resistivity [Motorola AN-790, 1986]. From a temperature of 25 °C to 200 °C, the thermal resistivity of silicon increases by 80 %.

Due to thermal inertia, resulting from heat capacity, it can be assumed that for steady-state RF operation above 1 MHz, the channel temperature remains constant. Thus for any particular set of operating conditions, such as output power and load impedance, a unique three-dimensional temperature distribution exists throughout the MOSFET chip. A finite-element model is able to take into account the instantaneous distribution of the heat dissipating region, as well as the temperature-dependent thermal characteristics of the device material. An equivalent circuit model, however, must necessarily include a number of simplifications.

A method of measuring the drain current characteristics of a MOSFET under thermally-controlled conditions is proposed. This consists of applying a fixed-length pulse to the gate, with the drain supplied from a constant voltage through a resistor. The MOSFET's power dissipation is measured during a trial pulse. An initial device temperature is calculated, such that, at the end of a similar pulse, the average channel temperature will rise to that estimated for typical RF operation. The values of gate and drain voltage and drain current are measured near the end of the pulse at this temperature. An appropriate initial device temperature can thus be determined for each point in the drain current characteristics, depending on the particular dissipation level. Figure 2.1 gives the channel temperature versus time for the thermally-controlled measurement of two pulses having different dissipation levels. The channel temperature is the same at the end of both pulses, due to the lower initial temperature provided for the high dissipation pulse. The calculation requires a value of thermal impedance Z_{thJC}, defined here as the change in average channel temperature per unit of heat dissipation, for a single isolated pulse of given length. The power dissipation

must be assumed to be constant during the pulse. It should be noted that this definition considers the average channel temperature, unlike reliability calculations where the maximum temperature is important in determining the safe operation of the device [Oettinger *et al* , 1976]. An average value, with the temperature measured by electrical methods, will be more relevant to RF operating conditions than the maximum. The thermal impedance tends to zero for very short pulses and to the well known thermal resistance for long pulse times approaching steady-state conditions.

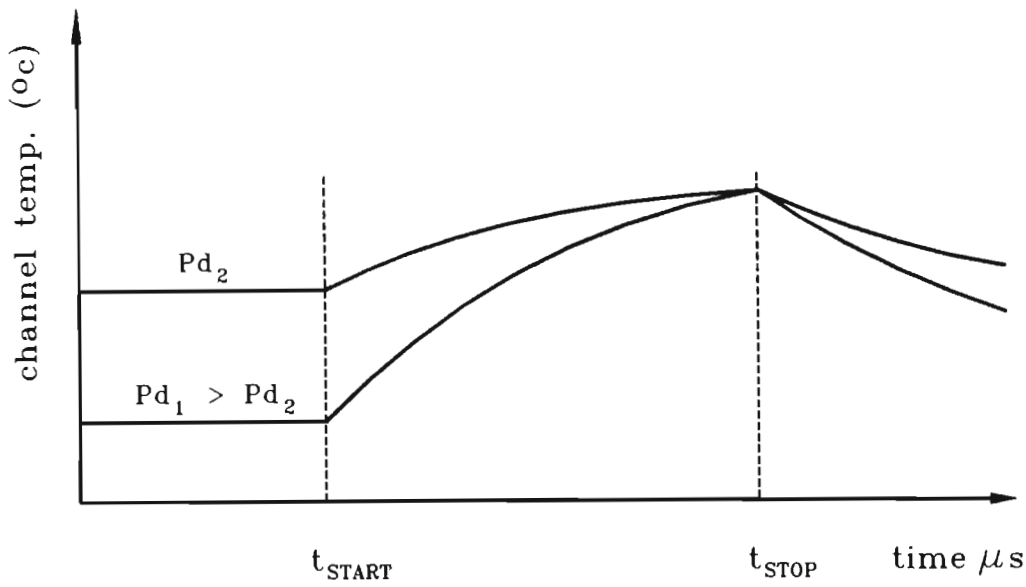


Figure 2.1 Thermally-controlled drain current measurements for two pulses having different dissipation levels

The value of the described measurement technique is evaluated by comparison with methods which disregard the device temperature, in terms of the likely errors in measured drain current. An MRF136 device is used as an example.

A significant limitation of the given temperature-control method is that a single value of thermal impedance is assumed, when in fact this varies with temperature. In section 2.2, the thermal impedance is measured for small temperature changes, at various average temperatures. The change in thermal impedance can be estimated by assuming that it occurs entirely as a result of variation in the thermal resistance of

silicon, ignoring the increase in thermal capacity, which is of less significance. The measured and calculated values of thermal impedance for an MRF136 are given in Table 2.1, using published values for the thermal resistivity of silicon in the calculations [Motorola AN-790, 1986].

Table 2.1 Measured and calculated values of thermal impedance Z_{thJC} versus temperature for an MRF136, and the assumed thermal resistivity of silicon. Note: k = thermal conductivity

Device temp. (°C)	27	55	75
Z_{thJC} (°C/W) Meas.	0.83	0.94	1.07
Z_{thJC} (°C/W) Calc.	base	0.93	1.00
1/k (cm.deg/W)	0.722	0.811	0.874

For a 100 μs pulse which increases the channel temperature from 27 °C to 75 °C, a value of thermal impedance of 0.94 °C/W may be chosen. The actual rate of change of temperature will initially be lower than expected but greater near the end of the pulse. The error in calculating the temperature rise will thus be averaged to some value smaller than the total change in thermal impedance, a worst-case estimate being 15 %. Thus, for the 48 °C change in temperature, the calculated value could be in error by 7 °C. The effect of this temperature error depends on the device temperature coefficient, which is largely a function of drain current. Using a value of 750 mA, which has a large negative coefficient, the MRF136 device data sheet suggests a drain current error of less than 1.5 %. This is, however, a severe example, since the majority of measurements involve much smaller temperature variations, with correspondingly better prediction of the final temperature. The remaining errors for the described method are not easily determined. However, due to the negative temperature coefficient for high currents, which inhibits uneven current sharing between MOSFET cells, these errors are expected to be small.

The errors incurred by measuring drain current characteristics without temperature control depend entirely upon the method used. It is most likely that the measurement would be pulsed, with the device case near to room temperature. Under these conditions, the drain current error will depend on the dissipation level and the temperature coefficient of the MOSFET at the particular drain current. High dissipation measurements will cause large temperature changes, with final temperatures nearing the desired level. For intermediate current levels, approximately 350 mA for the MRF136, the temperature coefficient is small, nullifying the effect of large temperature errors. The measurement error is worst for low current levels, as shown by the following hypothetical example derived from DC measurements of an MRF136. With V_{GS} = 3.85 V and V_{DS} = 28 V, the drain current was measured to be 25 mA at 25 °C and 48.2 mA at 75 °C. Using a thermal resistance of 3.1 °C/W, this implies channel temperatures of 27.2 °C and 79.2 °C respectively. The example assumes a pulsed measurement with an intended channel temperature of 79.2 °C, for the same gate and drain voltages. If the sink temperature is 26.3 °C, then assuming a thermal impedance of 1 °C/W, the measurement temperature will be about 27.2 °C, giving the current of 25 mA, which is 40 % in error.

It is thus seen that large errors in power MOSFET drain current measurements can occur if thermal effects are not considered. The method of temperature control which is given reduces these errors considerably.

2.1.2 Measurement system

A computer-driven system was built to allow measurement of MOSFET drain current characteristics, using the method of temperature control described in section 2.1.1. This consists of a PC(AT), a PC-30 card, which provides A/D, D/A and digital I/O functions, and analog circuitry.

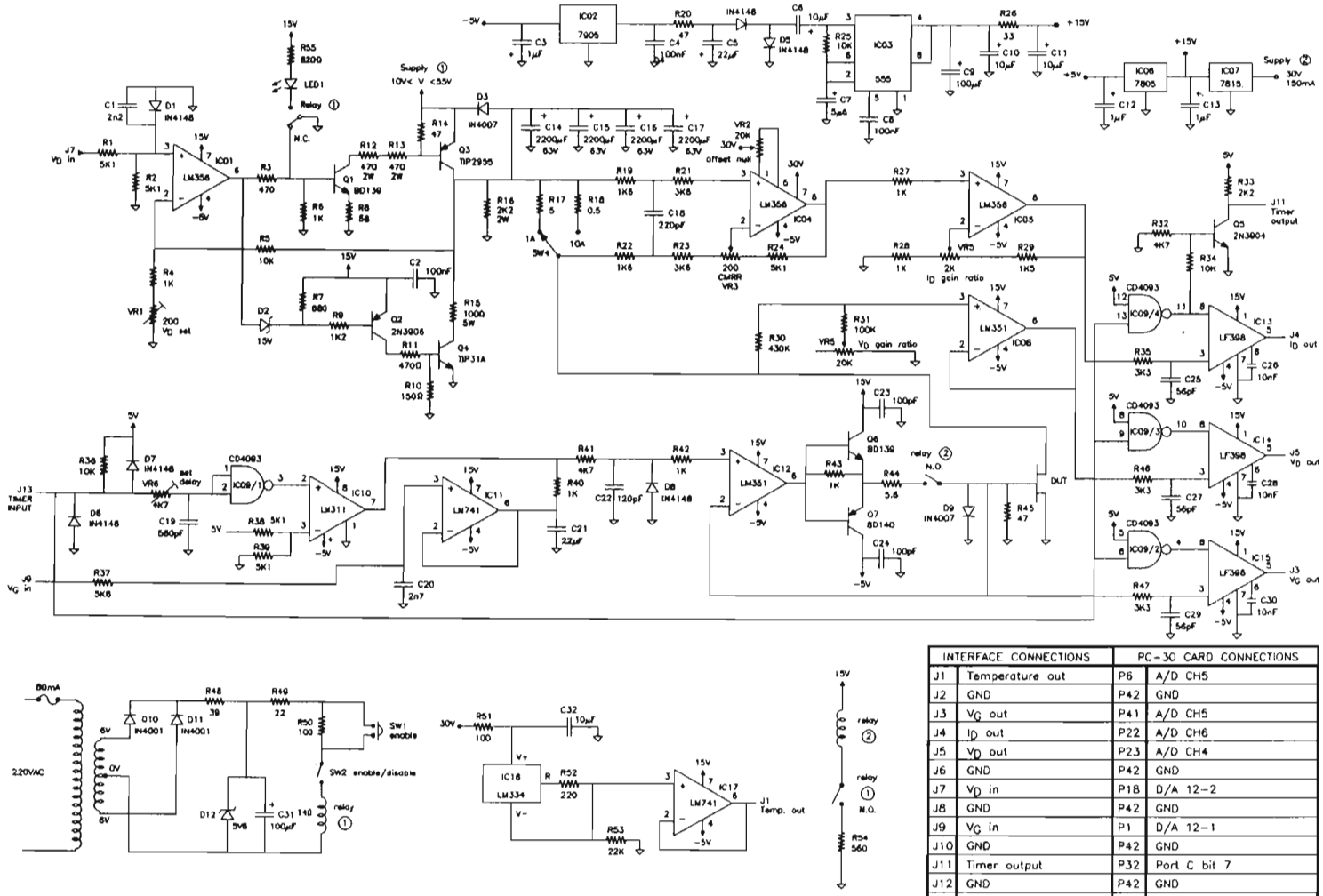
The basic measurement procedure is as follows. With the drain supply voltage applied to the device under test, a timer is triggered, initiating the gate voltage pulse. Three sample and hold (S/H) circuits track the gate voltage, drain voltage and drain current. Just prior to the end of the gate pulse, these values are held simultaneously. A fourth output gives the heatsink temperature. After the gate voltage has returned to zero, the measurements are read into the computer. This is repeated for a series of gate and drain voltages, typically yielding 400 measured points. A heatsink temperature is calculated for each point such that, at the end of the pulse, the channel temperature will reach the desired value. The MOSFET is externally heated for the temperature-controlled measurements. These begin with the heatsink near room temperature for high dissipation measurements and proceed to high sink temperatures for low dissipation points. Each measurement is taken as the heatsink reaches the appropriate temperature. The drain current, and hence dissipation , will be slightly different from the initial set of measurements, due to the MOSFET temperature coefficient. The measurements can, however, be repeated with a falling sink temperature, using the more accurate temperature-controlled values of dissipation.

The PC-30 card interfaces between the computer and analog circuitry. It includes two 12-bit D/A converters, a multiplexed 16-channel, 12-bit A/D converter and TTL input/output ports. The A/D and D/A converters operate with DC voltages of 0 V to 10 V. A digital timer, driven from a crystal oscillator, controls the length of gate pulse.

The analog circuitry, to which the MOSFET under test is connected, is shown in Figure 2.2. A number of functions are performed. The gate input voltage J9, from the PC-30 card D/A converter, is buffered and then switched by the timer input J13. A low impedance drive, with high current capability, connects to the MOSFET gate. The gate voltage can thus be pulsed, with an amplitude of 0 V to 10 V. The timer signal is fed back to the PC-30 card via J11 to be monitored. The drain input voltage J7 is translated up to a value of 0 V to 50 V, which is held by a large bank of capacitors. This allows drain currents of up to 10 A to be supplied for short durations. The drain current flows through a resistance, which is selected according

to the maximum value of current. The gate voltage is fed directly to its S/H circuit (LF398), while the drain voltage and current values are first translated back to 0 V to 10 V levels. An LM334 IC provides a steady indication of the heatsink temperature. The S/H circuits are switched to hold mode with the CMOS-buffered timer signal. A short RC delay prevents the MOSFET gate voltage from reverting to zero during this S/H transition. The outputs of the three S/H circuits, representing gate voltage, drain voltage and drain current, are returned to the PC-30 card via J3, J5 and J4 respectively. The heatsink temperature is given by a 0 V to 10 V signal at J1. Two relays disable the gate and drain voltage supplies in the event of a power failure. This protection is necessary since the D/A converters power up with unknown voltages if the computer is rebooted. The circuit is initially enabled by a manually operated switch.

The measurement system is controlled by a program written in the C language. On running the program, the D/A converters must be set to zero values, allowing the analog circuitry to be enabled. The required gate and drain supply voltages are specified in arrays. For each individual measurement, the drain voltage D/A converter must be set and then the actual drain voltage monitored, by repeated measurements with zero gate voltage. Once the drain voltage has stabilised, the gate voltage is set and the digital timer loaded and triggered. After the timed period has ended, the voltages from the S/H circuits are read in sequentially, followed by the heatsink temperature signal. The time taken for the temperature-controlled measurements is determined by the relatively slow temperature rise of the heatsink, typically requiring 20 minutes. The final set of measurements is saved to an ASCII file.



INTERFACE CONNECTIONS		PC-30 CARD CONNECTIONS	
J1	Temperature out	P6	A/D CH5
J2	GND	P42	GND
J3	V_G out	P41	A/D CH5
J4	I_D out	P22	A/D CH6
J5	V_D out	P23	A/D CH4
J6	GND	P42	GND
J7	V_D in	P18	D/A 12-2
J8	GND	P42	GND
J9	V_G in	P1	D/A 12-1
J10	GND	P42	GND
J11	Timer output	P32	Port C bit 7
J12	GND	P42	GND
J13	Timer input	P21	Timer 2 output

Figure 2.2 Analog circuitry for temperature-controlled drain current measurements

2.2 Thermal impedance

The required value of thermal impedance is defined as the change in average channel temperature per unit of heat dissipation, for a single isolated pulse of constant power. The heat dissipation is measured from the drain voltage and current. The average channel temperature can be inferred from a temperature-sensitive parameter (TSP). Such a MOSFET parameter is the drain current for fixed gate and drain voltages. There are two distinct methods of monitoring temperature in this way [Oettinger *et al*, 1976]. In the pulsed method, the TSP is measured for a number of device temperatures, using a short high-power pulse. The change in temperature during this pulse is assumed to be negligible. Thus, when a much longer pulse having the same gate and drain voltages is applied, the channel temperature can be calculated from the TSP value. The switched method alternates between high and low power conditions. The TSP is characterised with a low current pulse, which is assumed to cause negligible heating. This allows the channel temperature at the end of the high dissipation pulse to be determined from the low current pulse which follows. For MOSFETs, the switched method has the advantage that low current pulses are sensitive to temperature. Intermediate current levels, which may be used in a high dissipation pulse, have small temperature coefficients.

A technique of measuring thermal impedance was developed, which is similar to the switched method outlined above. However, the TSP is not characterised but used only to restore the channel temperature to a previous value. The procedure is described with reference to Figure 2.3. Two pulses may be applied repetitively to the gate, with a low duty cycle. The first pulse causes a large drain current to flow, while the second is shorter and results in a small current. If the drain voltages are similar in both cases, the heat dissipation will correspond to the current levels. Pulse 1 heats the MOSFET channel, the temperature of which is measured by pulse 2. Beginning with only pulse 2 applied, the heatsink temperature is raised to T_{SINKa} (Figure 2.3a). The two pulses are then applied consecutively (Figure 2.3b). Due to its temperature coefficient and the channel heating caused by pulse 1, the pulse 2 current increases. In Figure 2.3c, the heatsink temperature is lowered to

T_{SINKc} so that the initial pulse 2 current returns to its previous value. This implies that the channel temperature at the end of pulse 1 in Figure 2.3c is equal to the heatsink temperature T_{SINKa} in Figure 2.3a. The difference between T_{SINKa} and T_{SINKc} gives the rise in channel temperature due to pulse 1. The thermal impedance Z_{thJC} is calculated from the ratio of this temperature rise to the pulse 1 dissipation.

Several practical steps must be taken to enhance the accuracy of this method. Firstly, the pulse 1 dissipation should result in a temperature rise of roughly 3 °C. This temperature variation is easily measured but does not cause a significant change in dissipation during pulse 1. Furthermore, the pulse 1 current can be chosen to have a small temperature coefficient. Secondly, large errors can result from thermal gradients between the device channel and external temperature sensor. To alleviate this problem, the entire device should be heated to well above the required temperature and then allowed to cool slowly. Also, the temperature sensor should be mounted so as to be in thermal contact with the MOSFET flange and not the heatsink. The procedure in Figure 2.3 is chosen, since the heatsink temperature is raised only once, beyond T_{SINKa}. The values of pulse 2 current and heatsink temperature are observed as the device cools. An alternative method is to begin with both pulses applied and raise the heatsink temperature after pulse 1 is removed. This, however, requires two separate applications of heat.

The measurement technique for thermal impedance in Figure 2.3 can be extended to include thermal resistance, by increasing the duty cycle of the high dissipation pulse to near unity. This requires having long pulse 1 durations and a small delay between the end of pulse 2 and the beginning of pulse 1. To obtain a high duty cycle with a finite pulse 2 length, a low repetition rate of several times a second is required.

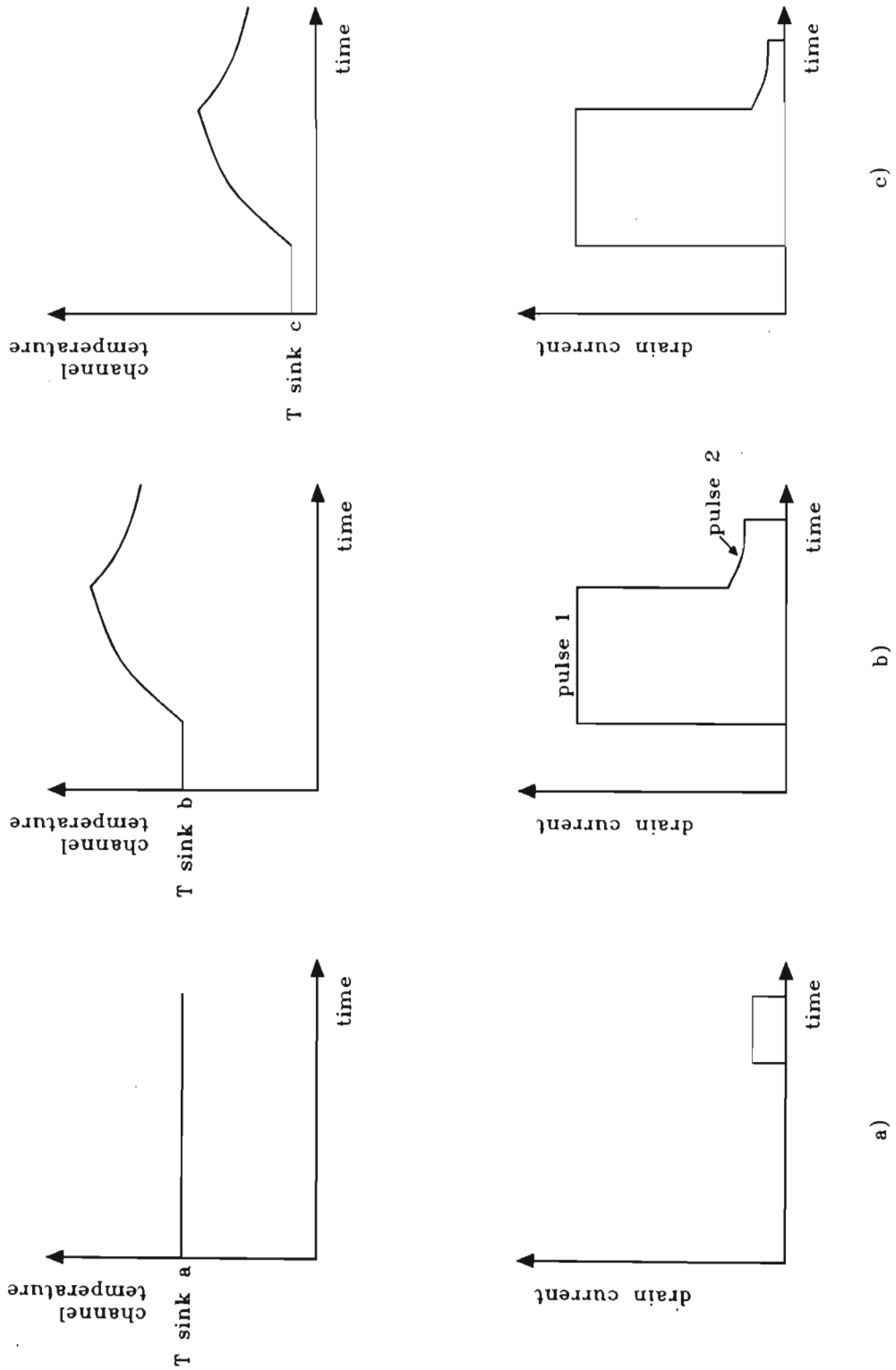


Figure 2.3 Measurement of MOSFET thermal impedance

A circuit was designed to measure a MOSFET's thermal impedance (Figure 2.4), briefly explained as follows. An oscillator triggers a monostable, giving pulse 1. The falling edge of pulse 1 triggers a second monostable, so that pulse 2 follows immediately. The outputs of the two monostables are summed together and applied to the MOSFET gate. To prevent instability, very high or low source impedances should not be used. Three oscilloscope measurements are required, as indicated in Figure 2.4. These are the pulse 1 current I_{D1}, the pulse 1 drain voltage V_{D1} and the pulse 2 current I_{D2}. The current during pulse 1 is measured by the voltage across three parallel 10 Ω resistors. It should be noted that a better arrangement would be to connect the 10 Ω resistors on the supply side of the diode string. For the given circuit, the oscilloscope and circuit grounds shift to different potentials during pulse 1. Although undesirable, this does not affect the measurement. The string of five fast-recovery diodes limits the potential across the 150 Ω resistor during pulse 1. The pulse 2 current is set so as to drop approximately 0.5 V across the 150 Ω resistor. Thus, during pulse 2 the potential across the Schottky diodes (IN518) is near to zero. These diodes limit the oscilloscope voltage during pulse 1, allowing I_{D2} to be observed on a sensitive instrument range. Drain current is taken from a regulated supply, with a nominal voltage of 24.1 V. The second supply of approximately 23.6 V is adjusted so that the oscilloscope reading I_{D2} is zero for pulse 2 in Figure 2.3a. Both supplies have a number of large capacitors, which provide a low impedance source. It is important that these supply voltages do not shift appreciably during the pulses, since this cannot be distinguished from the thermal effects being observed. An LM334 IC serves as a temperature sensor. Besides indicating the absolute temperature, a relative voltage output allows a DVM to be used on a sensitive range, giving an accurate indication of small temperature changes.

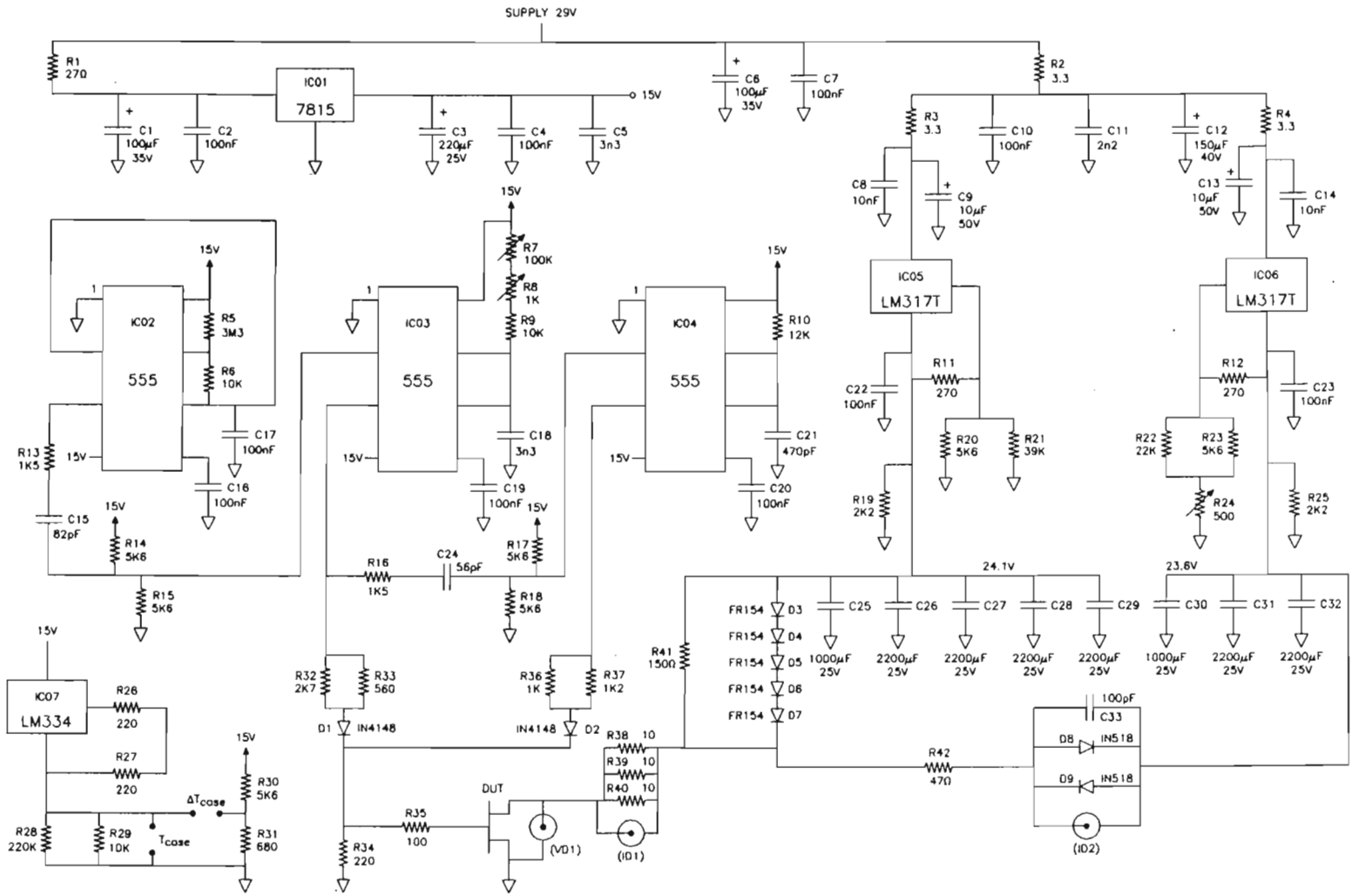


Figure 2.4 Circuit to measure thermal impedance of MOSFETs

Using the described circuit and measurement technique, the thermal characteristics of several devices were measured. These include an IRF520, which is an 8 A switching MOSFET, and an MRF136 RF power MOSFET. In Table 2.2 the measured thermal impedance of an IRF520 MOSFET is compared to data sheet information at a number of different pulse lengths. The measurement temperature is approximately 31 °C. The two sets of values correspond reasonably well and show clearly the increase of thermal impedance with pulse duration. A better correlation should not be expected since the thermal characteristics of semiconductor devices are poorly controlled.

Table 2.2 Thermal impedance versus pulse duration for an IRF520 MOSFET: Data sheet and measured values

Pulse duration (μs)	20	50	100	200	500	2000
Z_{thJC} (°C/W) Datasheet	0.075	0.11	0.15	0.19	0.29	0.64
Z_{thJC} (°C/W) Measured	0.036	0.09	0.12	0.22	0.30	0.70

The measured values of thermal impedance Z_{thJC} and resistance Θ_{JC} are given for an MRF136 at several device temperatures in Table 2.3. As expected from section 2.1.1, both parameters increase with temperature. The thermal impedance is measured for a pulse duration of 100μs.

Table 2.3 Measured thermal impedance (100 μs pulse) and thermal resistance versus temperature for an MRF136

Temperature (°C)	27	55	75	Temperature (°C)	37	75
Z_{thJC} (°C/W)	0.83	0.94	1.07	Θ_{JC} (°C/W)	3.1	3.4

The calculation of thermal impedance is illustrated for the MRF136 at a temperature of 55 °C. Firstly, the relative temperature sensor voltage, measured by a DVM, was 51.0 mV for a heatsink temperature of 55 °C. With the heatsink cooled to restore the low-dissipation pulse current to its previous value, this voltage changed to 37.1 mV. The temperature sensor coefficient is 5 mV / °C, which implies a temperature change of 2.78 °C. Secondly, during the high dissipation pulse, the drain voltage was measured to be 19 V and the current 0.156 A, representing a dissipation of 2.96 W. The temperature change of 2.78 °C divided by the dissipation of 2.96 W gives the thermal impedance of 0.94 °C/W.

2.3 Cold S parameters

The cold S parameters are measured using the test fixture shown in Figure 2.5. This comprises three sections of fibre-glass printed circuit board (PCB) which are bolted to underlying aluminium beams. The sections can thus be separated for calibration, or joined for the measurements, as shown. The PCB dielectric is 1.54 mm thick, with a dielectric constant of 4.39. The lower side of the PCB is copper-clad, so that the sections can be soldered together to form a continuous groundplane. Microstriplines are etched on the upper surface, with characteristic impedances of about 30 Ω under the gate and drain leads, tapering down to 50 Ω lines. Chip capacitors provide DC isolation between the microstriplines and SMA connectors. Both source leads are connected to the groundplane by wide straps. The device is inserted through cutouts underneath the source leads and rotated 45 ° into position. This technique avoids cutting away the PCB underneath the gate and drain leads, thus enhancing the accuracy of the de-embedding process. The MOSFET flange is bolted to an aluminium block, which allows for a heat sensor just below the flange and for resistor heaters at its base.

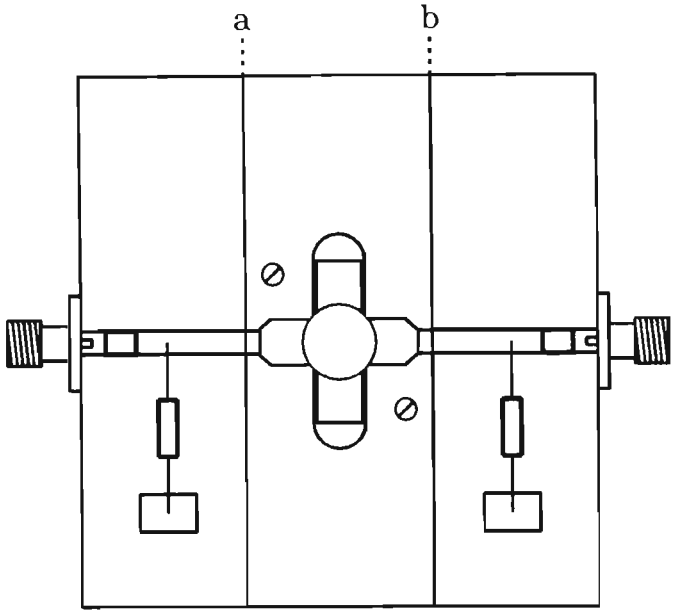


Figure 2.5 S parameter test fixture

The MOSFET's bias circuit is shown in Figure 2.6. The gate is grounded with a resistor, while the drain is biased through an RC network. This prevents rapid drain voltage transients, which could couple through the MOSFET gate-drain capacitance, turning the device on and resulting in RF oscillations. Since a drain leakage current of up to 2 mA may flow, the drain voltage should not be assumed to be equal to that of the supply.

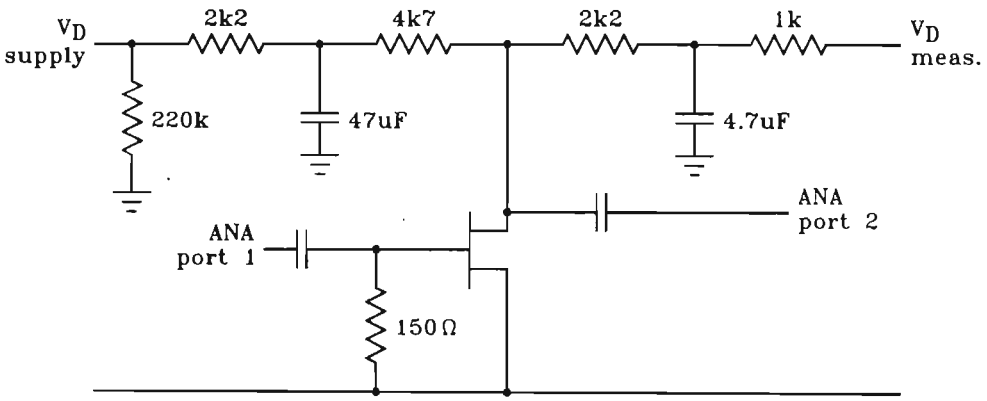


Figure 2.6 Cold S parameter bias network

A full 2-port ANA calibration is performed, with the reference planes a and b shown in Figure 2.5. The effects of the biasing components, DC blocking capacitors, 50 Ω microstriplines and SMA connectors are thus calibrated out of the measurement. The 30 Ω microstriplines, however, are included in the measurement and must be accounted for in a de-embedding process. The calibration requires short, open and load standards at each reference plane, as well as a through connection. For the short condition, a brass strap is soldered from the end of the microstripline to the groundplane. The open is obtained by leaving the end of the microstripline free. A load standard is constructed using a 50 Ω microstripline/SMA assembly, similar to an outer section of the test fixture. A verified 50 Ω SMA standard is placed on the SMA connector. For the calibration, this assembly is joined to the outer PCB section, soldering both the groundplanes and microstriplines together. The two outer sections are similarly joined for the through connection. Sufficient time should be allowed for soldered items to cool before measuring the standards. The described calibration procedure has been used successfully at frequencies up to 700 MHz.

The S parameter measurements are taken with the heatsink maintained at the required temperature, for a number of drain voltages. A PC controls the network analyser via an HPIB card. At each drain voltage, the measurement frequency is swept and the data points read into the PC. A typical frequency range is from 10 MHz to 700 MHz with 8 different drain voltages. Measurements for each drain voltage are saved to separate ASCII files. This data is later condensed automatically into a single file suitable for the model extraction program.

Chapter 3

Extraction of MOSFET model parameters

The model which is proposed in section 1.3 includes a number of parameters which must be identified from the measurements described in chapter 2. These parameters consist of elements in the equivalent circuit, both linear and nonlinear, and a controlled current source, which is a nonlinear function of the internal gate and drain voltages. The equivalent circuit is fitted to sets of cold S parameters which are measured at a number of drain voltages. In a separate procedure, an equation describing the drain current characteristics is fitted to measured data. The accuracy of the resulting MOSFET model is evaluated using high power measurements of a 15 W device in a well characterised test fixture.

3.1 S parameter fitting procedure

By fitting the linearised device model to S parameters measured at different bias points, the values of the linear elements may be determined, as well as those of the nonlinear capacitors at each bias point. Since the S parameter measurements include the effects of short lengths of microstripline on either side of the MOSFET, a de-embedding process must be performed. A program is written to perform the described optimisation procedures.

3.1.1 Method

The parameters of an equivalent circuit model may be found by fitting the model to measured S parameters, using an optimisation program. The difference between the modelled and measured S parameters is indicated by a single number, the objective function. The goal of the optimisation routine is thus to find out a set of model variables for which the objective function is minimised. The extraction of a large-signal model requires a number of sets of S parameters, each measured at a different bias point. A separate optimisation is usually employed for each set of S parameters [Willing *et al*, 1978 and Bunting, 1989]. The expected result is that linear elements

will have similar values in each optimisation and that the values of the nonlinear elements will be identified for each bias condition. An equation is then fitted to the bias-dependent values to describe the nonlinear elements.

An important problem is that of model consistency and uniqueness, which is discussed by Curtice [1988] and Bandler [1988]. For small differences in the objective function, some elements may have widely different and even non-physical values. This often leads to the anomaly of the extracted values of package elements having different optimal values for each bias point. The goal of a single correct solution distinguishes modelling from circuit design or curve fitting problems, where any good solution is acceptable.

This inconsistency has several causes. Firstly, measurement errors obscure the true response of a physical device. Secondly, the model may be too simplistic to describe the device adequately. Thirdly, there may be too many variables to be identified uniquely from the available measurements. The use of a model of appropriate complexity and the determination of elements, such as parasitics, by direct methods will alleviate this problem. Additionally, the optimisation procedure has an important effect.

Kondoh [1986] describes a procedure where selected elements are optimised to fit only one S parameter over some portion of the frequency range. For example, the drain parasitic inductance is optimised using only S_{22} over the upper half of the frequency band. The elements are divided amongst eight such steps in each iteration. The order of the eight steps is, however, important in ensuring convergence, and may depend on the model being used.

A method was developed whereby the model is fitted to the sets of S parameters simultaneously, corresponding to the multi-circuit modelling of Bandler [1988]. The linear elements are optimised, but are constrained to have the same values at all the bias points, while the nonlinear capacitors have different optimal values for each bias condition. A single least p_{th} objective function is formulated by comparing the

measured and calculated S parameters at the frequencies in all the bias points. The specification that the linear parasitic elements have the same values at all bias points can be seen as additional information for the optimisation process, thus enhancing the consistency and uniqueness of the model.

Besides the improvement in the derived model, the simultaneous fitting procedure offers several practical advantages. Firstly, only one optimisation is performed, instead of having one optimisation per set of bias-dependent S parameters. Secondly, the expressions which describe the nonlinear capacitors can be obtained automatically during the optimisation. This is achieved by optimising the coefficients of the expressions, rather than the discrete bias-dependent element values. For example, the nonlinear capacitors can be described by **(3.1)** using only 3 variables per capacitor, as opposed to perhaps eight variables giving the capacitor value at each bias point. This also eliminates the necessity to fit an expression to the bias-dependent values, which would result in additional modelling errors.

The voltage-dependent capacitance of C_{DG} and C_{DS} in Figure 1.6 is similar to that of a reverse-biased junction, and may be approximated as:

$$\begin{aligned} C &= a_0 / (1 + a_1 V)^{a2} && \text{for } V \geq 0 \\ C &= a_0 && \text{for } V < 0 \end{aligned} \qquad \textbf{(3.1)}$$

3.1.2 De-embedding and S parameter calculations

Referring to Figure 2.5, it is seen that, due to the calibration planes being defined at a and b, the S parameter measurements include short lengths of microstripline on either side of the MOSFET. It is not necessary for the optimisation program to include the effects of these in every calculation of the objective function. Instead, a more efficient method is to de-embed the MOSFET S parameters from the measurements once, at the beginning of the optimisation. This translates the measurement planes up to the edges of the MOSFET package.

The de-embedding process is accomplished using T parameters. These have the useful property that the parameters of a group of cascaded networks are equal to the product of the individual network parameters. The de-embedding of the MOSFET parameters from the measured values is given in equation **(3.3)**, with reference to Figure 3.1. The microstriplines between the MOSFET and the calibration planes a and b in Figure 2.5 consist of two sections with different widths, which are separated by a taper. A CAD program (LIBRA) is used to calculate the S parameters of these microstripline structures. The conversion between S and T small-signal parameters can be obtained from Abrie [1985].

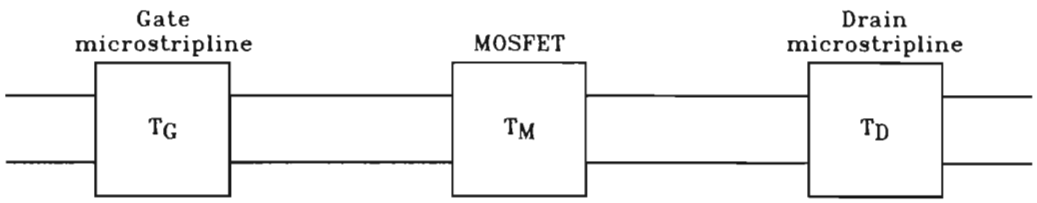


Figure 3.1 De-embedding of MOSFET from measurements using T parameters

$$T_T = T_G\, T_M\, T_D \qquad \textbf{(3.2)}$$

$$T_M = T_G^{-1}\, T_T\, T_D^{-1} \qquad \textbf{(3.3)}$$

During the optimisation, the S parameters of the model are required. These can be obtained by calculating the model Y parameters and converting these to S parameters. It is more efficient to calculate the S parameters directly by nodal analysis. The equations, **(3.10)** and **(3.11)**, are derived for S_{11} and S_{21}, with reference to Figure 3.2. The parameters S_{22} and S_{12} are given implicitly.

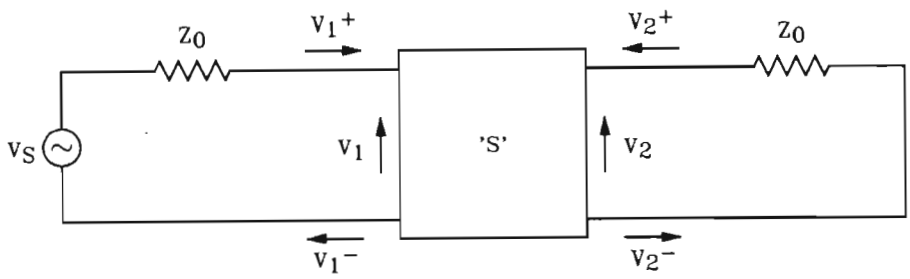


Figure 3.2 Circuit definitions for direct calculation of S parameters

The S parameters of the network in Figure 3.2 are defined as:

$$b_1 = S_{11}\, a_1 + S_{12}\, a_2 \qquad \textbf{(3.4)}$$

$$b_2 = S_{21}\, a_1 + S_{22}\, a_2 \qquad \textbf{(3.5)}$$

with

$$a_n = V_n^+ / \sqrt{Z_0} \qquad \textbf{(3.6)}$$

$$b_n = V_n^- / \sqrt{Z_0} \qquad \textbf{(3.7)}$$

where V_n^+ = incident wave on n_{th} port

V_n^- = reflected wave from n_{th} port

An important identity for the derivation is:

$$V_n = V_n^+ + V_n^- \qquad \textbf{(3.8)}$$

The incident wave V_1^+ in Figure 3.2 can be determined from **(3.8)** if port 1 of the network has an impedance of Z_0, for which $V_1^- = 0$ and $V_1 = V_S/2$. This gives:

$$V_1^+ = V_S / 2 \qquad \textbf{(3.9)}$$

The parameters S_{11} and S_{21} can be calculated as:

$$S_{11} = \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+} = \frac{V_1 - V_1^+}{V_1^+} = \frac{V_1 - V_s/2}{V_s/2} = \frac{2V_1 - V_s}{V_s} \qquad (3.10)$$

$$S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+} = \frac{V_2}{V_1^+} = \frac{V_2}{V_s/2} = \frac{2V_2}{V_S} \qquad (3.11)$$

Equations **(3.10)** and **(3.11)** begin from **(3.4)** and **(3.5)** respectively, with $a_2 = 0$, since port 2 in Figure 3.2 is terminated in an impedance Z_0, which gives $V_2^+ = 0$. The final expressions are obtained using **(3.6)** - **(3.9)**.

By replacing the voltage source in Figure 3.2 with its Norton equivalent, ie. a current source and parallel resistance, the required voltages can be calculated using nodal analysis. This results in matrices of the form:

$$[Y]\ [V] = [I] \qquad (3.12)$$

There are several methods of solving these equations. Cramer's rule, which uses determinants, is inefficient for large matrices. Gauss row reduction and LU factorisation are suitable methods. The LU factorisation method offers the advantage that the factorisation, which represents a substantial portion of the computational effort, is performed only once in order to calculate all four S parameters. A Gauss row-reduction subroutine must be called twice, since the parameters S_{11}, S_{21} and S_{22}, S_{12} are calculated with the source on port 1 and port 2 respectively. The LU factorisation method is therefore used in the optimisation program to be described.

3.1.3 Objective function and search method

The objective function is a single number which expresses the difference between the measured and modelled S parameters. In the S parameter fitting procedure, there are four S parameters, measured over a range of frequencies, at a number of bias conditions. Each of these individual vectors must be included in the objective function. Since a perfect fit of all S parameters is not obtained, the objective function must be chosen to provide an acceptable distribution of errors. An extreme example is the minimax objective function, which considers only the worst error. This is undesirable if, for example, the modelled results contain a few bad points, perhaps near to the limits of the model's validity. In such a case, the general fit of the model will be severely degraded in an attempt to improve the few large errors. The least p_{th} objective function in **(3.13)** allows a good compromise between the average and maximum errors. A value of p is chosen according to the desired emphasis. For example, p = 1 will yield a good overall fit, while large values of p tend towards a minimax solution. The well known least-squares objective function corresponds to p = 2.

$$U = 100 \left(\frac{1}{N_{FREQ} * N_{BIAS} * 4} \sum_{BIAS} \sum_{FREQ} \sum_{i=1}^{2} \sum_{j=1}^{2} \left[E_{Sij}^{p} \right] \right)^{1/p} \qquad (3.13)$$

where E_{Sij} = individual vector error

Several papers [Kumar and Pandharipande, 1988 and Fusco, 1991] have described objective functions which consider the magnitude and phase of S parameter vectors separately. For example, an error of 1 dB may be assigned the same weighting as an error of 1 °. There is little justification for any particular choice of weighting between magnitude and phase. A more natural method of comparing vectors, which avoids this problem, is shown in Figure 3.3. The error is defined to be a relative quantity in **(3.15)**, again avoiding the necessity for arbitrary weightings if absolute

errors are used for S parameters with greatly different magnitudes. This is the case, for example, with cold MOSFET S parameters, where S_{21} and S_{12} are much smaller than S_{11} and S_{22}.

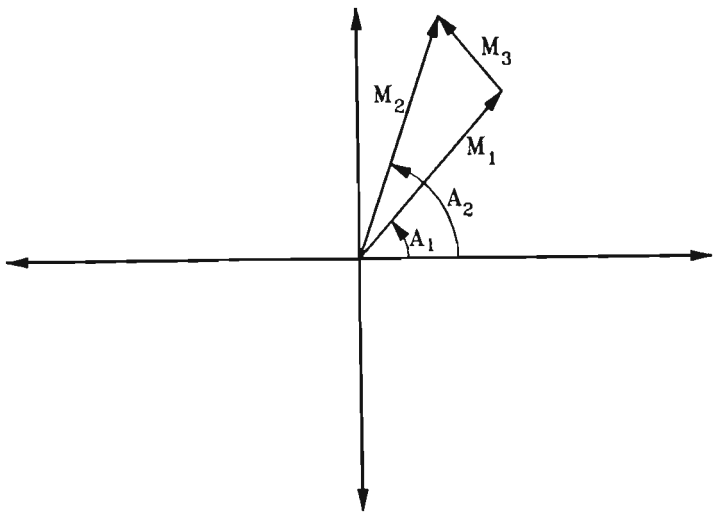


Figure 3.3 Definition of vectors for the objective function

$$M_3 = \sqrt{\left[M_1^2 + M_2^2 - 2 M_1 M_2 \cos (A_2 - A_1) \right]} \qquad (3.14)$$

$$E_{Sij} = M_3 / M_1 \qquad (3.15)$$

where $M_1 \angle A_1$ *is the goal vector*

$M_2 \angle A_2$ *is the vector being evaluated*

The search method is an algorithm within the optimising program which provides new sets of model variables for evaluation. A simple strategy is to select new sets of variables randomly, retaining only the set giving the lowest objective function. Gradient search methods locate minima far more quickly. The method of steepest-

descent searches in the direction of the negative of the objective function gradient. More sophisticated gradient methods use information from previous iterations to improve the speed of optimisation. The conjugate-direction method stores this information in a single scalar number, while the variable metric methods use an array. Since the optimisation process takes relatively little time, the steepest-descent method proved satisfactory.

A disadvantage of gradient-based methods is that a local minimum may be found instead of the global minimum. This problem can be avoided by providing a starting point which is sufficiently close to the optimum solution. Although initial values for a device model can be determined by direct measurements and calculations, a random search is more likely to find a solution near to the global minimum. The density of local minima increases with the number of optimisation variables. For the MOSFET model proposed in chapter 1, with 3 variables per nonlinear capacitor, there is a total of 15 variables. This is significantly more than for GaAsFET models where the package elements are determined prior to the optimisation. It is therefore advocated that the S parameter fitting procedure for the MOSFET model begin with a random search, to locate a solution near to the global minimum, followed by a much faster gradient optimisation to obtain the final solution.

Random optimisation methods are particularly slow if the model has many variables. A reason for this is that, in a trial, at least one of the variables is likely to be set to a value which precludes finding an improved solution. Firstly, placing tighter limits on the variables will alleviate this problem. However, if suitable bounds are not known precisely, the global minimum may be excluded. Secondly, noting that improvements are most likely to be found near to the best known solution, the probability of large variable changes can be decreased. For example, random numbers with a Gaussian probability density can be obtained from a generator which has a flat probability density [Adby, 1980].

3.1.4 Optimisation program

A program was written to fit the model of Figure 1.6 to measured S parameters, implementing the techniques discussed in this chapter. Due to the large amount of data that is manipulated, the program information is stored in files. The input data file specifies the bias points and frequencies, and gives the measured S parameters, as well as those calculated for the test fixture microstriplines. The minimum, maximum and start values of the variables are read in from an existing results file, together with the previously used optimisation variables, such as p for the least p_{th} objective function. The de-embedding process is performed once, at the start of the program. During the optimisation, the user may choose a random or gradient method and save the intermediate results to a file. The screen display is regularly updated, giving information such as the objective function, average and maximum errors, and the current values of model variables. At the conclusion of the optimisation, the results are saved to a file. This includes a list of all measured and calculated S parameters, with their individual errors. The calculated values of the nonlinear capacitors at each bias point are also given.

3.1.5 Results

The following optimisation results are obtained by fitting the model of Figure 1.6 to data measured for an MRF136 MOSFET. The S parameters are measured with V_{GS} = 0, at eight different drain voltages from 0 V to 30 V. At each bias point, eight frequencies from 10 MHz to 700 MHz are considered, with approximately the same relative spacing between adjacent frequencies.

In the example given, there are four S parameters, eight frequencies and eight bias points, so that 256 vectors are considered in the objective function. A value of p = 4 is used instead of the least-squares formulation, since this significantly reduces the worst errors, while only slightly degrading the average of the relative errors. The final value of the objective function, as well as the average and maximum relative

vector errors, are shown in Table 3.1. The corresponding parameter values for the model of Figure 1.6 are given in Table 3.2.

Table 3.1 Objective function and relative vector errors for S parameter fitting procedure

U	Average [E_{Sij}]	Maximum [E_{Sij}]
3.65	2.14 %	8.27 %

Table 3.2 Final model parameter values

C_{GP}(pF)	L_{GP}(nH)	R_{GP}(Ω)	C_{DP}(pF)	L_{DP}(nH)	R_{DP}(Ω)	L_{SP}(nH)	R_{SP}(Ω)
0.54	3.04	0.60	2.37	1.22	0.35	0.92	0.10
C_{GS}(pF)	C_{DG0}(pF)	C_{DG1}	C_{DG2}	C_{DS0}(pF)	C_{DS1}	C_{DS2}	
16.23	50.44	2.570	0.583	94.65	2.067	0.391	

From equation **(3.1)**, the bias-dependent values of C_{DG} and C_{DS}, as a function of the voltage across themselves, are given in Table 3.3.

Table 3.3 Bias-dependent values of C_{DG}, C_{DS} for the extracted model

V_{cap} (V)	0	1	2	3	5	10	15	30
C_{DG} (pF)	50.44	25.61	19.19	15.93	12.44	8.773	7.120	4.950
C_{DS} (pF)	94.65	61.09	49.95	43.76	36.65	28.46	24.43	18.75

Referring to the MRF136 package construction in Figure 3.4, a number of features can be noted, which correlate well with the extracted package element values in Table 3.2. Due to its reduced overlap with the source, the gate package capacitance can be expected to be much smaller than that of the drain. This is seen in the extracted values of 0.54 pF and 2.37 pF respectively. Since the chip is mounted on the drain tab, the drain package inductance should be small (1.22 nH). The inductance of the bond wires, which have a high length to diameter ratio, is approximately 1 nH/mm. Due to the package leads, the total gate and source inductances are expected to be slightly greater than that of the bond wires. Accordingly, the extracted values of gate inductance (3.04 nH) and source inductance (0.92 nH) are consistent with the bond wire lengths of about 2.5 mm and 0.8 mm respectively.

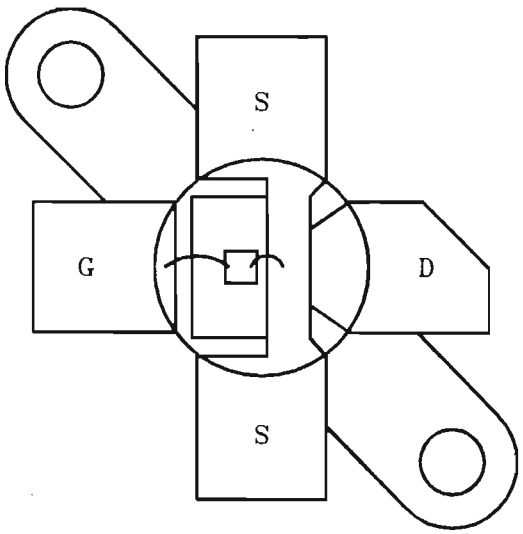


Figure 3.4 MRF136 package construction

An average fit between the modelled and measured S parameters of 2.14 % is achieved over a wide range of frequency and bias. This suggests that the MOSFET model of Figure 1.6, although relatively simple, represents the important characteristics of the device adequately. The method of fitting the model to a number of sets of bias-dependent S parameters simultaneously, using random and gradient techniques, results in physically consistent package element values.

3.2 Nonlinear voltage-controlled current source

In the model of Figure 1.6, the drain current must be expressed as a function of the internal voltages V_{CGS} and V_{CDS}. A suitable equation was developed, and a program written to curve fit this equation to measured data.

3.2.1 Drain current equation

As discussed in chapter 1, the theoretical square-law drain current relationship used for low power MOSFETs is not applicable to high power devices. Additionally, a number of approximations are made in the MOSFET model of Figure 1.6. Therefore, the drain current equation must be considered as part of a curve fitting problem.

Equation **(3.18)** was developed to describe the nonlinear voltage-controlled current source in the model of Figure 1.6. The drain current is given as a function of the internal voltages V_{CGS} and V_{CDS}. Since the measured DC drain current flows through the resistances R_{DP} and R_{SP}, these internal voltages are lower than the externally measured values, as calculated in **(3.16)** and **(3.17)**.

$$V_{CGS} = V_{GS} - I_D * R_{SP} \qquad \textbf{(3.16)}$$

$$V_{CDS} = V_{DS} - I_D * (R_{SP} + R_{DP}) \qquad \textbf{(3.17)}$$

where V_{GS}, V_{DS} and I_D are measured values

R_{SP} and R_{DP} are obtained from the S parameter fitting procedure

$$V_1 = V_{CGS} - K_5 \quad , \quad V_2 = V_{CDS}$$

$$I_D = \left[K_0 + K_1 V_1 + K_2 V_1^2 + K_3 V_1^3 + K_4 V_1^4\right]\left[1 - 2.72^{-[V_2/(K_6 + K_7 V_1)]^{(K_8 + K_9 V_1)}}\right] + V_2(K_{10} + K_{11} V_1)$$

$$I_D = 0 \qquad for \quad V_1 \; or \; V_2 < 0 \tag{3.18}$$

Referring to Figure 3.5 (section 3.2.3), it is seen that a number of features in the drain current characteristics are described by **(3.18)**. The constant K_5 represents the gate threshold voltage of the MOSFET, below which zero drain current flows. The terms $K_0 + K_1V_1 + K_2V_1^2 + \ldots$ describe the increase of drain current with gate voltage. The MOSFET drain current curve for a constant V_{GS} is often represented by a tanh function. This gives the initial steep slope of I_{DS} versus V_{DS} followed by a levelling off in I_D for higher drain voltages. In **(3.18)**, this is given by terms of the form 1-2.72^(-X_1^X_2). The X_1 exponent, with K_6 and K_7, defines the knee in the curves, which occurs at higher drain voltages for larger V_{GS} curves. The X_2 exponent, with K_8 and K_9, allows adjustment of the initial slope of the I_D curves, without affecting the position of the knee. If the curves for different gate voltages are scaled to have the same final I_D value, it is found that the high V_{GS} curves have lower initial slopes. The term $V_2(K_{10} + K_{11}V_1)$ provides a slope in the curves for drain voltages above the knee. The slope is greater for larger gate voltages.

3.2.2 Curve fitting program

A program was written to fit equation **(3.18)** to measured drain current characteristics. This is similar in many respects to the S parameter fitting program, for example, with the use of input and output data files and the screen display. The objective function is important in determining the quality of fit in the different regions of the drain current characteristics. Firstly, a value of p in the least p_{th} objective function can be chosen to give an acceptable balance between the large errors and the general fit. Secondly, the objective function can evaluate calculated values either in

a relative or absolute sense. Since a wide range of drain currents, from approximately 15 mA to several amps, is considered, an objective function with absolute errors will effectively neglect the low current points. The use of relative errors will correct this. However, the high current region is more important for large-signal operation than the low current levels and should therefore be favoured. The objective function in equation **(3.21)** achieves this, using relative errors with a weighting factor for high current points.

$$W_i = 1 + ERFW * I_{DMi} \tag{3.19}$$

$$E_i = \frac{|I_{DMi} - I_{DCi}|}{I_{DMi}} \tag{3.20}$$

$$U = 100 \left(\frac{1}{N} \sum_{i}^{N} W_i E_i^{\,p} \right)^{1/p} \tag{3.21}$$

where I_{DMi} = measured drain current for i_{th} bias point
I_{DCi} = calculated drain current for i_{th} bias point
ERFW = coefficient for weighting factor

3.2.3 Results

To allow a thorough evaluation of the curve fitting results, the distribution of errors is compared using the number CTx. This is defined as the percentage of points having relative errors of less than x percent.

The effect of different values of p is illustrated in Table 3.4. These results are obtained for data which comprises 347 measured points, with currents up to 2.4 A and voltages up to 45 V. Due to the presence of large errors, the best results are obtained with low values of p. It is important to note that, with p = 1, the few errors which exceed 25% are all points in the corner of the drain current

characteristics, with voltages and currents of less than 2 V and 50 mA respectively. These points do not fall within the locus of normal RF operation.

Table 3.4 Curve fitting results for different values of p (ERFW = 0.0)

p	U	Avg.[E_i] (%)	Max.[E_i] (%)	CT_5 (%)	CT_{10} (%)	CT_{15} (%)	CT_{20} (%)	CT_{25} (%)
1	3.18	3.18	59.5	81.9	96.3	98.6	98.9	98.9
4	8.95	4.79	28.8	62.3	92.2	97.4	99.4	99.7
12	14.3	7.5	21.2	34.3	68.0	95.1	99.4	100.0

A complete set of results is now presented. The drain current data comprises 347 points, measured for an MRF136 MOSFET. Equation **(3.18)**, which has 12 coefficients, is fitted to the measurements using the objective function of **(3.21)**, with p = 2 and ERFW = 5. The values of R_{SP} and R_{DP} are taken to be 0.087 Ω and 0.583 Ω respectively. Table 3.5 gives the coefficients for the drain current equation. The resulting fit between the equation and measurements is given in Figure 3.5 and Table 3.6.

Table 3.5 Optimised coefficients for drain current equation

K_0	K_1	K_2	K_3	K_4	K_5
$7.35*10^{-3}$	$5.66*10^{-3}$	$2.09*10^{-1}$	$-4.00*10^{-2}$	$2.9*10^{-3}$	3.553
K_6	K_7	K_8	K_9	K_{10}	K_{11}
$7.44*10^{-2}$	$4.00*10^{-1}$	$9.47*10^{-1}$	$7.77*10^{-2}$	$2.50*10^{-4}$	$1.20*10^{-3}$

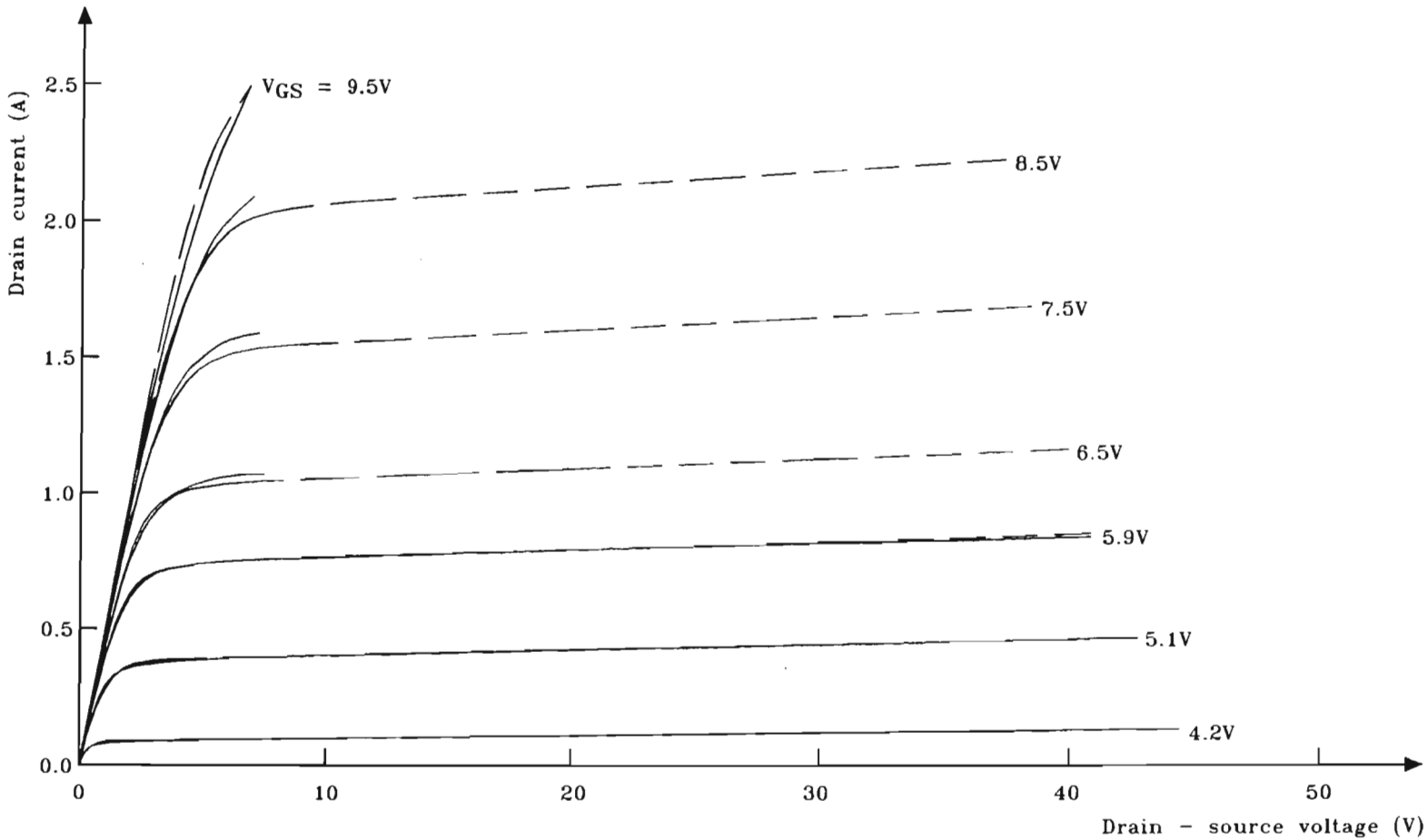


Figure 3.5 Drain current characteristics (p = 2, ERFW = 5) ——— (measured) - - - - (calculated)

Table 3.6 Curve fitting results for drain current equation (p = 2, ERFW = 5)

U	Avg.[E_i] (%)	Max.[E_i] (%)	CT_5 (%)	CT_{10} (%)	CT_{15} (%)	CT_{20} (%)	CT_{25} (%)
7.8	3.2	56.4	82.7	95.1	98.3	98.9	98.9

The drain current equation of **(3.18)** fits the measurements with an average error of 3.2 %. As a precaution against device failure, points with simultaneously high voltages and currents were not measured. However, in the important central region of the drain current characteristics, the fit is good at currents up to the maximum measured value of 1 A. The particularly large errors are within relatively unimportant regions.

3.3 Model verification

A model was extracted for an MRF136 MOSFET, using the S parameter and drain current fitting procedures which have been discussed. Predictions made using this MOSFET model in the harmonic balance program LIBRA are compared to large signal measurements of the device in a test fixture.

The measurements are made with the device mounted in the test fixture shown in Figure 2.5. A 27 Ω resistor biases the gate, and the drain is supplied through a 400 nH choke. DC blocking is provided by 3 nF plate ceramic capacitors. The test fixture is connected to a 50 Ω source and load. This circuit is analysed using a harmonic balance program. The biasing components are described by simple equivalent circuits and the microstriplines defined by their physical dimensions.

Tables 3.7 to 3.10 compare measured and predicted values of output power, drain supply current, harmonic levels and the input impedance seen into the SMA connector of the test fixture. The input and output powers are measured using a bolometer power meter. The input power stated is thus the available power of the source, while the output power is the total RF power delivered into a 50 Ω load, including the harmonics. The harmonic power levels in Table 3.9 are measured using a spectrum analyser, with an estimated error of up to 1.5 dB. The high power impedances in Table 3.10 are measured using the method described in section 5.1.3. The measured and calculated impedances are compared using the relative vector error defined in Figure 3.3 and equation **(3.15)**.

Table 3.7 Output power and drain supply current versus input power and frequency (Drain supply = 28 V I_{DQ} = 25 mA)

	50 MHz		100 MHz		200 MHz	
P_{in} (W)	0.185	0.566	0.408	1.095	1.015	2.233
P_{out} meas. (W)	4.875	9.750	4.977	9.954	4.060	7.106
P_{out} calc. (W)	4.058	9.100	4.290	8.740	4.290	7.766
Error	-16.8 %	-6.6 %	-13.8 %	-12.2 %	5.7 %	9.3%
ID_{DC} meas. (mA)	305	482	412	672	561	800
ID_{DC} calc. (mA)	274	475	379	625	584	860
Error	-10.1 %	-1.5 %	-8.0 %	-7.0%	4.1 %	7.5 %

Table 3.8 Output power and drain supply current versus gate bias voltage
(Drain supply = 28 V P_{in} = 1.99 W 100 MHz)

V_{GS} DC (V)	-0.4	0	1	2	3	4	4.5
P_{out} meas. (W)	5.87	6.57	8.26	9.95	11.45	12.94	13.44
P_{out} calc. (W)	4.85	5.47	7.08	8.82	10.69	12.64	13.63
Error	-17.5 %	-16.7 %	-14.3 %	-11.4 %	-6.7 %	-2.3 %	1.4 %
ID_{DC} meas. (mA)	393	430	527	625	714	806	853
ID_{DC} calc. (mA)	343	379	474	585	715	864	944
Error	-12.7 %	-12.0 %	-10.0 %	-6.3 %	0.1 %	7.1 %	10.6 %

Table 3.9 Output harmonic power versus input power
(Drain supply = 28 V I_{DQ} = 25 mA 100 MHz)
(Measured using spectrum analyser with error up to 1.5 dB)

P_{in}(dBm)	P_{out}(dBm)	100 MHz	200 MHz	300 MHz	400 MHz	500 MHz	600 MHz	700 MHz
23.0	meas.	35	13	9	-8	-6	-11	-
	calc.	33	12	8	-12	-6	-13	-20
26.2	meas.	38	-20	16	0	-1	-4	-18
	calc.	36	5	14	-1	-3	-6	-20
26.9	meas.	38	7	16	4	-4	-2	-18
	calc.	37	-6	15	1	-2	-4	-21
30.0	meas.	40	24	18	10	2	2	-1
	meas.	39	22	19	9	-5	3	-7

Table 3.10 Impedance into test fixture versus input power and frequency (Drain supply = 28 V I_{DQ} = 25 mA)

	50 MHz		100 MHz		200 MHz	
P_{in} (W)	0.23	0.79	0.49	1.45	0.54	1.30
P_{out} (W) meas.	5.3	10.6	5.4	10.7	2.7	5.4
Z meas. (Ω)	17.1-j8.57	15.6-j8.81	12.4-j3.59	10.3-j2.56	8.36+j3.19	7.35+j3.96
Z calc. (Ω)	19.1-j7.64	14.6-j6.74	13.8-j3.11	11.3-j1.85	9.10+j4.80	8.42+j5.55
Error	11.5 %	12.7 %	11.1 %	11.4 %	19.8 %	22.9 %

The average error for the complete set of results is 10 %, with most errors being less than 25 %. The large errors in the prediction of the second harmonic in Table 3.9 are the result of a sharp dip occurring in the response. This occurred at an input level of 26.2 dBm in the measurements and at 27 dBm in the predicted results.

There are a number of factors which result in the differences between the measurements and calculations. These include inaccuracies in the measurements, the test fixture component models and the MOSFET model. Except for the harmonic power values, the measurement errors are not expected to exceed a few percent. Similarly, the models used for the biasing components, decoupling capacitors and microstriplines have little effect on the overall result. It is believed that the errors can be attributed largely to the MOSFET model. Besides the inherent limitations of the modelling process, it should be noted that, firstly, the large signal measurements were made with the device temperature uncontrolled, between approximately 25 °C and 65 °C, while the model was intended for a channel temperature of 75 °C. Secondly, as a precaution, the measured drain current data did not include points having simultaneously high drain voltages and currents. The model's drain current equation will thus represent this region poorly.

Several improvements can be made to the model. The maximum error of 8 % in the S parameter fitting procedure suggests that the model topology is appropriate. However, a slightly more detailed representation of the intrinsic device would be of some benefit. The drain current equation offers greater scope for improvement, with approximately 20 % of all fitted points having an error greater than 5 %. Further accuracy could be gained through the careful selection of measurements for the model extraction, for example with the choice of drain voltages and frequencies in the cold S parameter measurements. Also, the density of measurements in the drain current characteristics could be chosen to reflect the relative importance of the different regions.

The large-signal measurements, which cover a wide range of operating conditions, demonstrate that the proposed MOSFET modelling procedure is useful for the design of RF power amplifiers. Although the model's accuracy is enhanced by the use of temperature-controlled drain current measurements, good results are obtained at greatly different temperatures. The accuracy of the model can be improved in several ways without fundamental changes to the proposed modelling procedure.

Chapter 4

Passive component and network models

A number of different types of passive components are found in RF power amplifiers, being used for biasing, impedance matching, stability enhancement and filtering. These components include resistors, inductors, capacitors, microstriplines and ferrite transformers. Physical components of this type can display characteristics which are far from the ideal, reflecting numerous phenomena of varying importance. A suitable level of model complexity must be chosen. The approach taken here is to use a simple model which includes only the most important effects. This reduces the time taken to extract model parameters and to analyse the complete amplifier circuit. Microstripline models are not discussed, since the standard models in CAD packages provide an accurate description using either physical or electrical parameters.

4.1 Resistors, inductors and capacitors

4.1.1 Model topologies

The dominant parasitic effect with resistors is series inductance, due to the length of the resistor body and its leads (Figure 4.1a). Inductors show parasitic parallel capacitance and series resistance which varies with the root of the frequency, due to the skin effect. The use of a ferrite core additionally results in hysteresis and eddy current losses, usually represented in a model as a parallel element (Figure 4.1b). Ferrite losses are a complex function of frequency and maximum flux density, often described by means of empirical curves [Abrie, 1985, p50]. Capacitors display series inductance and dielectric losses (Figure 4.1c). The component leads can contribute significantly to the total parasitic inductance, adding approximately 0.5 nH per mm of lead length [Abrie, 1985, p246].

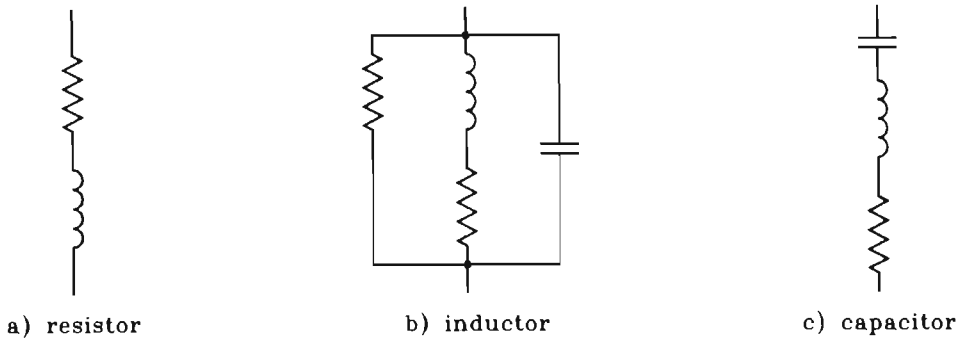


Figure 4.1 Detailed models for resistors, inductors and capacitors

The characteristics of resistors and air-cored inductors are relatively stable. However, the permeability of a ferrite core changes with temperature, while capacitor values can be sensitive to temperature and voltage. The dielectric losses of capacitors increase with temperature, which can lead to thermal runaway at high power levels [Abrie, 1985, p39].

The amplifiers described in chapter 6 are constructed with metal film resistors, air-cored inductors and plate ceramic capacitors. The models used to describe these components in the CAD package are shown in Figure 4.2.

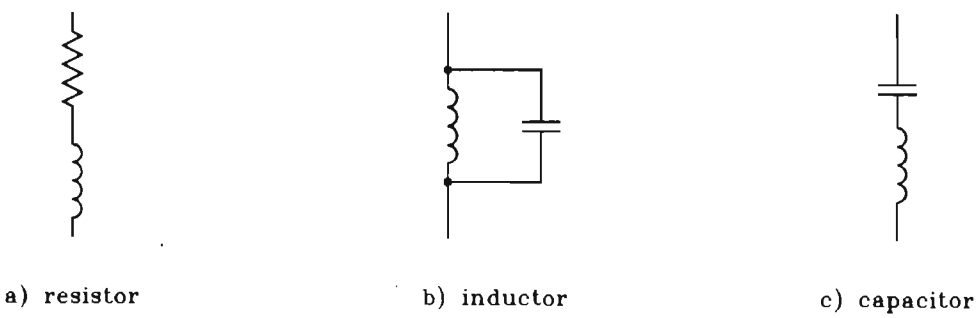


Figure 4.2 Models used for resistors, inductors and capacitors

The models in Figure 4.2 include only the dominant first-order effects. In most cases it is a good approximation to assume that air-cored inductors and capacitors are lossless. However, this would not be true for components used in high Q circuits, or with DC blocking capacitors, where the circuit impedance levels are lower than a few ohms. It is important to note that more detailed models incorporating AC loss effects may not work correctly at DC, which is often a requirement in large signal analysis. For example, if a drain bias inductor is modelled with series resistance to represent the skin effect losses in the copper wire, an unacceptably large DC voltage drop will occur.

4.1.2 Parameter extraction

Parameters must be chosen so that the impedance of the model closely approximates the values measured for a component. It is possible to determine analytically the resistor model parameters from an impedance measurement at one frequency, with two being required for the inductor and capacitor models. However, since the physical components display effects not represented in the model, it is better to consider a number of frequencies over a wide range. For power amplifier analysis, this should preferably include the fundamental and several harmonics. A convenient method is to fit the model to measured data using a least-squares optimisation routine.

The extracted parameters for a resistor are given in Table 4.1 and for an inductor and capacitor in Table 4.2. The models are fitted at three frequencies, comprising 118 MHz, 150 MHz and 175 MHz. For comparison, the impedances of the corresponding ideal components are given, showing the significant effect of the parasitics.

Table 4.1 Resistor impedance : measured and modelled

	resistor (27 Ω , 1/2 W , 2 % metal film)					
	meas.		model		ideal	
	-		(22.05 Ω + 5.92 nH)		(22.05 Ω)	
	Re [Z] (Ω)	Im [Z] (Ω)	Re [Z] (Ω)	Im [Z] (Ω)	Re [Z] (Ω)	Im [Z] (Ω)
118 MHz	22.00	4.40	22.05	4.39	22.05	0.00
150 MHz	22.05	5.58	22.05	5.58	22.05	0.00
175 MHz	22.05	6.54	22.05	6.51	22.05	0.00

Table 4.2 Inductor and capacitor impedances : measured and modelled

	Inductor (400 nH air-cored)			Capacitor (27 pF plate ceramic)		
	meas.	model	ideal	meas.	model	ideal
	-	(354.5nH //0.561pF)	(428.1nH)	-	(27.06pF +2.79nH)	(29pF)
	Im [Z] (Ω)	Im [Z] (Ω)	Im [Z] (Ω)	Im [Z] (Ω)	Im [Z] (Ω)	Im [Z] (Ω)
118 MHz	295.0	295.1	317.0	-47.75	-47.78	-46.51
150 MHz	406.0	405.8	403.5	-36.59	-36.58	-36.59
175 MHz	513.0	513.2	470.7	-30.53	-30.54	-31.36

The inductance of air-cored coils can be calculated using various equations [H.W. SAMS Eng. staff (ed), 1979, p184 and Plonus, 1978, p268]. The parasitic capacitance and Q factor is usually estimated using empirical curves or equations [Abrie, 1985, p42, 52]. However, the values thus obtained can be significantly in error. Apart from the inaccuracy of the estimation method, it is difficult to measure

precisely the dimensions of small handwound coils. Furthermore, the type of wire, which may be copper, tinplated or coated with one of several types of insulation, affects the inductor characteristics.

Calculated values should therefore only be used as an initial guide, with coil parameters being extracted from accurate measurements. A calibrated ANA is preferable to an impedance bridge, as the capacitance of the test fixture will often exceed that of a coil being measured. With coils having inductances of less than about 30 nH, it is important to include the lead inductance of approximately 0.5 nH per mm length. Table 4.3 gives an example of measured and calculated inductance values for an air-cored coil. The calculations are made using equation **(4.1)** [H.W. SAMS Eng. staff (ed), 1979, p184]. The large difference between calculated and measured values of inductance results from the difficulty in determining accurately the coil dimensions. In this case, the coil was misshapen from adjustments made to it in an amplifier matching network.

Table 4.3 Air-cored coil inductance : measured and calculated

Wire diameter (mm)	Turns	Former diameter (mm)	Total coil length (mm)	Total lead length (mm)	L (coil) (nH)	L (leads) (nH)	L (calc.) (nH)	L(meas.) (nH)
0.35	3	3.25	6.0	4	15.1	2	17.1	24.1

$$L = \frac{N^2 r^2}{229 r + 254 l} \qquad (4.1)$$

where L = coil inductance (μH)
N = number of turns
r = mean radius of coil (mm)
l = total coil length (mm)

4.2 Ferrite transformers

With LC matching networks, there is a tradeoff between the size of the impedance transformation and the frequency bandwidth obtained. Thus, for impedance transformation ratios larger than 10 times, it is difficult to achieve greater than an octave bandwidth. Transformers can be used over decade bandwidths with large impedance transformation ratios.

Broadband transformers can be classified into three different types. Firstly, a conventional magnetically coupled transformer, with two separate windings, is shown in Figure 4.3a. The second type, an autotransformer, uses a single tapped winding (Figure 4.3b). Finally, Figure 4.3c shows a transmission-line transformer. An autotransformer generally offers better performance than the magnetically coupled type, with the transmission-line type being best of the three. Requiring less turns in total than a transformer with two separate windings, an autotransformer has lower flux leakage, copper loss and parasitic capacitance. A transmission-line transformer has the advantage that the distributed capacitance and inductance of the winding is not a parasitic effect which degrades performance, but a necessary characteristic of the transmission line.

A typical autotransformer consists of several turns of enamelled copper wire wound onto a ferrite balun core. One end of the winding is grounded, with the other being the high impedance terminal. A low impedance connection is made at some point along the length of the winding. If the total number of turns is N_1 and there are N_2 turns across the low impedance port, then ideally the voltage transformation ratio will be N_1/N_2 : 1. This corresponds to an impedance transformation ratio of $(N_1/N_2)^2$: 1.

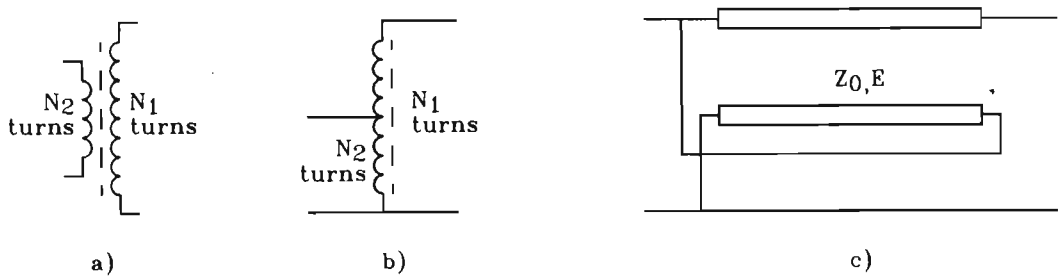


Figure 4.3 Three transformer types :

a) Conventional magnetically coupled transformer

b) Autotransformer

c) Transmission-line transformer

The operation of a 4:1 transmission-line transformer is explained simply by Johnson [1973], as illustrated in Figure 4.4. The 25 Ω transmission line transforms the unbalanced 25 Ω load (R_1) to a floating 25 Ω impedance. This is connected in series with the other 25 Ω load (R_2), to give 50 Ω. If the electrical length of the transmission line can be considered as being short, the phase shift across it is small and R_1 can be combined with R_2 (Figure 4.4b). An impedance of 12.5 Ω is thus transformed by a factor of 4 times to 50 Ω (Figure 4.4c). The operation of a transmission-line transformer depends on two factors. Firstly, the common mode impedance of the line must be sufficient to isolate the two ends. A ferrite core is commonly used to increase the inductance of the line to achieve this. Secondly, the phase shift across the line must not be excessive. These two conditions constitute practical limits to the high and low frequency performance of transmission-line transformers. Although there is an optimum characteristic impedance for the transmission line, this becomes less critical for moderate bandwidths. As an example, the transformer of Figure 4.4 will work quite acceptably over octave bandwidths using 50 Ω coax, even though a 25 Ω line impedance is called for.

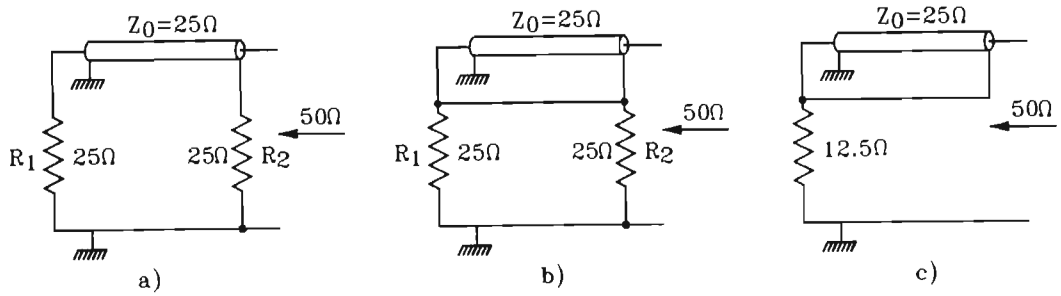


Figure 4.4 Operation of a 4:1 transmission-line transformer

The design of transmission-line transformers requires having sufficient common mode impedance at the lowest frequency, with as short a line as possible, to limit the phase shift across the line at the highest frequency. A further compromise must be made in the choice of ferrite core, since its losses increase with permeability. A commonly used rule of thumb is for the impedance of the magnetising inductance to be at least 4 times that of the respective port impedance.

An example is a 4:1 transmission-line transformer which scales 12.5 Ω to 50 Ω. The impedance of the magnetising inductance at the lowest frequency should be more than 50 Ω and 200 Ω for the low and high impedance ports respectively. Transmission-line transformers are constructed using coaxial cable, bifilar and multifilar twisted lines wound on balun cores or stacked toroids. Coaxial cables, in particular the semi-rigid types, offer the lowest losses for very high power applications.

The characteristics of ferrite materials, such as permeability and loss, vary with the applied magnetic field strength. This nonlinear behaviour is difficult to describe in circuit analysis programs, since the magnetic flux density is not a single valued function of the magnetic field strength. The instantaneous flux density in fact also depends on the previous magnetisation of the material, due to hysteresis. It is, however, considerably simpler to construct a linear ferrite transformer model, and little accuracy is lost. The primary reason is that ferrite RF transformers are not usually driven far into the nonlinear region, since excessive heating would result. A possible area for the use of nonlinear transformer models is that of high power linear amplifiers, where parameters such as intermodulation distortion may be affected.

4.2.1 Linear models

Linear models for an autotransformer and 4:1 transmission-line transformer are discussed. Since a DC path can be built around the AC transformer model if required, only the high frequency characteristics are modelled. Although a conventional magnetically coupled transformer is not treated specifically, the topology and parameter identification procedure for an autotransformer can be applied.

The autotransformer model in Figure 4.5 consists of an ideal transformer, with turns ratio N_1/N_2, and several parasitic elements. The magnetising inductance, L_P shunts the transformer ports to ground. The magnetic flux does not couple into all the turns perfectly, giving rise to a leakage inductance, L_S. Capacitance occurs between the turns of the winding, represented by a single lumped element C_P. Losses occur due to the ferrite core and the resistance of the wire. The ferrite losses result from hysteresis, and to a lesser extent, eddy currents. The copper loss is often negligible compared to that of the ferrite core, which is represented by the parallel resistance R_P.

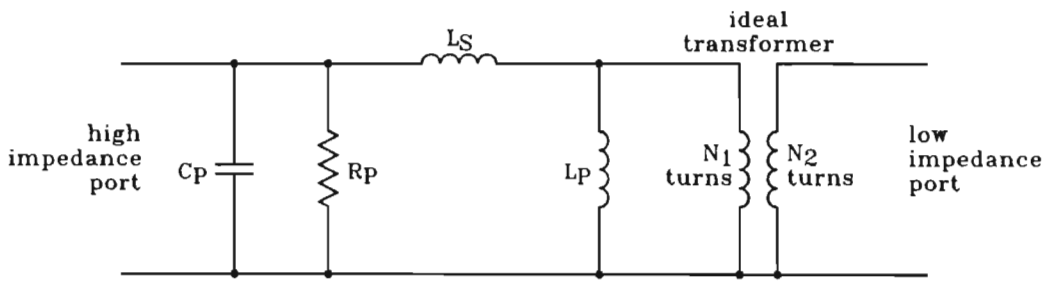


Figure 4.5 Linear autotransformer model

There are several possible methods of determining the five model parameters for a particular autotransformer. The most accurate is perhaps to fit the model to measured S parameters. However, it is more convenient to measure just the impedances into the transformer ports, as follows. Firstly, with the tap open circuit (see Figure 4.3b), the impedance of the entire winding (Z_1) is measured. Secondly, with a 50 Ω

resistance across the winding, Z_2 is measured into the tap. The model is fitted to the two measured impedances by means of computer optimisation. It should be noted that the optimisation's objective function must include both impedances, since neither criterion can establish a unique parameter set by itself. For example, the first measurement gives no information on the turns ratio, while the second obscures the values of R_P and C_P. If the quality of the 50 Ω resistance in the second measurement is poor, it can in effect be calibrated out of the optimisation by representing it as a one-port, with impedance data measured for the particular resistor.

The described method is illustrated for an autotransformer having a total of five turns and a low impedance port with two turns. The optimised model parameter values are shown in Table 4.4, and the resulting impedances compared to measurements in Table 4.5. Of the two impedances, it is more important that Z_2 be modelled accurately, as the transformer operates with similar impedance levels in an RF power amplifier.

Table 4.4 Optimised parameter values for autotransformer model

R_p (Ω)	C_p (pF)	L_s (nH)	L_p (nH)	N_1 / N_2
7869	1.06	30.66	637.6	2.353

Table 4.5 Autotransformer impedances : measured and modelled

	Z_1 (Ω)		Z_2 (Ω)	
Freq. (MHz)	measured	modelled	measured	modelled
118	63.5 + j805	82.5 + j801	8.08 + j4.42	8.14 + j4.42
150	300 + j1600	346 + j1600	8.19 + j5.21	8.16 + j5.22
175	2300 + j3500	2300 + j3600	8.22 + 5.90	8.17 + j5.89

The autotransformer model in Figure 4.5 uses an ideal transformer, described by its turns ratio. A mutually coupled coil can also be used in a CAD package, as shown in Figure 4.6. The required parameters are the magnetising inductances, L_1 and L_2, and the mutual inductance M. The calculations to derive these from the parameters of Figure 4.5 are given in equations **(4.2) - (4.4)**. The coupling factor of 1.0 in **(4.4)** corresponds to an ideal transformer.

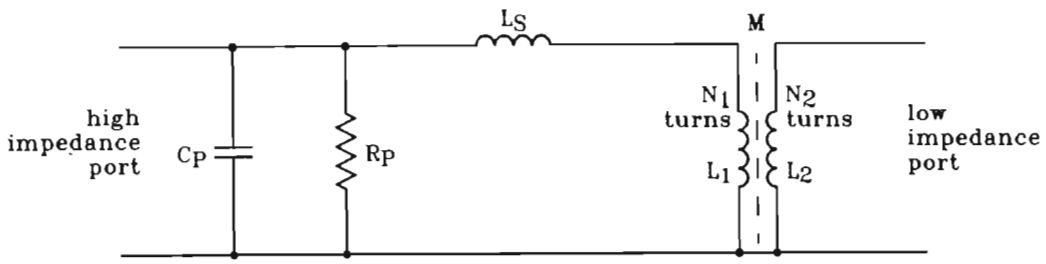


Figure 4.6 Autotransformer model using coupled-coil element

$$L_1 = L_P \quad \textbf{(4.2)}$$

$$L_2 = L_1 (N_2 / N_1)^2 \quad \textbf{(4.3)}$$

$$M = 1.0\sqrt{(L_1 L_2)} \quad \textbf{(4.4)}$$

A transmission-line transformer model is given in Figure 4.7. This employs an ideal transmission line and elements arising from the ferrite core. The line has a characteristic impedance Z_0 and an electrical length E, specified at 100 MHz in this case. The common mode impedance of the line, enhanced by the ferrite core, is determined by the shunt inductance L_P. The hysteresis and eddy current losses of the ferrite core are represented by R_P.

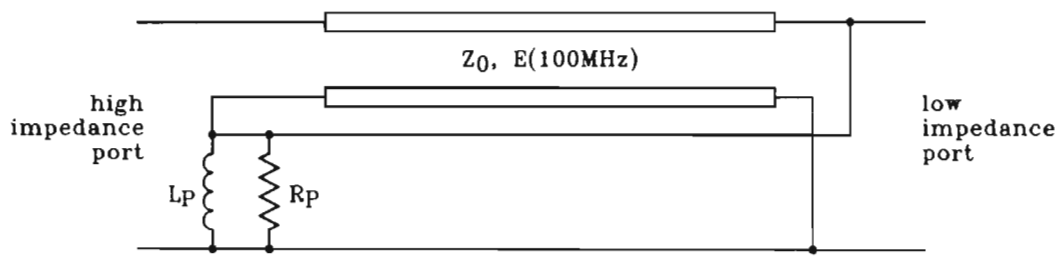


Figure 4.7 Transmission-line transformer model

A parameter extraction scheme, whereby the model is fitted to two impedance measurements, as demonstrated for an autotransformer, cannot be used for a transmission-line transformer. The model impedances are not a strong function of the line's characteristic impedance and electrical length, which can result in unrealistic parameter values. An example of one such optimisation gave $Z_0 = 180.3\ \Omega$ and $E = 4.3\ °$ for a standard 50 Ω coaxial cable with an expected electrical length of about 16.5 °. In order to extract physically consistent parameter values, the following technique is used, consisting of impedance measurements, calculations and an optimisation.

Three impedances must be determined for the parameter extraction. Firstly, the common mode impedance Z_1 of the transmission line on the core is measured. This is probably best done directly, but a similar result is obtained using enamelled copper wire, with the same number of turns as the transmission line. Secondly, with a 50 Ω resistance across the high impedance port, Z_2 is measured into the other port. Finally, if the value of Z_0 for the transmission line is not known accurately, for instance with a twisted-wire line, then this must be determined. Two methods which are commonly used to obtain the characteristic impedance of a transmission line are given [Motorola AN-546, 1971]. The first method measures the impedance into a quarter-wave length of line, which is terminated by a resistance equal to approximately half the expected value of Z_0. The quarter wavelength requirement is obtained by increasing the frequency until the measured impedance is purely resistive. A physical line length should be chosen so that this frequency is near to that at which the transformer operates. The line's characteristic impedance is given by:

$$Z_0 = \sqrt{(R_L \cdot R_{in})} \qquad \textbf{(4.5)}$$

where R_L = termination resistance

R_{in} = measured input impedance

The second method measures the impedances into a line which is terminated first with an open circuit and then with a short circuit. A line length of approximately $\lambda/8$ should be used. The characteristic impedance of the line is given by :

$$Z_0 = \sqrt{(|X_S| \cdot |X_O|)} \qquad \textbf{(4.6)}$$

where X_S = input reactance with short circuit termination

X_O = input reactance with open circuit termination

The value of R_P is calculated from the Z_1 measurement, by taking the real part of the equivalent admittance. The remaining two parameters, L_P and E, are obtained by optimising the model to fit the measured values of Z_2.

There are a number of possible variations to the given technique. Firstly, the impedance Z_1 can be added to the objective function, treating R_P as a variable. This inevitably degrades the fit of Z_2, which is more important. Also, due to its small influence, inaccurate values of R_P may result. Secondly, all the parameter values can be determined without optimisation. The values of R_P and L_P are calculated from Z_1, by converting this to an admittance. The characteristic impedance and electrical length are found using the previously given method involving a resistively terminated transmission line. Although slower, optimisation provides better results than direct calculation.

The described parameter extraction technique is demonstrated for a 4:1 transmission-line transformer having two turns of 50 Ω coaxial cable. The value of R_P is calculated at 100 MHz. The final model parameters are given in Table 4.6 and the results compared in Table 4.7.

Table 4.6 Parameter values for transmission-line transformer model

R_p (Ω)	L_p (nH)	Z_0 (Ω)	E (°)
3161	123.7	50.0	18.504

Table 4.7 Transmission-line transformer impedances : measured and modelled

	Z_1 (Ω)		Z_2 (Ω)	
Freq. (MHz)	measured	modelled	measured	modelled
10	0.10 + j8.96	0.02 + j 7.77	3.37 + j5.58	3.42 + j5.56
50	0.75 + j44.4	0.48 + j38.9	10.7 + j4.90	10.5 + j4.69
100	2.46 + j88.2	1.91 + j77.7	11.5 + j4.87	11.2 + j4.64
200	11.8 + j181.6	7.63 + j155.1	12.0 + j7.00	11.1 + j6.88

To confirm that the optimised values of L_p and E are physically consistent, they are compared to direct calculations. A value for L_p of 140.5 nH is obtained from the admittance corresponding to the Z_1 measurement at 100 MHz. The electrical length E is calculated to be approximately 16.5 ° at 100 MHz, using the physical length of the line and an assumed propagation velocity of 2×10^8 $m.s^{-1}$. The optimised parameters in Table 4.6 are close to these values.

4.2.2 Nonlinear models

A ferrite core is nonlinear since the flux density B is not proportional to the applied magnetic field strength H. It is seen in Figure 4.8 that, due to hysteresis, the flux density is not an explicit function of H, but depends on the previous magnetisation. Although hysteresis loops are given for only three particular values of maximum

magnetic field strength, a large number of such curves could be drawn. These characteristics cannot be described in standard nonlinear RF analysis packages.

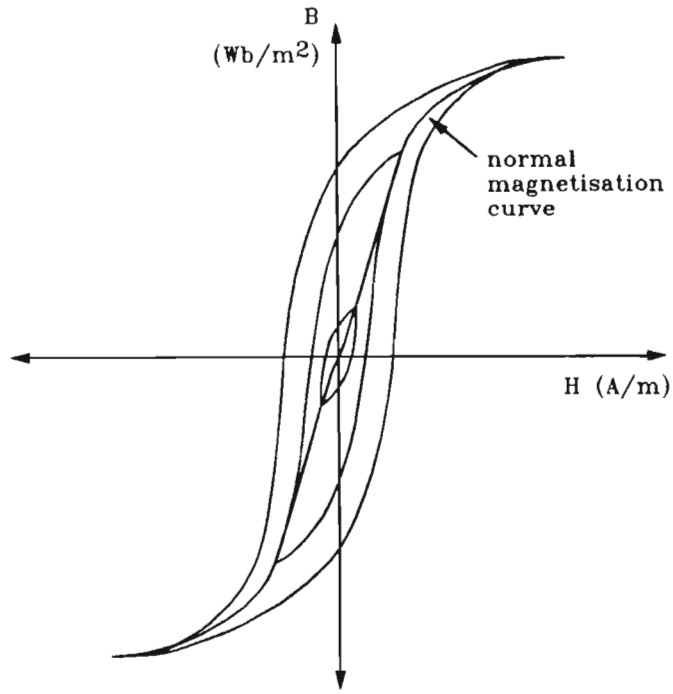
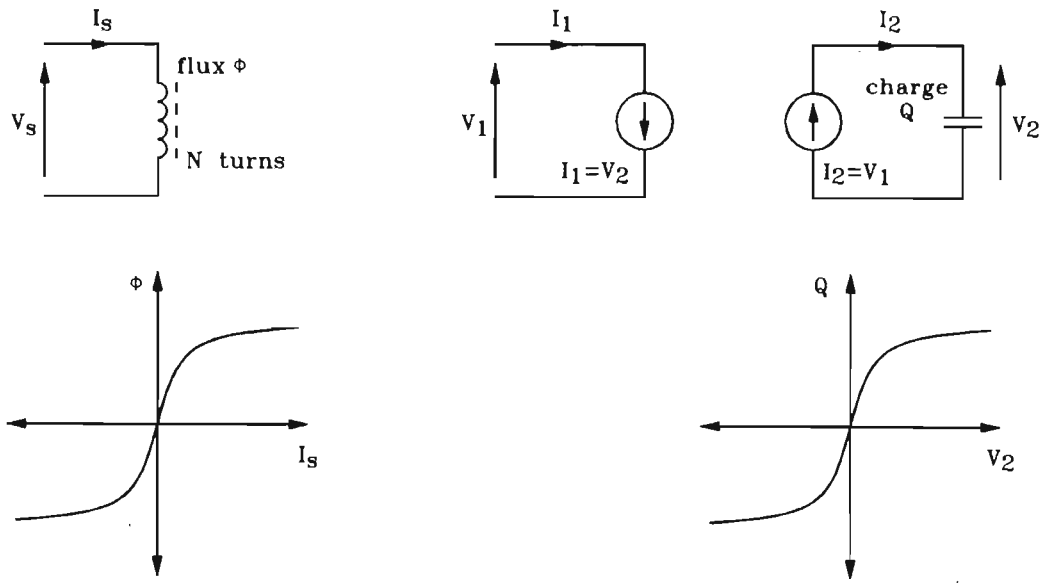


Figure 4.8 Magnetic hysteresis loops

The magnetic characteristics of ferrite materials can be approximated using the normal magnetisation curve which is shown in Figure 4.8. This curve is defined by the endpoints of successively larger hysteresis loops. The flux density is thus described as a single-valued function of magnetic field strength and can therefore be included in nonlinear CAD programs. The approximation is reasonably accurate as the ferrite cores which are used in RF transformers have narrow hysteresis loops. The loop is necessarily narrow in high frequency materials since its area represents energy lost per cycle, manifested as heating of the core.

Typically, RF analysis packages do not permit the description of elements in terms of magnetic quantities, such as flux density and magnetic field strength. An alternative method is therefore devised, relating the external currents and voltages of an inductor to its internal nonlinear magnetic characteristics, using a nonlinear

capacitor. A capacitive element is used due to the requirements of the CAD package, LIBRA. With this program, user-defined nonlinear components must be described in terms of their voltage dependent currents and charges, and the derivatives of these with respect to voltage, ie. conductance and capacitance. A nonlinear capacitor is accommodated easily within this framework. In linear circuits, a gyrator is used to convert an impedance to its inverse. A capacitor is thus transformed to an inductor, which can, for instance, be used with inductor-less op-amp filters. This concept is extended to nonlinear capacitors and inductors. Using equations **(4.7) - (4.10)**, it is shown that the equivalent circuit in Figure 4.9 has the same current/voltage characteristics as the nonlinear inductor. The quantities Φ and I_s in Figure 4.9a are proportional to B and H respectively, with constants which relate to the core dimensions and number of turns.



$$\Phi\ (I_S) = f_1\ (I_S)$$
$$\partial\Phi\ /\ \partial I_S = f_1'\ (I_S)$$

a)

$$Q = N\ f_1\ (V_2)$$
$$\partial Q/\partial V_2 = N f_1'\ (V_2)$$

b)

Figure 4.9 Nonlinear inductor and equivalent circuit

a) Nonlinear inductor and flux/current relationships

b) Nonlinear capacitor equivalent circuit and charge/voltage relationships

$$V_S = N\frac{\partial \Phi}{\partial t} = N\frac{\partial \Phi}{\partial I_S}\frac{\partial I_S}{\partial t} \qquad \textbf{(4.7)}$$

$$\frac{\partial I_S}{\partial t} = \frac{V_S}{\left(Nf_1'(I_S)\right)} \qquad \textbf{(4.8)}$$

$$\frac{\partial I_1}{\partial t} = \frac{\partial V_2}{\partial t} = \frac{\partial V_2}{\partial Q}\frac{\partial Q}{\partial t} = \frac{\partial v_2}{\partial Q}I_2 = \frac{\partial V_2}{\partial Q}V_1 \qquad \textbf{(4.9)}$$

$$\frac{\partial I_1}{\partial t} = \frac{V_1}{\left(Nf_1'(V_2)\right)} = \frac{V_1}{\left(Nf_1'(I_1)\right)} \qquad \textbf{(4.10)}$$

Flux/current and charge/voltage definitions are given in Figure 4.9, for the nonlinear inductor and capacitor, respectively. Equation **(4.7)** stems from Faraday's law, which relates the voltage induced in a winding to the rate of change of flux. For the inductor in Figure 4.9a, which is lossless, the induced voltage equals the supply voltage V_S. Since the flux is a function of I_S, the expression in **(4.7)** can be expanded, using the chain rule of calculus. The derivative $\partial\Phi/\partial I_S$ equals $f_1'(I_S)$, giving **(4.8)**. Equation **(4.9)** gives the rate of change of I_1 in Figure 4.9b. The capacitor voltage V_2 equals I_1, and can be substituted. After the expansion of the derivative by the chain rule, it is seen that the term $\partial Q/\partial t$ represents the current I_2, which equals V_1. From the definition of $Q = Nf_1(V_2)$, it follows that $Nf_1'(V_2)$ can be substituted to yield **(4.10)**. Finally, V_2 can be replaced by I_1. Equations **(4.8)** and **(4.10)** show that the rates of change of I_S in Figure 4.9a and I_1 in Figure 4.9b are governed by the same functions of supply voltage and current. Thus, using the given charge/voltage capacitor definition, the equivalent circuit of Figure 4.9b behaves as the nonlinear inductor of Figure 4.9a.

A nonlinear transformer model (Figure 4.10) is constructed using the equivalent circuit of Figure 4.9b. The model parameters are representative of a 50 Hz mains transformer, which is convenient to measure. Although no attempt is made to model accurately any particular transformer, the example illustrates the technique and resulting waveforms.

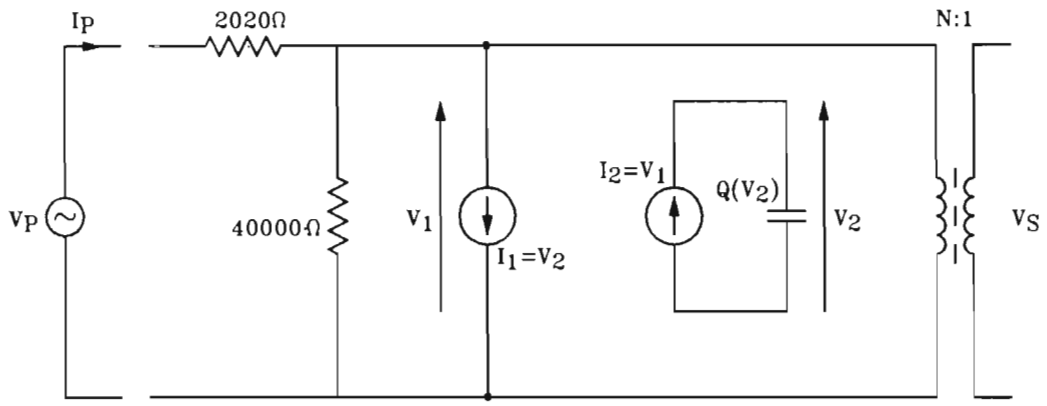


Figure 4.10 Nonlinear transformer model and voltage supply

The charge/voltage relationships for the nonlinear capacitor in Figure 4.10 are given in equations **(4.11)** and **(4.12)**. The $\tan^{-1}$ function provides a characteristic corresponding to saturation of magnetic core flux.

$$Q = \frac{1}{k} \tan^{-1}(k V_2) \qquad \textbf{(4.11)}$$

$$\frac{\partial Q}{\partial V} = \frac{1}{(1 + k^2 V^2)} \qquad \textbf{(4.12)}$$

The current and voltage characteristics of the transformer primary are shown in Figure 4.11. The current waveform lags the supply voltage and shows the distortion associated with typical hysteresis curves [Plonus, 1978, p427]. Similar waveforms are measured for small mains transformers.

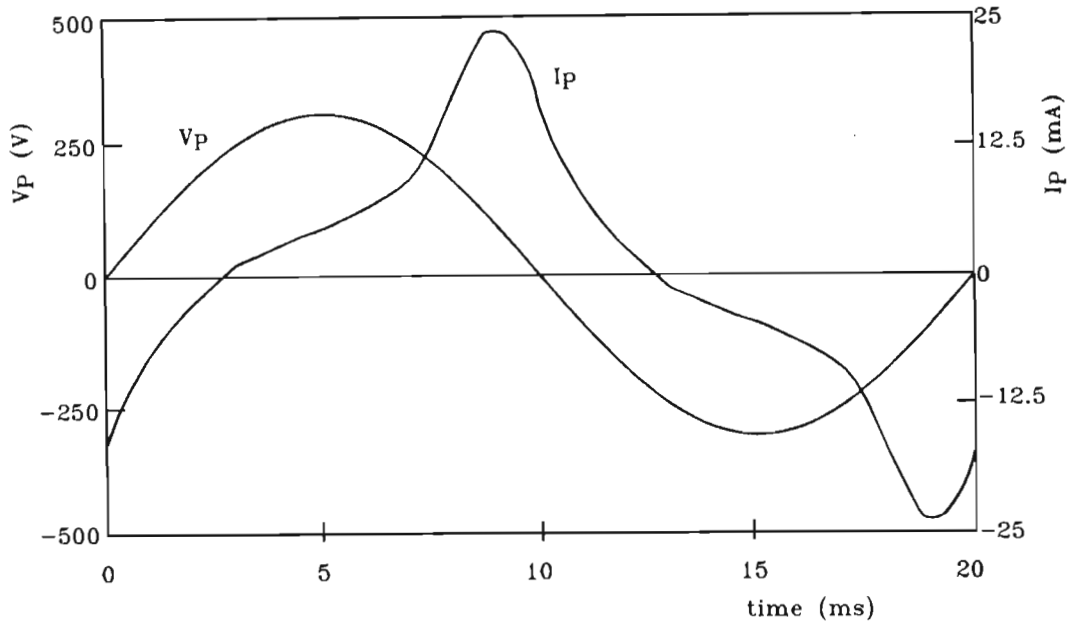


Figure 4.11 Primary voltage and current waveforms for the nonlinear transformer model

The nonlinear transformer model is not used for the amplifier of chapter 6, since the harmonics generated by the ferrite core are negligible compared to those of the MOSFET. However, in a linear power amplifier, the distortion caused by ferrite cores is significant. A complete analysis would require the use of a nonlinear transformer model.

4.3 RLC networks

RLC networks are typically used together with transformers in RF power amplifiers for impedance scaling. An example is an input matching network which transforms the relatively low gate impedance up to 50 Ω. Any errors in the network model will result in a design with a correspondingly poor input impedance. These errors arise from the measurement of individual components as well as inaccuracies in the component descriptions.

4.3.1 Component measurement errors

For the modelling of small R, L, C components, impedance bridge measurements are relatively inaccurate and a calibrated ANA is preferred. The test fixture must accommodate components with lead spacings ranging from about 2 mm to 10 mm. A convenient method employs a length of flexible coaxial cable and tinned copper-clad board. A calibration is effected at the end of the cable using short, open and 50 Ω standards. At frequencies below 400 MHz, the short and open conditions can be obtained simply by grounding the centre conductor or leaving it free, both with the outer grounded. Similarly, two physically small 100 Ω resistors, connected from the centre to ground, constitute a reasonable 50 Ω standard. Ground connections should be made close to the outer conductor, and all lead lengths kept to a minimum. For greater accuracy, verified SMA standards can be connected to a microstripline, with the appropriate offset delay included in the ANA CAL kit.

The measurement environment has a significant effect on accuracy. Temperature is probably the most important factor, changing the cable delay and component characteristics, especially those of capacitors. To counter this, ambient temperatures should be kept stable, and soldered components allowed to cool sufficiently before measurements are taken. For an inductor, due to changes in the ambient temperature, a variation in impedance of up to 4% was measured. Bending and re-positioning of the cable can additionally cause impedance changes of up to 3%. With due care, however, repeatability errors should be limited to a few percent.

4.3.2 Component description errors

The relatively small errors involved in modelling individual components can become large when a multi-element network is analysed. This problem is illustrated using the network of Figure 4.12, obtained from the input circuit of a 15 W amplifier design.

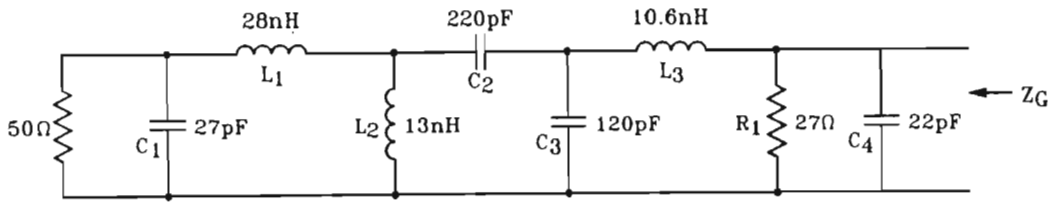


Figure 4.12 Input matching circuit

The physical circuit is constructed with plate ceramic capacitors, air-cored inductors wound with enamelled copper wire, and 1/4 W metal film resistors. The component models include parasitic series inductance for the capacitors and resistors, and parallel capacitance with the inductors.

The models are fitted at five frequencies from 118 MHz to 450 MHz, yielding the parameters in Table 4.8.

Table 4.8 Nominal component values and model parameters

nominal		C_1	C_2	C_3	C_4		R_1		L_1	L_2	L_3
value	(pF)	27	220	120	22	(Ω)	27	(nH)	28	13	10.6
model	C (pF)	27.2	225	119	22.1	R (Ω)	26.9	L (nH)	28.2	13.1	10.6
parms.	L_s (nH)	2.50	1.46	2.04	3.10	L_s (nH)	3.60	C_p (pF)	0.10	0.04	0.00

The modelled network impedances are compared to measurements in Table 4.9. The vector errors are calculated using the method in section 3.1.3 .

Table 4.9 Measured and calculated network impedances

Freq. (MHz)		100	118	150	175	300	450
Z_G (Ω)	Re (Z)	4.59	7.97	6.52	5.87	30.2	2.48
measured	Im (Z)	5.64	4.67	2.66	4.15	5.99	-10.12
Z_G (Ω)	Re (Z)	5.27	8.49	7.85	7.54	27.9	3.34
calculated	Im (Z)	6.28	5.05	3.10	3.00	4.60	-9.57
Relative error		12.8 %	7.0 %	19.9 %	28.2 %	8.8 %	9.8 %

A number of possible reasons for the large errors in modelled impedances are investigated. Firstly, if the model is optimised to fit the measured impedances, allowing only the series inductance values to vary by approximately 1 nH, the maximum error is reduced to 7.5%. The tolerance of 1 nH is within the variation expected of the construction method, which was to solder the components onto a copper-clad board. Secondly, the addition of coupling between the inductors produced no significant improvement, discounting this phenomenon as a cause of error. Thirdly, the network was rebuilt using the same components, placing them in slightly different orientations. The impedances of this and the first-constructed network are different by an average of 9%. This may be due to a change in effective lead length and hence series inductance, or result from altered coil dimensions. Another possibility is a shift in inductance values caused by proximity to other

components and the groundplane. Lastly, a sensitivity analysis shows that the parasitic series inductance of the capacitors has an inordinately large effect on the network impedance.

The above discussion suggests that the series inductance of components, particularly capacitors, is the predominant cause of the large model errors. The example given, however, exaggerates the problem, due to the relatively poor quality capacitors used. Network modelling errors can be minimised by the use of good quality capacitors, careful measurement of individual components and by constructing the circuit on a PCB layout, which will also improve repeatability.

Chapter 5

Analysis and design of RF power amplifiers

The design of high power RF amplifiers has in the past relied heavily on measurements, with simple linear theory being used for the matching networks. The computer-aided analysis of nonlinear RF circuits has been commercially unattractive due to the slowness of time-domain methods. However, CAD packages using harmonic balance techniques are now available which offer greatly reduced analysis times. These computer-aided methods are a valuable addition to the traditional design tools.

5.1 Design methods

The basic requirements for an RF power amplifier are that it can produce the required output power with acceptable gain, efficiency, harmonics and input impedance over the frequency band. It is also necessary that the amplifier be stable, with sufficiently low spurious outputs, even under severe load-mismatch conditions. Special requirements may be dictated by the modulation method, for example linearity in the case of SSB transmitters.

The design of an amplifier will typically begin with the choice of topology and the selection of active devices. In general, greater linearity will be obtained with high quiescent currents, although this reduces the amplifier efficiency. Methods of stabilisation include gate shunt-loading and negative feedback from drain to gate. In both cases, increased stability is obtained at the expense of amplifier gain. The output matching network is chosen largely on the basis of the output power requirement, while the input network is designed so that a specified impedance, normally 50 Ω, is seen into the amplifier. Because the input impedance is strongly affected by the drain load and stability enhancing elements, the input matching network must be designed last. The amplifier design is finalised by adjusting the circuit component values so that the required specifications are obtained.

The design process which has been outlined can incorporate a number of theoretical and empirical techniques. At the lowest level, an essentially trial and error approach may be adopted, using a minimum of test equipment such as a power meter and spectrum analyser. Significant advantage can be gained by first determining a circuit design which requires only minimal adjustment to obtain the desired performance.

5.1.1 Estimation of drain load impedance

A simple theoretical method of determining the required drain load impedance for an amplifier is to assume that the drain voltage is sinusoidal. For a single-ended class AB amplifier, if the drain voltage swing is approximately between ground and twice the supply, the output power can be approximated by:

$$P_{OUT} = \frac{(V_S / \sqrt{2})^2}{R_L} \tag{5.1}$$

where V_S = supply voltage
R_L = drain load resistance

The calculation may be refined by taking into account the effect of the MOSFET on-resistance R_{DSon} and the MOSFET capacitances. Due to the MOSFET on-resistance, the drain voltage cannot be pulled to ground during the RF cycle, thus reducing the AC voltage. The drain is shunted by the MOSFET feedback and output capacitances, which may be approximated by C_{oss}. To develop maximum output power and gain, the load admittance should include an inductive susceptance which cancels this. The required load admittance is :

$$Y_L = \frac{P_{OUT}}{[\,(V_S - V_{DSon}) / \sqrt{2}\,]^2} - j\omega C_{oss} \tag{5.2}$$

where V_{DSon} = minimum drain-source voltage during the RF cycle

For example, to obtain an output of 15 W from a 28 V device with V_{DSon} = 2.5 V, this implies a load conductance of 46.1 x 10^{-3} S, which corresponds to a resistance of 21.7 Ω. At 150 MHz, if the drain shunt capacitance is 27 pF, the required load impedance is 16.6 + j9.2 Ω.

5.1.2 Source and load impedance data

Empirical impedance data is available for RF power transistors manufactured by Motorola. This gives the optimum source and load impedances for a device with a particular supply voltage, quiescent current, output power and frequency. These large-signal impedances are measured using a test circuit such as that shown in Figure 5.1 [Motorola AN-282 A, 1991]. Typically, a gate bias resistance of 27 Ω is used in order to ensure stability. The input and output matching networks are adjusted to give maximum gain with low input VSWR for a specified output power. The transistor is then removed from the fixture and the source and load replaced with 50 Ω terminations. Impedances are measured at the gate and drain circuit connections, c and d respectively. Although it is not clear in the device data sheets, a duplicate experiment confirms that the first impedance is measured at plane c and not plane b. The data sheet gives the conjugate of these measured values, describing them as large-signal input and output impedances.

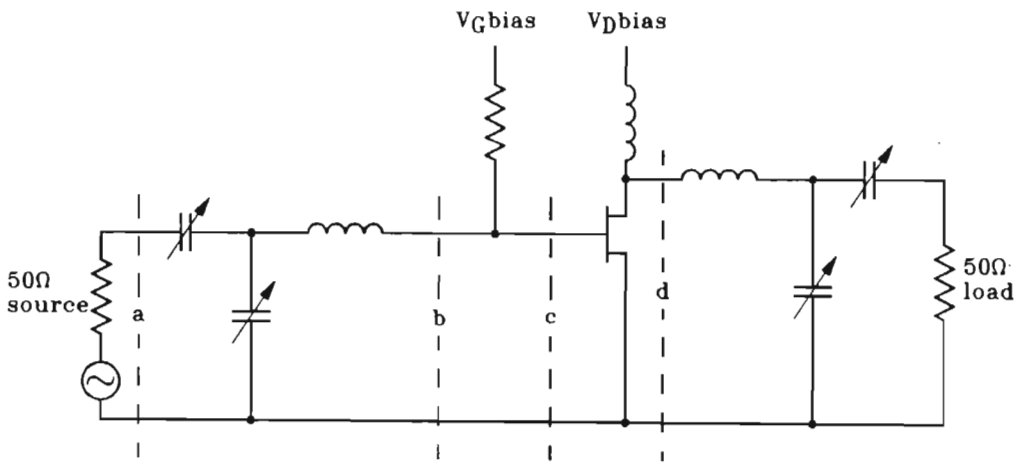


Figure 5.1 Test fixture for MOSFET large-signal impedance measurements

It is important to note that the data sheet does not give the impedances seen into the gate and drain, as would be the case for a conjugately matched small-signal device. Firstly, the concept of output impedance cannot be applied to nonlinear power amplifiers where the drain current-controlling element is essentially a switch, albeit non-ideal, giving an efficiency of typically 60 %. This is confirmed by noting that a generator with an impedance equal to that of its load cannot have an efficiency greater than 50 %. Secondly, although the input matching network is lossless and is matched to the 50 Ω source, there is not a conjugate match at the device's gate. This is due to the presence of the gate bias resistor. Figure 5.2 gives an example of a network which matches an impedance to a 50 Ω source, with planes a, b and c corresponding to those in Figure 5.1. The elements are calculated using a Smith chart to give the data sheet value of large-signal input impedance for an MRF136 MOSFET at 150 MHz, which is $4.1 - j7.6\ \Omega$. It is seen in Figure 5.2 that there is a conjugate match at all planes from the source to plane b, but not at c. The data sheet value of large-signal input impedance is thus not equal to that seen into the gate, which is $-1.6 - j9.6\ \Omega$. The negative real part of the gate impedance indicates the need for the shunt 27 Ω resistor in order to achieve amplifier stability.

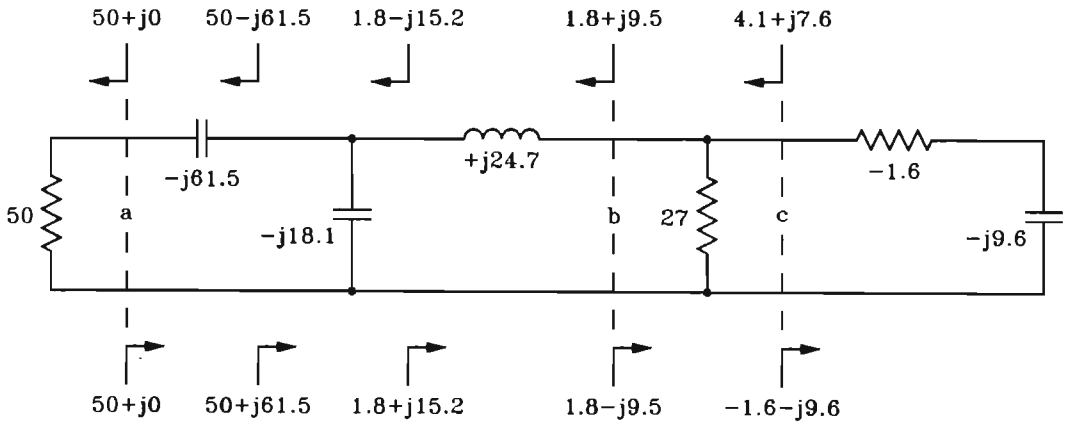


Figure 5.2 Example of input matching network with calculated impedances

Table 5.1 compares the values of drain load impedance obtained from equation **(5.2)** and the device data sheet to those measured for an MRF136 at 150 MHz. The supply voltage is 28 V with an output power of 15 W. The first measured value is taken from a narrowband amplifier similar to the test fixture of Figure 5.1. The second

measurement is for an amplifier operating from 118 MHz to 175 MHz, using autotransformers and LC elements in the matching networks. It is seen that the data sheet and narrowband amplifier values correspond to each other but are quite different to those obtained from equation **(5.2)** and the broadband amplifier. The discrepancy between the narrowband and broadband values is possibly the result of large differences in the harmonic impedances. The drain load impedance at the second harmonic is estimated to be 7.4 + j25.6 Ω for the broadband amplifier and 5.7 + j72 Ω for the narrowband circuit. Furthermore, the broadband amplifier was not optimised at 150 MHz but adjusted for best performance over the frequency band.

Table 5.1 Measured and calculated values of drain load impedance for MRF136

	Equation **(5.2)**	Data sheet	Narrowband measurement	Broadband measurement
Z_L (Ω)	16.6+j9.2	9.1+j15.4	6.7+j15.0	16.9+j12.3

5.1.3 High-power impedance measurements

An empirical design technique, which allows impedances to be measured with a source power of several watts, is illustrated within the context of a complete measurement setup in Figure 5.3. A linear amplifier provides a high power source from the RF output of the automatic network analyser (ANA). A four-port directional coupler samples the incident and reflected waves, feeding a portion of these back to the ANA inputs. If the output impedance of the linear amplifier is poor, or the directional coupler degrades the impedance of this source, a 3 dB attenuator may be included. The forward power delivered to the input of the amplifier is measured by a directional power meter. Connection to the amplifier is made through small-diameter flexible coaxial cable. The parameter S_{11} is defined to be the ratio of reflected and incident waves, and calibrated using short, open and load standards at the end of the coaxial cable, using a low power level. Since a ratio is considered, the calibration is valid for any power and does not depend on the linearity

of the source amplifier. Although harmonics may be present, the ANA measures only the fundamental frequency. The measurement setup is completed with a second directional power meter to measure the output power of the amplifier under test and a spectrum analyser to check for instabilities and spurious outputs.

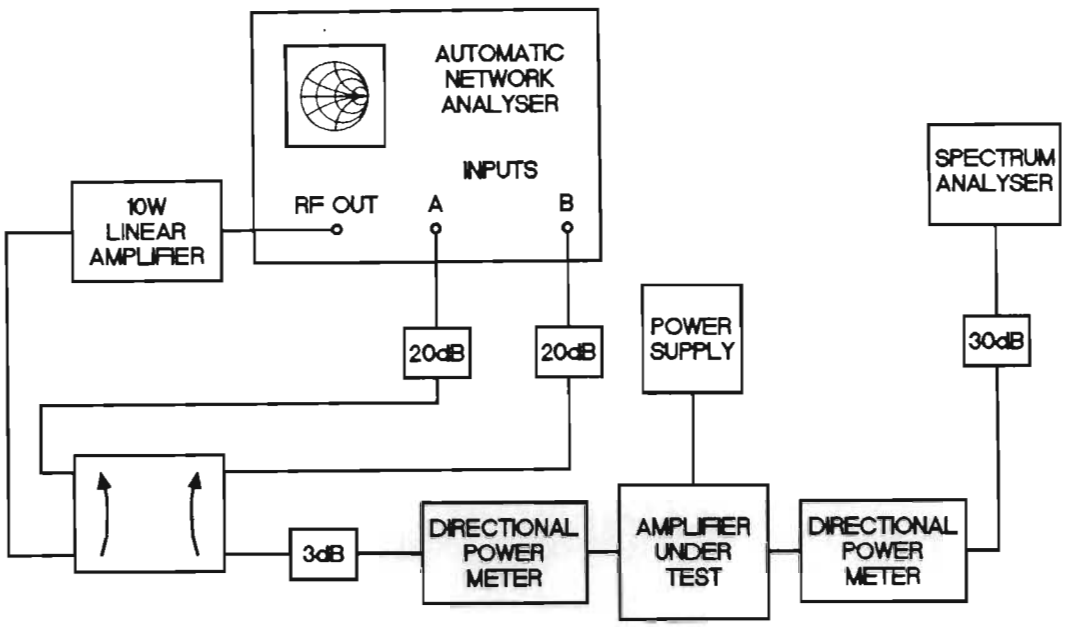


Figure 5.3 Measurement setup for empirical design of RF power amplifiers

Using the described technique, the input impedance of the amplifier under test can be viewed in Smith chart format on the ANA. Assuming that a suitable output matching network has been designed, the input network can be developed empirically, beginning with only stabilising elements. By observing the impedance versus frequency trace, appropriate matching elements can be added until a low input VSWR is achieved over the frequency band. Finally, the entire amplifier can be adjusted to optimise its performance parameters such as gain flatness, input VSWR, efficiency and stability under load mismatch conditions. A minor problem is that the power delivered to the amplifier is not constant with frequency, due to the frequency dependent characteristics of the ANA source and linear amplifier. This is undesirable if the input impedance of the amplifier under test changes significantly with drive level. A simple solution would be to control the ANA from a PC through an HPIB card, automatically setting an appropriate source power for each frequency.

5.1.4 New design methods

The previously described design methods have important limitations. The drain load impedance given by equation **(5.2)** can only be regarded as a rough starting point. The large-signal impedance values are measured under narrowband conditions and are inaccurate for wideband amplifiers. Furthermore, the use of this data is limited to the specific stabilising network of the test circuit and particular operating parameters such as supply voltage and output power. Design techniques which are largely empirical have a number of disadvantages. Firstly, since it is time consuming to evaluate different circuit topologies, an optimal design is difficult to attain. Secondly, some physical components, such as microstriplines, are not easily adjusted. Thirdly, there is a danger of the active device being damaged or destroyed, especially in the initial stages of the design.

In contrast to small-signal design, computer-aided techniques have not been applied routinely to nonlinear RF circuits. This has been due primarily to the slowness of time-domain analysis methods. However, CAD packages using harmonic balance techniques have recently become widely available. These allow rapid analysis of RF power amplifiers. A new design strategy can thus be developed, yielding better initial circuits which require little empirical development. This will lead to improved circuit performance and faster design times.

5.2 Nonlinear computer-aided design programs

The methods which are available for the analysis of nonlinear RF circuits can be divided into three types. Circuit elements may be analysed in the time domain, in the frequency domain, for example using Volterra series [Law and Aitchison, 1986], or with a combination of time and frequency domain methods, such as the harmonic balance technique [Gilmore, 1986]. None of these methods constitutes a complete analysis tool, each being more efficient in different applications.

Time-domain simulators describe circuits using differential equations, which can be solved by numerical integration to give the node voltages at discrete time points. Analysis of circuits having greatly different time constants is inefficient, since the integration time step must be short enough for the smallest time constant, while the number of time steps is dictated by the largest time constant. A similar situation applies if widely differing frequencies are considered, as would occur with amplitude modulated signals. Also, time-domain methods have poor dynamic range, making it difficult to analyse circuits having signals with greatly different amplitudes, such as mixers. Finally, the analysis of circuits with distributed elements is slow, particularly for mismatched transmission lines, where multiple reflections must be considered.

With Volterra-series analysis, the nonlinear elements are represented by power series, typically up to the third order. The circuit is analysed entirely in the frequency domain, allowing a large number of harmonically-unrelated frequencies to be included. This method is restricted to weakly nonlinear circuits. A related technique, Generalised Power Series Analysis [Rhyne *et al*, 1988], addresses this problem.

The harmonic balance technique attempts to find a voltage spectrum at each circuit node such that Kirchoff's current law is true at each harmonic. To reduce the number of unknowns, the circuit is partitioned into linear and nonlinear subcircuits, balancing the currents into the common nodes. The estimated voltage spectrum at each of these nodes is Fourier transformed into time-domain signals, which are applied to the nonlinear elements. The resulting time-domain currents are transformed back into the frequency domain and compared to the current spectrum of the linear subcircuit, which can be analysed using standard frequency domain methods. The harmonic balance is commonly obtained by iterative optimisation. Use of the discrete Fourier transform restricts analysis to harmonically related signals. In order to analyse circuits such as mixers, which may have two closely spaced frequencies, a number of modified harmonic balance techniques have been developed [Kundert *et al*, 1988].

Commonly available nonlinear simulators use time-domain or harmonic balance techniques. The principal application for time-domain programs is the analysis of

transients, which is not possible with harmonic balance. However, for steady-state analysis, the harmonic balance program is often over 100 times faster. This is particularly true if the circuit contains distributed elements. The use of nonlinear analysis programs is illustrated for two well-known versions, using the time domain (MWSPICE) and harmonic balance (LIBRA) methods respectively.

Both LIBRA and MWSPICE employ a text file to describe the circuit and analysis requirements. An optional DIM block overrides the default units of parameters such as frequency and inductance. The CKT and SOURCE blocks together define the circuit topology, using a numbered nodal description. (A notable exception to this form of circuit description is the use of symbols to represent graphically the elements and circuit [HP85150].) The required frequencies are given in the FREQ block, and in LIBRA, a range of source power levels can be specified in the POWER block. An important component of the circuit files are statements which affect the analysis process. In LIBRA, the HBCNTL block contains a number of terms. A compromise must be made between analysis speed, accuracy and convergence. The INITNH and FTRUNC terms apply to the analysis frequencies, while RELTOL, RELTOLV and ABSTOLV specify the required accuracy of the solution. The values of SAMAN and SAMPLE are used to solve nonconvergence. The CONTROL block in MWSPICE specifies the maximum step size, the analysis duration, the time from which results should be saved and the intervals thereof. The maximum step size can be important in determining the accuracy of the solution in certain situations, such as the transition of an unstable circuit into oscillation. The output of LIBRA is specified in the OUTVAR, OUTEQN, OUT and GRID blocks, allowing a wide choice of circuit parameters and presentation of results. In MWSPICE, the blocks, SPICEOUT, FUNCT and OUT apply. An important specification in the FUNCT block is that of Fourier transforms, which allow the display of results in the frequency domain.

5.3 Description of nonlinear MOSFET model

The model of Figure 1.6 contains two forms of nonlinear elements, which are the capacitors, C_{DG} and C_{DS}, and the voltage-controlled current source. In LIBRA and

MWSPICE, these are created as user-defined elements, which can be included in the circuit file. This requires the writing of code to calculate currents and charges, as well as the derivatives of these with respect to voltage.

In the extraction of the model parameters, the nonlinear capacitors are described by voltage-dependent values of differential capacitance, using equation **(3.1)**. The charge is obtained from this by integration. It should be noted, however, that the charge is considered as the fundamental capacitor characteristic. The resulting expressions of charge and capacitance are given in equations **(5.3)** and **(5.4)**, shown graphically in Figure 5.4.

$$Q = \frac{a_0}{a_1 (1 - a_2)} (a_1 V + 1)^{1 - a_2} - \frac{a_0}{a_1 (1 - a_2)} \qquad V > 0$$

$$Q = a_0 V \qquad V \leq 0 \qquad \textbf{(5.3)}$$

$$C = Q'(V) = \frac{a_0}{(1 + a_1 V)^{a_2}} \qquad V > 0$$

$$C = a_0 \qquad V \leq 0 \qquad \textbf{(5.4)}$$

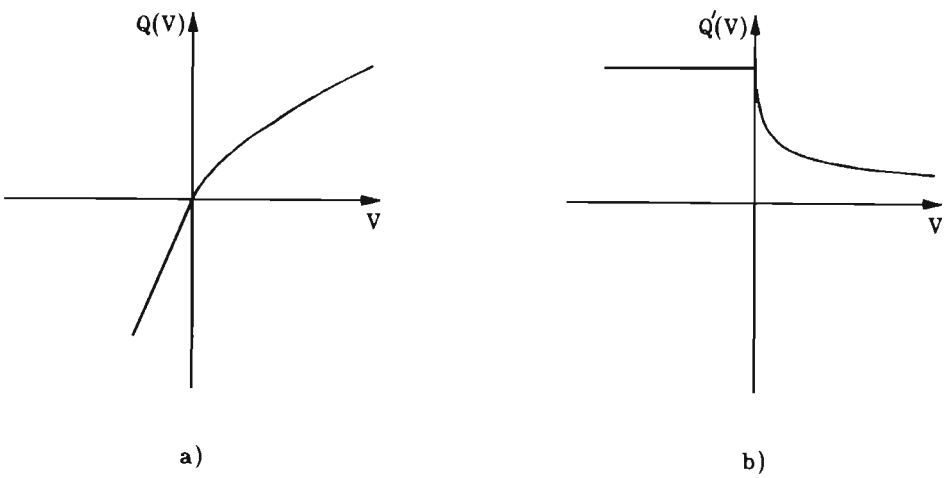


Figure 5.4 Description of nonlinear capacitor a) charge b) capacitance

From Figure 5.4, it is seen that the derivative of capacitance with respect to voltage has a discontinuity at zero voltage. This can prevent the convergence of harmonic balance simulations. A solution is to use a polynomial to describe the charge in a small interval around V = 0. If the polynomial is of high enough order, the function $Q''(V)$ can be made continuous. However, to obtain convergence, it is sufficient merely to reduce the size of the discontinuity. For example, a quadratic equation may be used for the charge within an interval of 0.2 V around the zero voltage point.

The voltage-controlled current source is described by equation **(3.18)**, giving the drain current as a function of two voltages, V_{CGS} and V_{CDS}. The derivatives of the current with respect to these voltages, termed G_m and G_D respectively, would normally be determined analytically from the partial derivatives of equation **(3.18)**. Due to the complexity of the equation, however, it is simpler to obtain these values numerically during the analysis. Furthermore, this allows changes to be made to the equation relatively easily. The size of the voltage increment used in the numerical procedure may be important in determining the accuracy of the analysis and its convergence. Large increments will give inaccurate estimates for the derivatives, while the use of very small values is limited by the numerical precision of the floating point numbers. Voltage increments as small as 2×10^{-8} V have been used successfully with double-precision variables.

In LIBRA, the nonlinear capacitor and current source elements are defined separately. The MOSFET model is then built up in the circuit file using these and standard linear elements. User-defined elements are created by writing code in the C language. Besides several declarations which must be made in the file, the elements are described in separate functions. The element parameters and node voltages are obtained by calling existing functions, allowing the branch currents and pin charges to be calculated. The derivatives of these currents and charges with respect to the node voltages must then be determined. Finally, functions are called to load the currents, charges and their derivatives into matrices. The C code is compiled and linked to the main program.

With MWSPICE, the MOSFET model must be obtained largely by modifying an existing GaAsFET model, with the parasitic series inductances and package capacitances being added in the circuit file. The necessary code is in the form of a FORTRAN subroutine. A number of the elements in the GaAsFET model are not required and must either be deleted from the subroutine or set to negligible values. For example, unwanted series resistances can be specified to be zero in the circuit file's MODEL statement.

5.4 Computer-aided design techniques

The computer-aided analysis and design of RF power amplifiers requires a number of different techniques. Some of these are straightforward and easily implemented in commercially available CAD packages, as shown by practical examples. Other procedures are limited by the capabilities of current software. Solutions to these problems do, however, exist.

5.4.1 General techniques

One of the important characteristics of an RF power amplifier is its input impedance at the fundamental frequency. This is calculated using the voltages across the source resistance, as shown in equation **(5.5)**, with reference to Figure 5.5. Both V_1 and V_2 are vector quantities, specified at the fundamental frequency, and are obtained directly from a harmonic balance analysis. With a time-domain program, the calculation would entail Fourier transformation. Similarly, the DC supply current is obtained easily from harmonic balance as the DC component of current through a small resistance. In the time-domain program, an LC filter (Figure 5.5) is needed to reduce the RF variations. The filter elements must be chosen to provide sufficient smoothing without introducing large time constants, which would increase the required analysis time. Finally, the harmonic balance program LIBRA allows the output power to be determined at the fundamental frequency or any of the harmonics, as well as the total power, which would be measured by a bolometer power meter. These specifications each require only a single short statement in the circuit file. From a time-domain

analysis, the total output power could be determined as the sum of several Fourier transformed harmonics. The program MWSPICE does, however, provide an analysis specifically for the total output power.

$$Z_{in} = \frac{V_2}{(V_1 - V_2)/R_S} \tag{5.5}$$

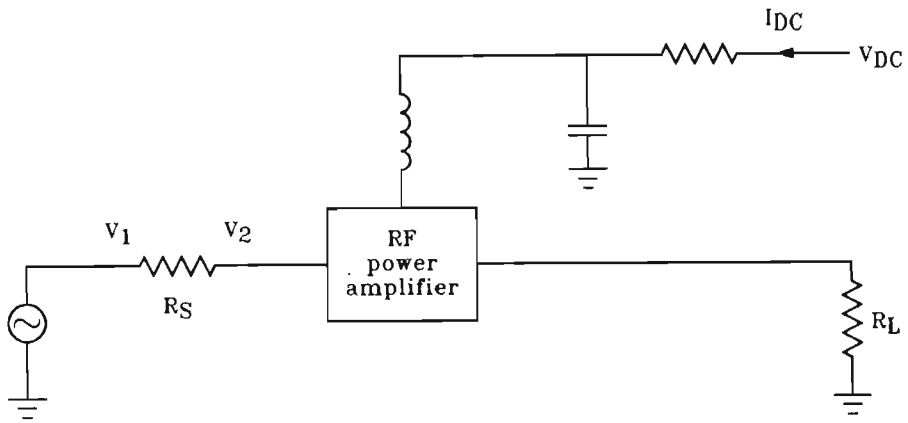


Figure 5.5 Circuit definitions for calculation of amplifier input impedance, supply current and output power

The amplifier input impedance calculation allows any source impedance to be used, including complex values. The source can also be transformed through a matching network to obtain realistic harmonic impedances. Due to the MOSFET nonlinearities, the gate impedance may, for a fixed output power, vary with source impedance .

5.4.2 Amplitude modulation

Amplitude modulated transmitters are used in a wide range of applications, a typical example being commercial light aircraft radios. With MWSPICE, an amplitude modulated signal is naturally expressed in the time domain, using the standard AM equation shown in **(5.6)**. For a harmonic balance program, the AM source must be represented in the frequency domain, using three correctly phased generators. The amplitude and phase of the generators are seen in equation **(5.7)**, which is obtained from **(5.6)** using a trigonometric identity.

Figure 5.6 shows the time and frequency domain generators with 50 Ω source and load impedances. The phase offsets of $3\pi/2$ and $\pi/2$ are required, since only sine generators are used in the CAD program.

$$V_g(t) = V_c(1 + m \sin \omega_m t) \sin(\omega_c t) \tag{5.6}$$

$$V_g(t) = V_c \sin(\omega_c t) + V_c \frac{m}{2} \cos(\omega_c t - \omega_m t) - V_c \frac{m}{2} \cos(\omega_c t + \omega_m t) \tag{5.7}$$

where V_c = constant
m = modulation index
ω_m = modulation frequency (radians/second)
ω_c = carrier frequency (radians/second)

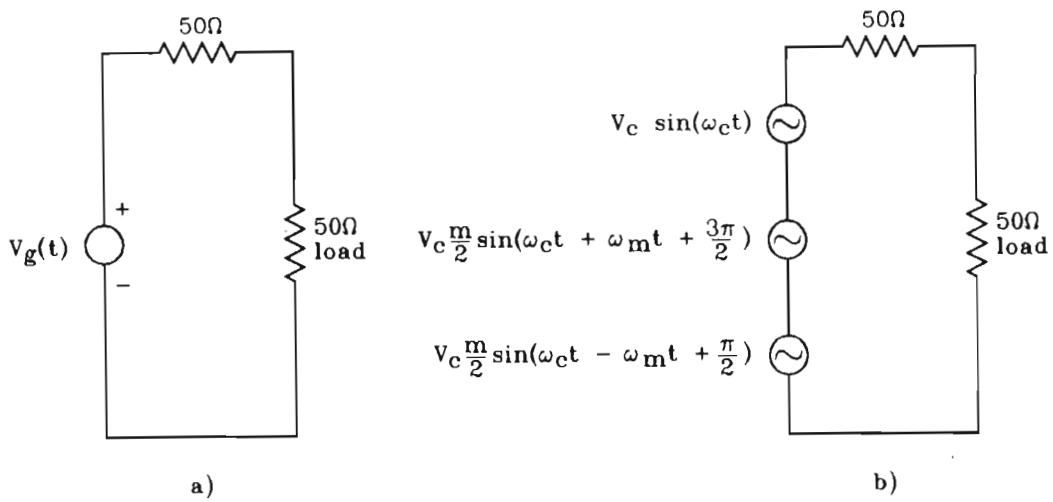


Figure 5.6 Amplitude modulation: a) time domain b) frequency domain

It is convenient to relate the constant V_c to practical measurements of AM signals using the average power delivered into a 50 Ω load. This is a long-term average value, which would be measured by a bolometer power meter. The average power

in the 50 Ω loads of Figure 5.6 can be calculated by summing the contributions of each frequency component in **(5.7)**, as shown in equations **(5.8)** and **(5.9)**.

$$P_{avg.} = \frac{1}{50}\left[\left(\frac{V_c}{2\sqrt{2}}\right)^2 + \left(\frac{V_c m}{4\sqrt{2}}\right)^2 + \left(\frac{V_c m}{4\sqrt{2}}\right)^2\right] \qquad \textbf{(5.8)}$$

$$= \frac{V_c^2}{400}\left(1 + \frac{m^2}{2}\right) \qquad \textbf{(5.9)}$$

An important quantity is the peak envelope power (PEP), which is the RF power at the peak of the modulating signal. If the RF amplifier has insufficient gain at this power level, significant envelope distortion will result. The load PEP in Figure 5.6 is calculated in equations **(5.10)** and **(5.11)**, beginning from **(5.6)** with $\sin \omega_m t = 1$.

$$PEP = \frac{1}{50}\left[\frac{V_c(1+m)}{2\sqrt{2}}\right]^2 \qquad \textbf{(5.10)}$$

$$= \frac{V_c^2}{400}\left(1+m\right)^2 \qquad \textbf{(5.11)}$$

From **(5.9)** and **(5.11)**, the ratio of peak envelope power to the average power is simply a function of the modulation index. For example, with m = 0.8, which is commonly specified, the ratio is 2.455. This allows the rapid calculation of PEP from a measured average value, but only applies if the AM waveform is undistorted.

5.4.3 Stability

It is a necessary design requirement that an RF power amplifier be stable. This is not only to ensure correct signal transmission, but also to avoid radiating power at out-of-band frequencies, which could interfere with other communications.

From a practical viewpoint, three important types of instability can be identified. Firstly, a large-signal oscillation may occur, possibly only limited by the power capabilities of the active device or the DC supply. Secondly, low-level spurious oscillations may appear in the output spectrum. Thirdly, hysteresis may be observed with the output power as the input drive level is raised and lowered, which severely distorts amplitude modulated signals. Since an AM signal causes an amplifier to traverse a wide range of conditions, it is more likely to reveal instabilities than an FM signal, for instance. The antenna impedance of a mobile transmitter will generally have a large and changing VSWR, due to physical constraints on the antenna size and the effect of varying surroundings. An RF power amplifier should remain stable even under severe load-mismatch conditions. Since this is generally achieved at the expense of gain and efficiency, a common specification only requires stability for a VSWR of 3 or less, through all angles of reflection coefficient.

The analysis of amplifier stability can take into account several increasingly rigorous specifications, namely DC, local and global stability. Although DC stability is a necessary condition, it does not include possibly unstable states which may occur during an RF cycle. Local stability implies stable steady-state RF operation around a particular set of conditions, such as drive level, supply voltage and load impedance. Large changes to these operating conditions may lead the circuit into an unstable region and perhaps another stable state. This is observed, for instance, with hysteresis of the output power. Global stability is an all-encompassing term which guarantees amplifier stability over a specified range of operating conditions. By verifying local stability at a large number of operating points, global stability may be presumed with a high degree of confidence, but without certainty. Rizzoli and Neri [1988] describes the use of bifurcation theory to determine the stability of a circuit

in a global sense, without requiring an infinite number of operations. Briefly, a bifurcation is defined as a circuit state for which system stability undergoes an abrupt change, such that the real part of at least one natural frequency changes sign. Bifurcations are located in the parameter space by Nyquist analysis. Since, by definition, circuit stability remains unchanged along branches which do not contain bifurcations, the circuit states are readily classified into stable or unstable regions.

A global stability analysis is not currently possible with the widely available nonlinear analysis programs. Even a single local analysis is difficult, as time-domain programs are slow and a standard harmonic balance simulation does not provide an unambiguous indication of stability. Instead, this must be determined indirectly by noting that a harmonic balance analysis of an unstable circuit will usually fail to converge, show a negative real input impedance or produce unrealistic results. However, these tests are not reliable, since the circuit may be unstable at frequencies other than that of the analysis. The program LIBRA offers an oscillator design facility, which may assist in the problem, since this allows the analysis frequency to vary. Thus, although current CAD programs do not offer a comprehensive solutions to stability analysis, it can be anticipated that suitable techniques will be introduced.

5.4.4 Optimisation

The power of computer-aided design methods lies in their ability to automatically optimise a design in its modelled form. This is a well-established facility with linear CAD programs and a significant reason for their success. Linear circuit optimisation is accomplished using a standard analysis method to generate the circuit response and, hence, an objective function, which is then minimised within an optimisation loop. If, however, the same procedure is employed with nonlinear analysis, the value of the optimisation facility is severely limited by its speed. Even with the harmonic balance method, considerable time is needed to perform the hundreds or thousands of analyses that are often required.

The speed of nonlinear optimisation can be greatly increased through methods which avoid performing a large number of full analyses. For example, with the harmonic balance method, an objective function may be defined as a combination of the harmonic balance and circuit performance requirements. A single optimisation procedure is then performed, which terminates with the harmonics balanced and the circuit-performance objective function minimised. Depending on the number of circuit variables, the entire optimisation should not take significantly longer than a standard circuit analysis. Lipparini *et al* [1982] report a speed improvement of about two orders of magnitude compared to the standard optimisation method. Furthermore, the extra degrees of freedom provided by the circuit variables assist the search for harmonic balance.

Although the method of nonlinear optimisation used by LIBRA is not described in its manuals, it would appear that full analyses are performed within an optimisation loop. Due to the importance of nonlinear optimisation, it is certain that significant improvements will be made in this regard.

Chapter 6

Studies of computer-aided analysis and design

The practical application of computer-aided methods to RF power amplifiers is demonstrated with two different examples. The first describes the computer-aided analysis of an empirically designed amplifier which incorporates ferrite autotransformers in its matching networks. In the second example, an amplifier with LC matching networks is designed using linear and nonlinear analysis programs. The amplifier is constructed and its performance compared to the design objectives. Both amplifiers, which employ an MRF136 MOSFET, have a nominal peak output power of 15 W over the frequency band 118 MHz to 175 MHz, and can be used for FM and AM signals.

6.1 Computer-aided analysis

This section describes the analysis of an amplifier, which is designed empirically using the methods given in section 5.1. Measured and calculated values are compared for a number of important amplifier characteristics over a wide range of operating conditions.

6.1.1 Empirical design and construction

The essential characteristics of an RF power amplifier design are the drain load impedance, stability enhancing elements and the input matching network. Initial values for the design in this section are based on a test circuit given in the MRF136 data sheet. This has a 27 Ω gate shunt resistance to ensure stability and optimum source and load impedances which are given as large-signal impedance data. Additionally, equation **(5.2)** is used to estimate the required drain load impedance.

It is seen in Table 6.1 that equation **(5.2)** yields higher values of drain load impedance than the narrowband test circuit of the device data sheet. Furthermore, the imaginary part of the load impedance increases with frequency for equation **(5.2)**,

whereas the corresponding data sheet values decrease. Experiments show that the lower values of impedance magnitude generally result in greater amplifier gain but degrade amplifier stability.

Table 6.1 Values of drain load impedance: equation **(5.2)** and data sheet
Equation **(5.2)** assumes: V_S = 28 V, P_{out} = 15 W, V_{DSon} = 2.3 V, C_{oss} = 27 pF. 'Data sheet' values at 118 MHz and 175 MHz are interpolated from the MRF136 data sheet.

Frequency (MHz)	118	150	175
Z_L (Ω) Eqn. **(5.2)**	18.4 + j8.1	16.8 + j9.4	15.4 + j10.1
Z_L (Ω) Data sheet	12.0 + j16.3	9.1 + j15.4	6.9 + j12.2

With relatively low values of drain load impedance, various instabilities are observed. These range from spurious outputs in the spectrum, particularly at low input power levels, to hysteresis of the output power for changing drive levels. While this can be prevented by decreasing the gate shunt resistance, the amplifier gain may be reduced considerably. No advantage was obtained by the use of resistive feedback from drain to gate. The design philosophy is therefore to use moderately high values of drain load impedance and gate shunt resistance. Additional stability is obtained with a shunt capacitance from gate to ground. Although the potential amplifier bandwidth is reduced, this is unimportant for the frequency range considered.

The desired form of drain load impedance can be obtained with a ferrite autotransformer, shunt capacitance and series inductance, as shown in Figure 6.1. Table 6.2 gives the measured impedance of this network. The Smith chart of Figure 6.2 shows the development of the drain load, with the impedances, Z_a, Z_b and Z_c defined in Figure 6.1. Z_a and Z_c are measured values, while Z_b is calculated from the component impedances. A trimmer capacitor is used, which results in a relatively large parasitic series inductance for the shunt capacitance.

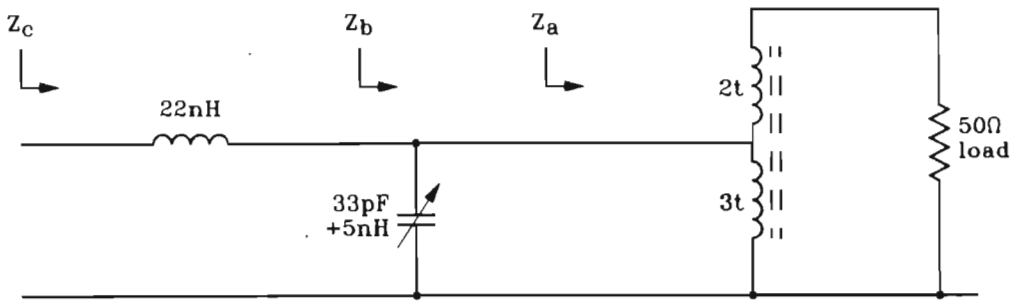


Figure 6.1 Amplifier output matching network

Table 6.2 Measured impedance into output matching network

Frequency (MHz)	118	150	175
Z_c (Ω)	19.4 + j11.0	16.9 + j12.3	13.6 + j14.7

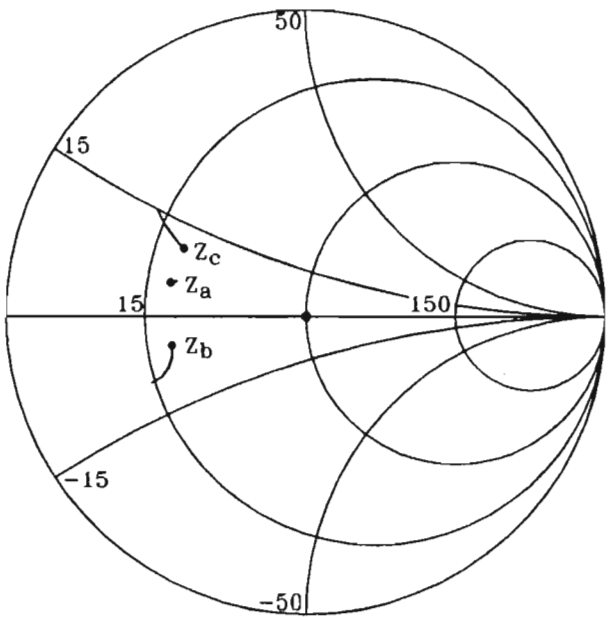


Figure 6.2 Development of drain load impedance

For stabilisation, a 22 Ω gate shunt resistance is chosen, which provides greater stability than the 27 Ω value of the MOSFET data sheet, with minimal loss of gain. Additionally, a suitable value of shunt capacitance is found to be 27 pF.

As the input impedance of the amplifier is strongly affected by the drain load impedance and stabilising elements, the data sheet values of large-signal input impedance are not used directly. However, it can be noted from the device data sheet that the source impedance for the gate is of similar form to the drain load but requires a greater impedance transformation ratio. A suitable input matching network comprises an autotransformer followed by a series inductance, shunt capacitance and series inductance, as shown in the amplifier circuit diagram of Figure 6.3. The autotransformer increases the impedance level to near 50 Ω. For an input power of 1.1 W, this impedance has a large, inductive reflection coefficient at the high-end frequency of 175 MHz. The series inductor L_3 and shunt capacitance C_1, C_2 rotate the impedance trace on a Smith chart, forming a semi-circle. This is centred around the 50 Ω point with the series inductance L_1. The inductor L_2 in parallel with the shunt capacitors reduces the effective capacitance at low frequencies, thus enhancing the curvature of the impedance trace.

The final amplifier design is shown in Figure 6.3. The input and output matching networks are adjusted to provide maximum flat gain over the frequency band, with minimum input VSWR, for an input power of 1.1 W. This procedure uses the measurement setup shown in Figure 5.3. Figure 6.4 gives the physical layout of the amplifier. This is built on plain printed circuit board, which forms a continuous groundplane, with the MOSFET bolted to a large heatsink underneath. Plate ceramic capacitors are used for matching, de-coupling and DC blocking purposes. Trimmer capacitors allow fine adjustment of the amplifier performance. The inductors are air-cored and wound with enamelled copper wire. It is important to note that the metal−film resistors used are not cut spirally. Rather, they consist essentially of a cylinder of resistive material, resulting in relatively low series inductance. The autotransformers employ ferrite balun cores and enamelled copper wire.

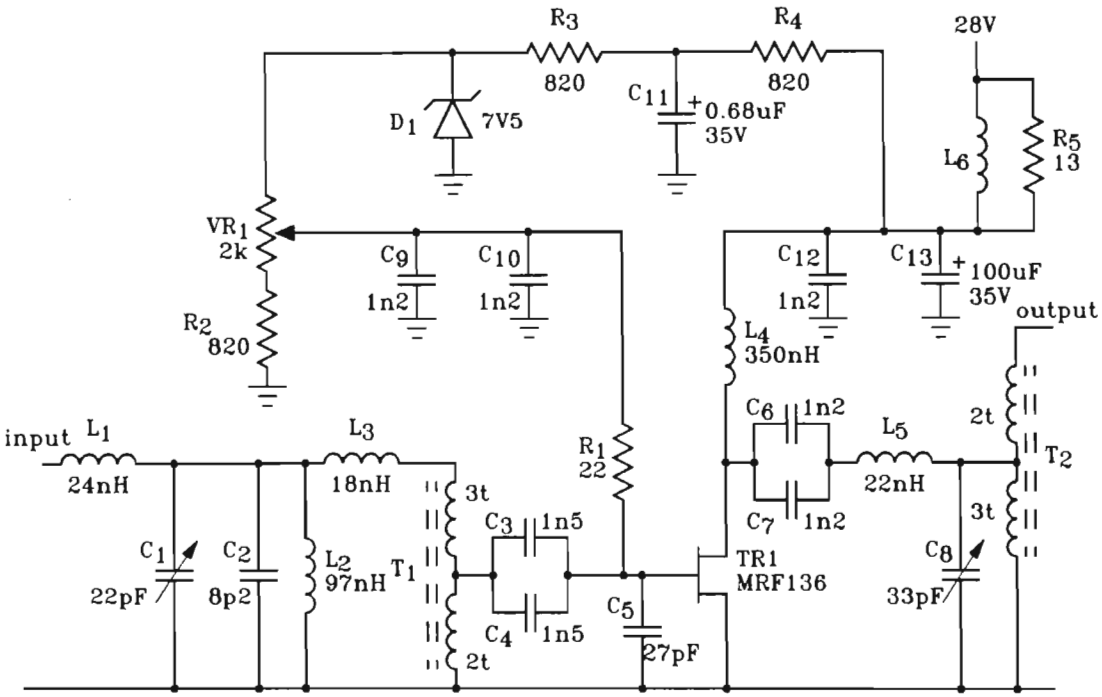


Figure 6.3 Amplifier circuit diagram

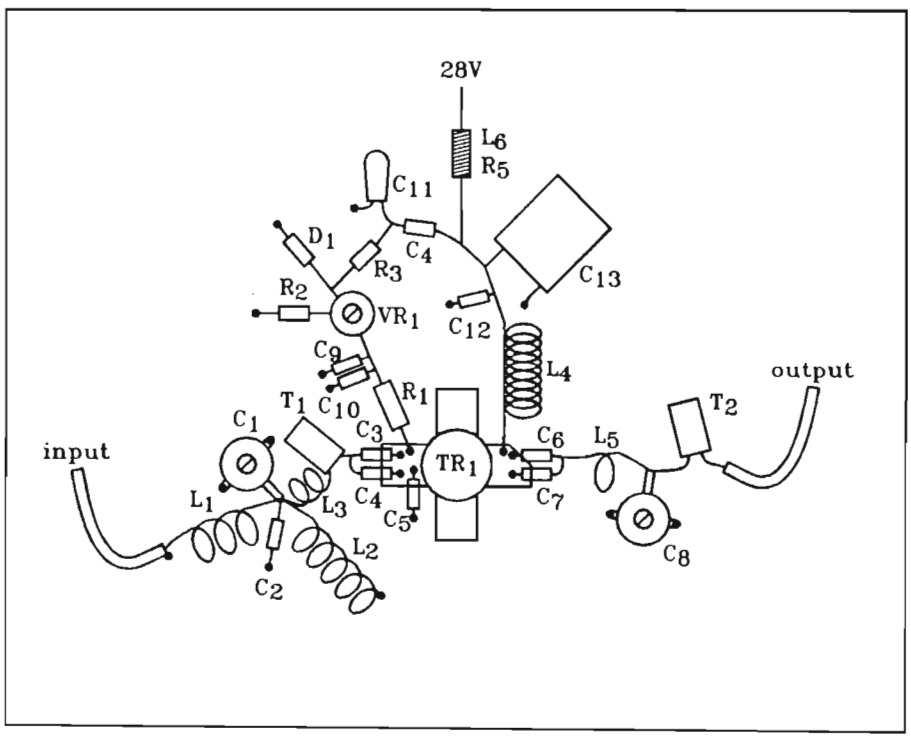


Figure 6.4 Physical layout of amplifier (approximately to scale)

For an input power of 1.1 W and frequency range of 118 MHz to 175 MHz, the measured output power of the amplifier varies from 14.9 W to 15.5 W, with a maximum input VSWR of 1.6. The stability of the amplifier is evaluated for a variety of source and load impedances. With a 50 Ω load, the amplifier is stable for short-circuit, open-circuit, inductive and capacitive source impedances. The amplifier oscillates if the output is open or short-circuited. However, with such loads padded by a 3 dB attenuator, which gives a VSWR of 3, the amplifier is stable.

6.1.2 Analysis procedure

The amplifier shown in Figures 6.3 and 6.4 is analysed using the time-domain program MWSPICE and the harmonic balance program LIBRA. The model used for the MRF136 MOSFET is described in chapters 1, 2 and 3. It is important to note that this MOSFET model is extracted for a different device, of the same type, to that used in the physical amplifier. This was done to avoid damaging the modelled device and to demonstrate the results that are possible with a model which is extracted for another device of the same type. Models for the passive components are described in chapter 4. The autotransformers are assumed to be linear. Due to the upper frequency limit of the automatic network analyser, the passive component models are only fitted at frequencies within the amplifier operating band, namely 118 MHz, 150 MHz and 175 MHz. In several instances, two distinct components are modelled as one element. For example, C_1 and C_2 are measured and modelled together, resulting in a single capacitive element with parasitic series inductance. Similarly, the capacitors C_3, C_4 and C_6, C_7 are combined. Although the modelling accuracy is reduced, for example due to differing series inductances, this requires less time for measurement and modelling. A number of simplifications are made in modelling the amplifier circuit, apart from those inherent in the component models. The capacitors C_9, C_{10}, C_{12} and C_{13} are assumed to have zero impedance, as the impedances of R_1 and L_4 are comparatively large. Thus, in the circuit model, R_1 and L_4 are driven from ideal voltage sources. Also, the impedance of the groundplane is assumed to be negligible. Calculations [Ramo *et al*, 1984] indicate that the groundplane impedance will have only a small effect at frequencies in the region of 150 Mhz.

The computer used for the analysis is a SUN IPC workstation. Due to the slow speed of the time-domain program when used for steady-state analysis, the results to be presented are obtained from the harmonic balance program. However, the predictions of the two programs are verified to be close for parameters such as output power, DC supply current and harmonic outputs. A factor in this comparison is that time-domain analyses need to run for impractical lengths of time in order to accurately calculate the steady-state response. Typically, the time required for a steady-state analysis, with a single-frequency source, is 15 minutes for the time-domain program and 4 seconds for the harmonic balance program. The analysis time is considerably increased for AM signals to several hours and 15 minutes respectively. Except for the AM case, the results are obtained rapidly from the harmonic balance program. This gives all the required outputs (load power, DC supply current, input impedance and harmonic outputs) from a single analysis at each of a number of specified frequencies.

6.1.3 Results

The following results compare the predictions of the computer-aided analysis to measurements of the physical amplifier shown in Figures 6.3 and 6.4. In all cases, the supply voltage is 28 V, the MOSFET quiescent current is 25 mA and the amplifier source and load impedances are 50 Ω. Owing to the size of the heatsink used, the MOSFET case temperature is near to 27 °C for all measurements. The MOSFET channel temperature is expected to be between the heatsink temperature and about 75 °C, depending on the drive level and frequency. For the nominal output power of 15 W, the channel temperature is approximately 60 °C, which is near to the 70 °C temperature at which the MOSFET is modelled.

Figures 6.5 to 6.8 compare several amplifier characteristics for a fixed input power of 1.1 W, over the frequency range 118 MHz to 175 MHz. Figure 6.5 gives the total RF power dissipated in the 50 Ω load, including the harmonics. The DC current in Figure 6.6 is that flowing through the MOSFET drain supply choke and excludes the current required for the gate bias network, which is approximately 11 mA.

Figure 6.7 shows the input impedance of the amplifier. This is measured using the method described in section 5.1.3, with the calibration plane being defined at the input side of L_1 in Figure 6.4. The output harmonic levels, relative to the fundamental, are given in Figure 6.8.

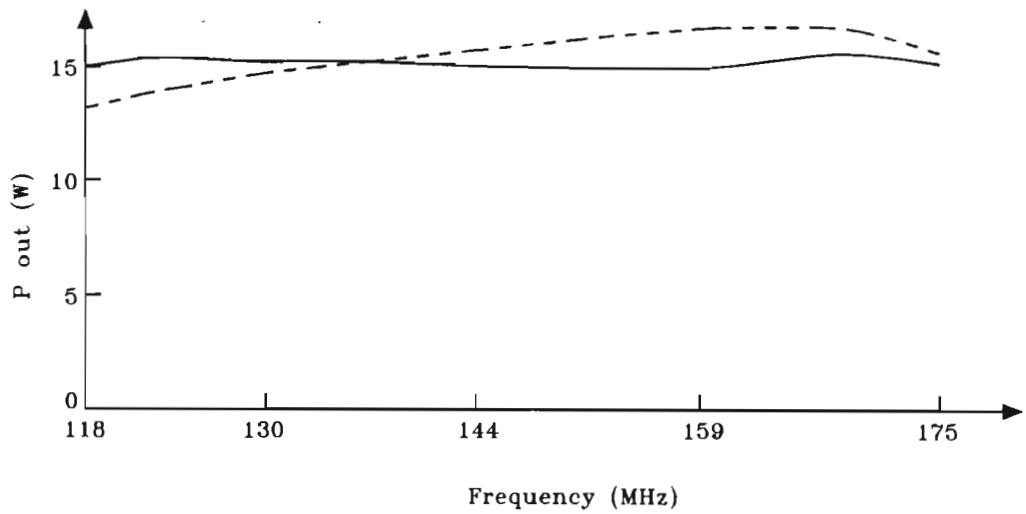


Figure 6.5 Amplifier output power versus frequency for P_{in} = 1.1 W
——— (measured) - - - - (calculated)

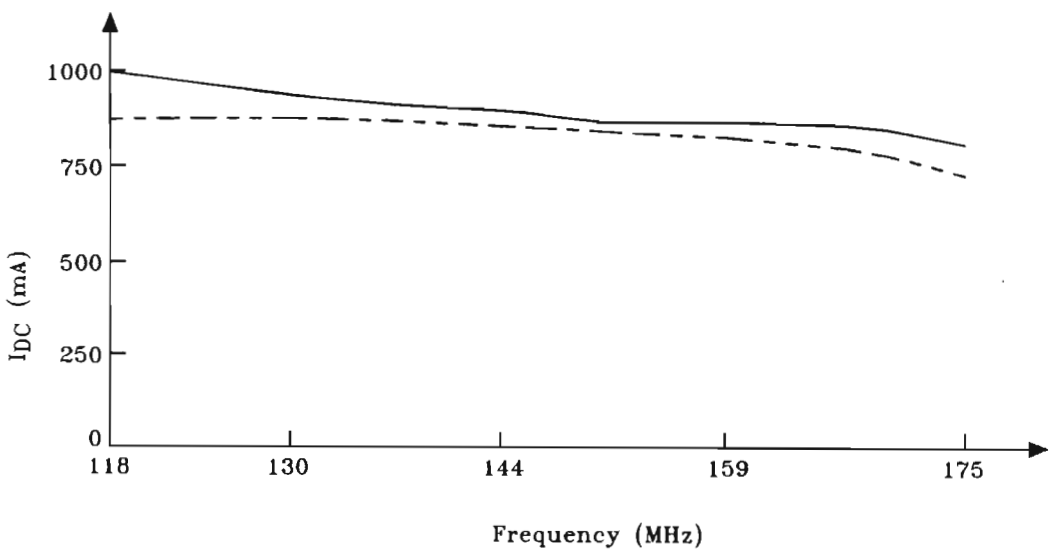


Figure 6.6 DC drain supply current versus frequency for P_{in} = 1.1 W
——— (measured) - - - - (calculated)

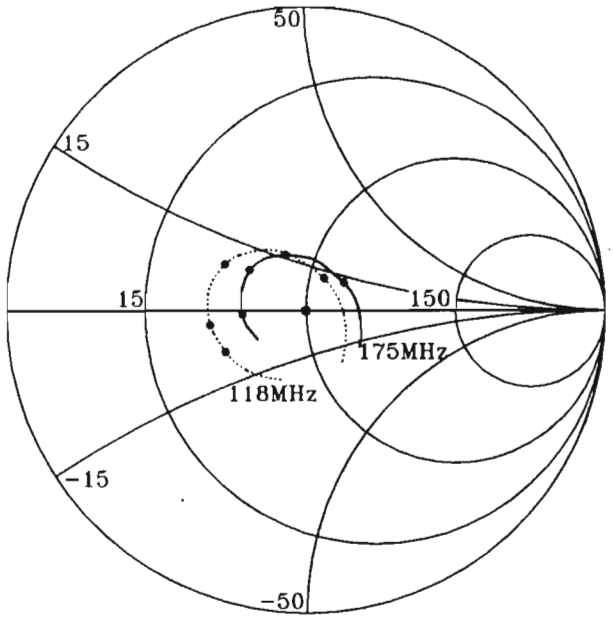


Figure 6.7 Amplifier input impedance versus frequency for P_{in} = 1.1 W
——— (measured) - - - - (calculated)

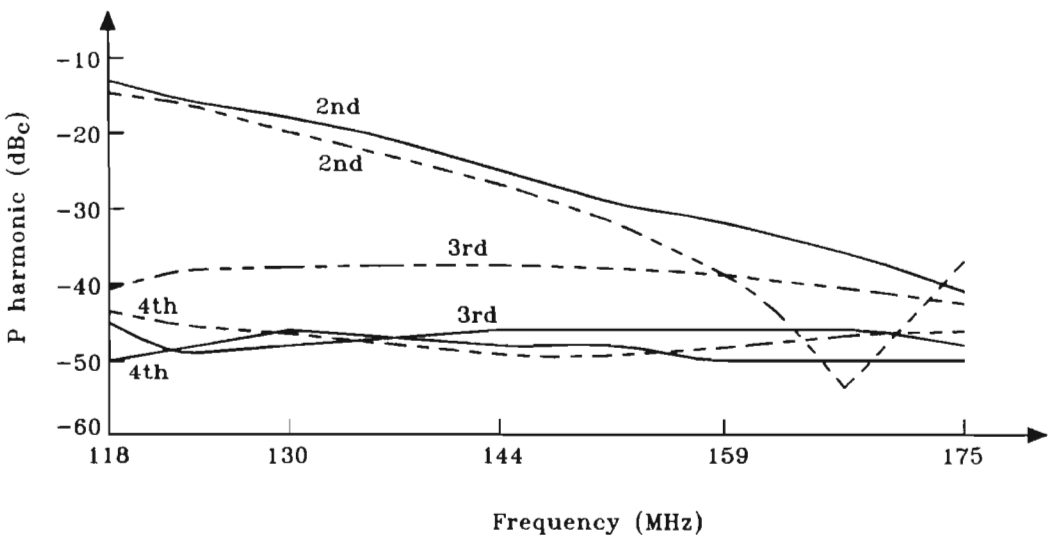


Figure 6.8 Output harmonics relative to fundamental : P_{in} = 1.1 W
——— (measured) - - - - (calculated)

Figures 6.9 to 6.11 compare measured and calculated values of output power, DC drain supply current and amplifier input impedance at 150 MHz, for a range of input powers.

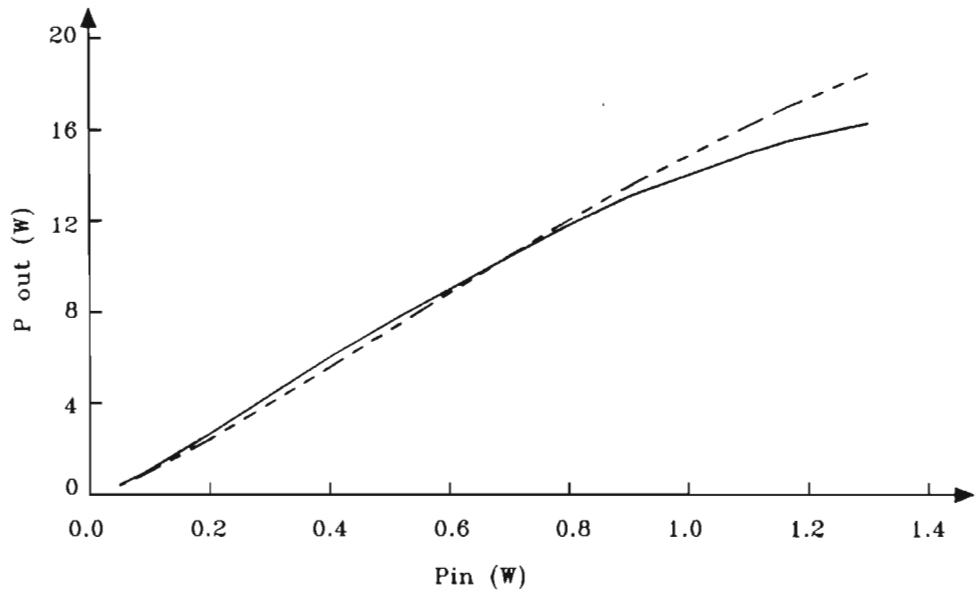


Figure 6.9 Amplifier output power versus input power at 150 MHz

——— (measured) - - - - (calculated)

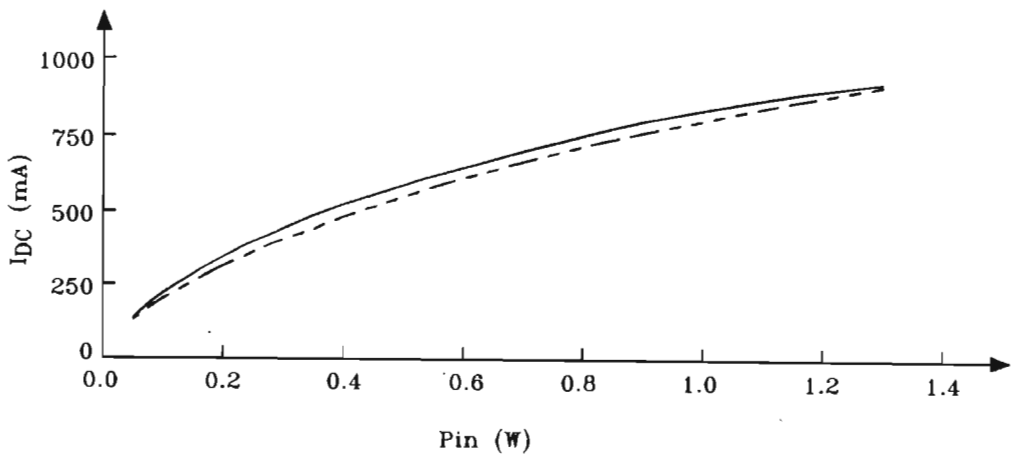


Figure 6.10 DC drain supply current versus input power at 150 MHz

——— (measured) - - - - (calculated)

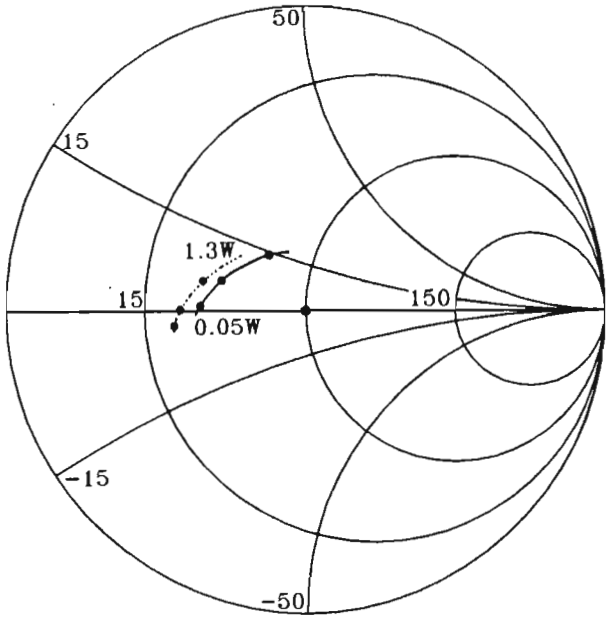


Figure 6.11 Amplifier input impedance versus input power at 150 MHz
——— (measured) - - - - (calculated)

Table 6.3 compares measurements and calculations for the average power of an amplitude modulated signal with a carrier frequency of 150 MHz and modulation index of 0.8. A modulation frequency of 40 kHz is used to allow easy observation of the AM spectrum and to reduce the analysis duration with a time-domain program.

Table 6.3 Average output power and DC drain supply current versus average input power for an AM signal at 150 MHz (m = 0.8)

P_{in} avg. (W)	0.1	0.4	0.8
P_{out} avg. (W) meas.	1.23	6.0	9.6
P_{out} avg. (W) calc.	1.167	5.81	10.92
Error	-5.1 %	-3.3 %	13.7 %
I_{DC} (mA) meas.	200	456	617
I_{DC} (mA) calc.	194	461	681
Error	-2.9 %	1.0 %	10.4 %

From the given results, it is seen that the amplifier output power and DC drain supply current are accurately calculated. For example, the maximum error is less than 12 % in Figures 6.5 and 6.6 and less than 9 % in Figure 6.10. In Figure 6.9, the output power prediction diverges above the measured value for high input powers. This is believed to result from the particular MOSFET model used. To minimise the danger of destroying the device, the drain current characteristics were not measured at levels greater than 1 A for large drain voltages. The MOSFET drain current equation therefore represents the high dissipation region poorly. This problem can easily be corrected in future work. A similar effect is seen with the average AM output power prediction in Table 6.3. For an average input power of 0.8 W, the peak input power is 1.96 W. Since the gain at high power levels is overestimated, the average output power prediction is accordingly too high. The output harmonic levels in Figure 6.8 are not expected to be accurately predicted for the given example. As the passive components are modelled from measurements within the fundamental frequency range only, the matching network impedances are not well characterised at the higher harmonic frequencies. Finally, the amplifier input impedance calculations in Figures 6.7 and 6.11 show maximum errors of 40 % with an average of 31 %. In section 3.3, the input impedance of the MOSFET, mounted in a well characterised test fixture, is predicted with errors of between 11 % and 23 %. In section 4.3.2, the errors in predicting the impedance into a LC matching network range between 7 % and 28 %. The amplifier input impedance errors can therefore be attributed equally to the MOSFET and matching network models.

6.2 Computer-aided design

In this section, an amplifier is designed using linear and nonlinear analysis programs. This has similar specifications to the previously described amplifier, but uses only LC elements in its matching networks.

6.2.1 Design procedure

The amplifier which is designed is single-ended and employs an MRF136. The required performance specifications are as follows. Over the frequency band of 118 MHz to 175 MHz, and for a nominal output power of 15 W, the amplifier is to have maximum flat gain and a low input VSWR. Also, the amplifier should be stable over all operating conditions with a load VSWR of 3 or less. This must be achieved with a supply voltage of 28 V and a MOSFET quiescent current of 25 mA.

The chosen design strategy involves several steps. Firstly, an output matching network is synthesized to present an impedance to the drain which is estimated to result in an output power of 15 W across the frequency band. Secondly, a stabilisation method is chosen. Suitable topologies and component values can be determined by computer analysis with simple input matching networks or based on empirical knowledge. Thirdly, the impedance into the gate and stabilisation network is calculated over the frequency band. A matching network is designed to transform this impedance to the desired amplifier input value. Fourthly, a nonlinear optimisation is performed with selected component values in order to achieve the desired circuit specifications. This includes setting the capacitors to preferred values. Lastly, the amplifier is constructed from the computer-aided design and small adjustments made to maximise its performance.

The estimates for the required drain load impedance are given in Table 6.4. These values are an empirically based combination of the MOSFET data sheet values and those of equation **(5.2)** in Table 6.1, with greater emphasis being placed on equation **(5.2)**. Table 6.4 also gives the values of impedance calculated for the output

matching network in Figure 6.12. This network is obtained by approximate calculations using a Smith chart, followed by an optimisation procedure which yields network impedances close to the desired values. The optimisation is performed with fixed component parasitics, which are based on previous measurements. In this example, inductors are assumed to have a parallel capacitance of 0.25 pF and capacitors to have a series inductance of 2.8 nH.

Table 6.4 Estimated values for the required drain load impedance and calculated network values

Frequency (MHz)	118	130.2	143.7	158.6	175
Z_L (Ω) Required	17+j11	16+j11.5	15+j12	13.5+j12.5	12+j13
Z_L (Ω) Calculated	15.5+j11.0	16.6+j11.2	16.1+j11.2	14.1+j12.0	11.4+j14.2

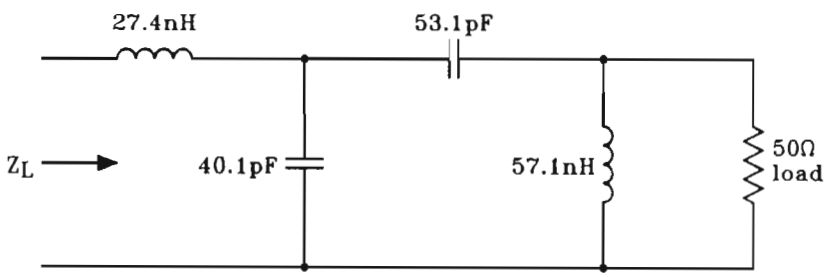


Figure 6.12 Output matching network with optimised component values.

The method of stabilisation employed is that of shunting the gate to ground with resistive and capacitive elements. Based on previous experience, initial values of 22 Ω and 22 pF are chosen. These initial values are not critical, as they can be changed later in the design if required. A series inductance of 6 nH is assumed for the 22 Ω resistor.

A harmonic balance analysis is used to determine the impedance into the MOSFET gate and stabilising elements, with the MOSFET drain connected to the output matching network and 50 Ω load. Since the gate impedance is a strong function of drive level, it is important to ensure that the output power at each frequency is approximately equal to the nominal value of 15 W. Due to the nonlinearity of the MOSFET, the required input impedance is most accurately calculated with a realistic, complex source impedance, as would result from a suitable input matching network. However, this is a minor effect and the use of a resistive source is simpler. In this example, a 12 Ω source is used, since this is approximately equal to the magnitude of the gate input impedance. Due to the input mismatch, a source with an available power of 1.4 W is required to obtain an output power near to 15 W. Table 6.5 gives the resulting values of input impedance and output power.

Table 6.5 Calculated impedance into MOSFET gate and stabilising elements

Frequency (MHz)	118	130.2	143.7	158.6	175
Z_G (Ω)	9.5-j8.8	8.3-j8.2	7.5-j7.8	6.4-j7.6	4.6-j6.4
P_{out} (W)	15.0	15.5	15.3	15.5	15.1

The input matching network must transform the impedances in Table 6.5 to near 50 Ω. A suitable network is shown in Figure 6.13. This is developed on a Smith chart and, with component parasitics incorporated, optimised using a linear-circuit program to give an input VSWR near to unity. The use of three LC pairs in the network gives a significantly lower VSWR than is obtained with only two LC pairs. For the network in Figure 6.13, given the impedance Z_G in Table 6.5, the maximum calculated input VSWR is 1.1.

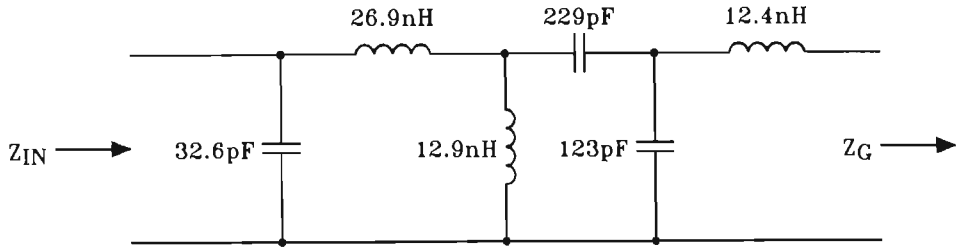


Figure 6.13 Input matching network with optimised component values

The complete amplifier consists of the MRF136 MOSFET, the output and input matching networks of Figures 6.12 and 6.13, the gate shunt loading elements and a large air-cored inductor to supply the drain. For the computer-aided analysis and optimisation, ideal DC power supplies are employed, with the gate voltage supplied through the 22 Ω gate shunt resistance. The performance of the amplifier is calculated for an input power of 1.1 W. Over the frequency band, this yields an output power of between 15.6 W and 16.9 W with a worst input VSWR of 1.37.

The nonlinear optimisation of the amplifier is performed using a gradient optimisation routine within a harmonic balance program. The objective function is defined so as to achieve an output power of 15 W with minimum input VSWR for an input power of 1.05 W. Both least-squares and minimax formulations are used in this example. However, the minimax is preferred, as the worst performance deviations are considered to be more important than the average. Only the primary LC matching element parameters of the input and output matching networks are allowed to vary, while their parasitics and all other components are fixed. A significant problem is that of harmonic balance nonconvergence, even though the particular circuit can be analysed and shows no signs of instability. This is avoided by relaxing the specification for the required accuracy of the solution during optimisation. Near the end of the optimisation, the matching network capacitors are fixed at the nearest preferred values. The remaining variable components are then re-optimised to compensate for the changes which occur. Owing to the non-optimum values of capacitance, the amplifier performance is slightly degraded. The final optimised circuit design is shown in Figure 6.14, with the same DC bias network as that used in the empirically designed amplifier.

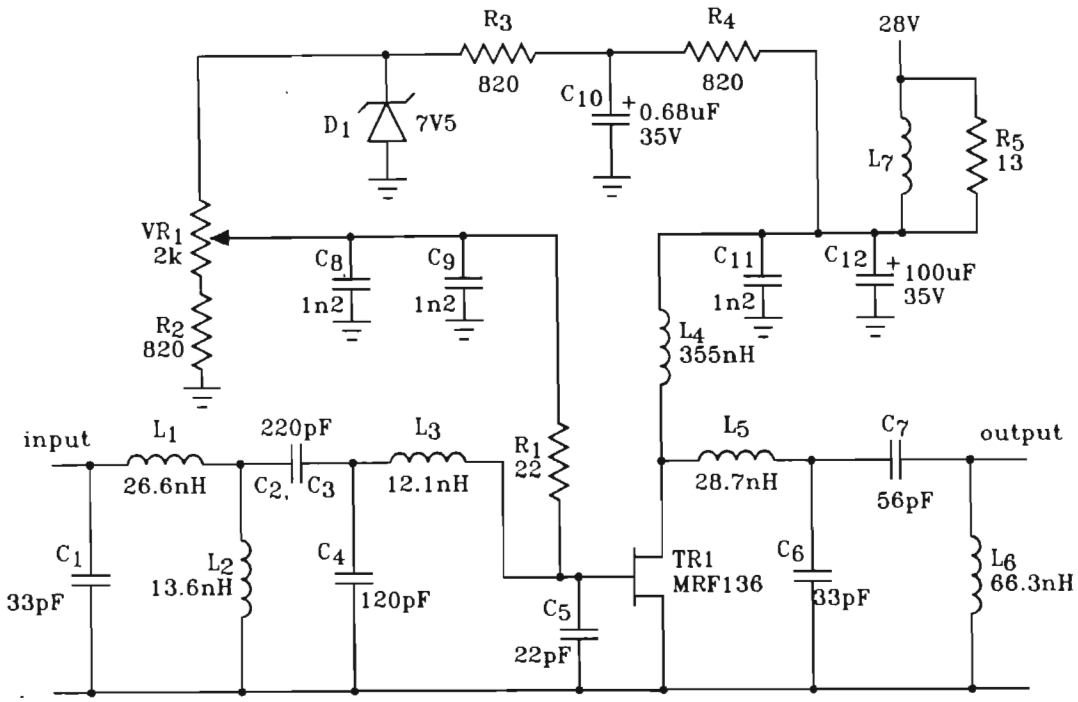


Figure 6.14 Optimised amplifier design with practical DC bias network

6.2.2 Construction of amplifier and initial performance

All the passive components are chosen prior to beginning construction of the amplifier. This is done by comparing the measured impedances of each component to those specified in the design. The desired impedance of each component is a function of both the primary component characteristics and parasitics. Accordingly, a components impedance must be verified, at several widely spaced frequencies. In this case, due to the upper frequency limit of the automatic network analyser, comparisons are made at 118 MHz, 150 MHz and 175 MHz only. The plate ceramic capacitors used are not specifically selected but merely verified to be approximately correct. Thus, the impedances of some of the capacitors are in error by between 3.5 % and 6 %. As the series inductance of a single 220 pF plate ceramic capacitor is excessive, two capacitors, of values 120 pF and 100 pF are used in parallel. The air-cored inductors are adjusted to give the desired impedances. For these components, impedance errors of less than 1 % are obtained readily. The leads of

the gate shunt resistor are merely cut to minimum length, corresponding to a previously characterised component, and are not adjusted to obtain accurately the series inductance in the computer design.

The amplifier construction is shown in Figure 6.15 and is similar to that seen in Figure 6.4, using the same bias network. The circuit is laid out according to the design shown in Figure 6.14. No further impedance measurements are made and the components are used, unmodified, from the procedure described above.

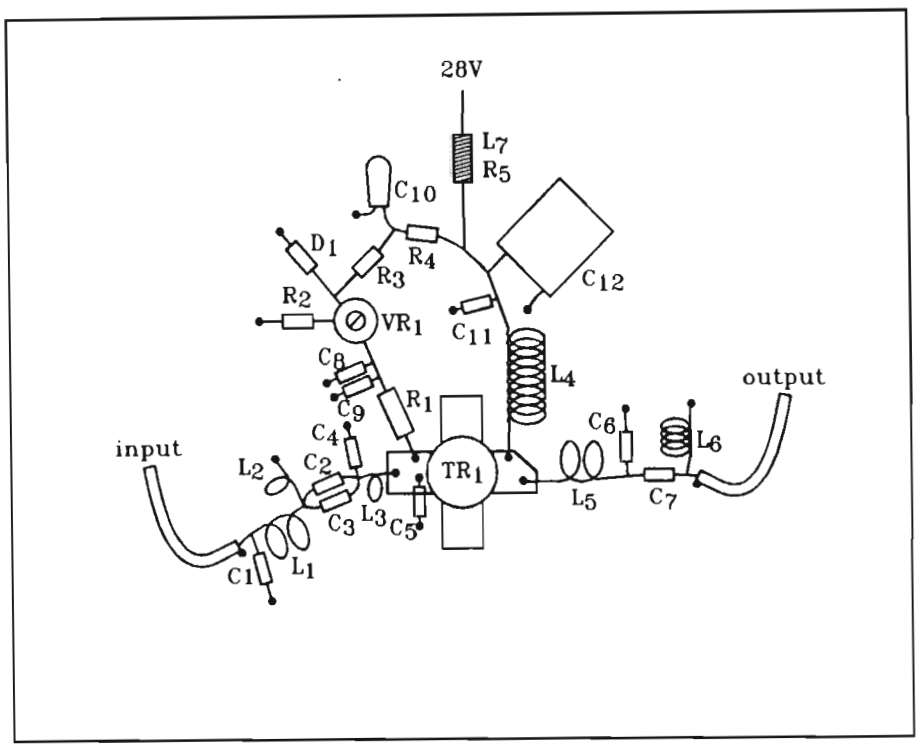


Figure 6.15 Physical implementation of amplifier design (approximately to scale)

The characteristics of the amplifier are measured using the equipment setup in Figure 5.3. Besides checking the performance of the amplifier against the stated design objectives, measurements show stable operation over a wide range of input power levels and frequencies. Stability is also observed for a load VSWR of 3. Figure 6.16 gives the measured output power of the amplifier, as built directly from the computer-aided design, for an input power of 1.05 W. This shows a minimum output power of 12.2 W with a maximum of 15.9 W. The largest error between

measured and calculated output powers is 20 % at 158.6 MHz. In Figure 6.17, it is seen that the input VSWR is small in the lower half of the frequency band but degrades to 2.9 at 175 Mhz, where the error in calculated input impedance is 84 %.

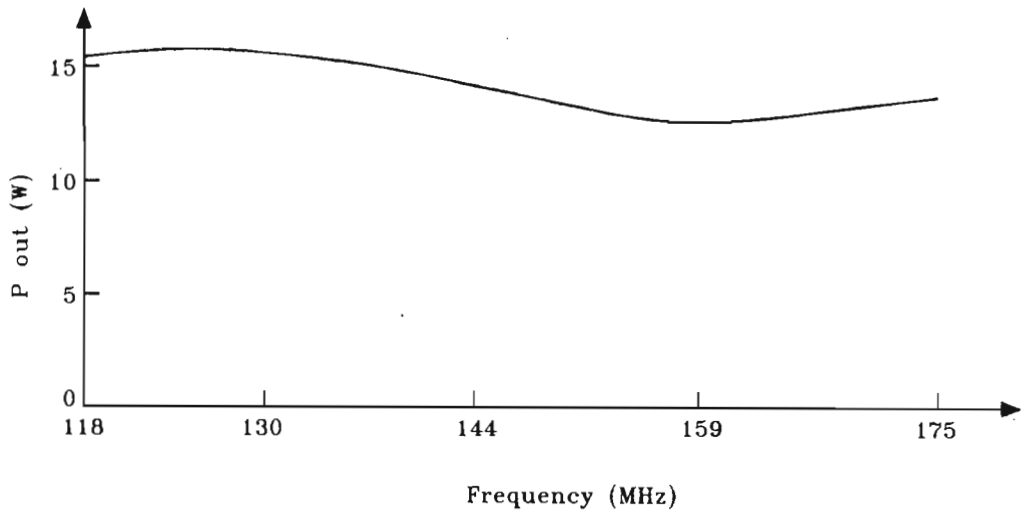


Figure 6.16 Measured output power versus frequency for initial amplifier construction: P_{in} = 1.05 W

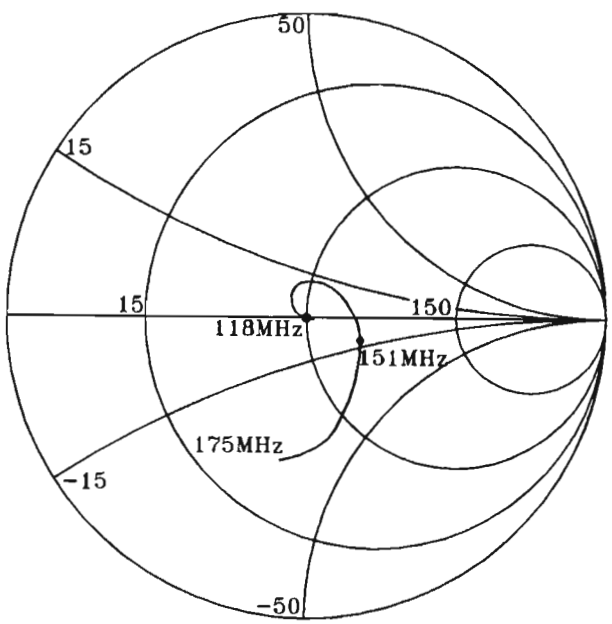


Figure 6.17 Measured input impedance versus frequency for initial amplifier construction : P_{in} = 1.05 W

6.2.3 Amplifier adjustments and results

In Figures 6.16 and 6.17, it is seen that the performance of the amplifier, as built directly from the computer-aided design, is good in the lower half of the frequency band, but degrades significantly at higher frequencies. From inspection of Figure 6.17, it can be noted that the impedance trace at high frequencies corresponds to a shunt capacitance at the amplifier input. Accordingly, the amplifier input VSWR is greatly improved by substituting a 27 pF capacitor for C_1 in Figure 6.14, which has a design value of 33 pF. Small adjustments are made to the inductors L_1, L_2 and L_3, by lengthening or shortening their windings. However, C_1 is the only component which is replaced. Under these restrictions, the amplifier is rapidly adjusted to provide acceptable performance, as seen in Figure 6.18 and Figure 6.19, which shows a worst input VSWR of 1.7. Additional measurements are made at the frequencies 118 Mhz, 150 MHz and 175 MHz, with input powers from 0.05 W to 1.3 W. These indicate a smooth progression of output power with drive level, which is important for amplitude modulated signals. Of all the measurements made at these frequencies and drive levels, the worst input VSWR is 1.8, which occurs at 150 MHz with an input power of 0.05 W.

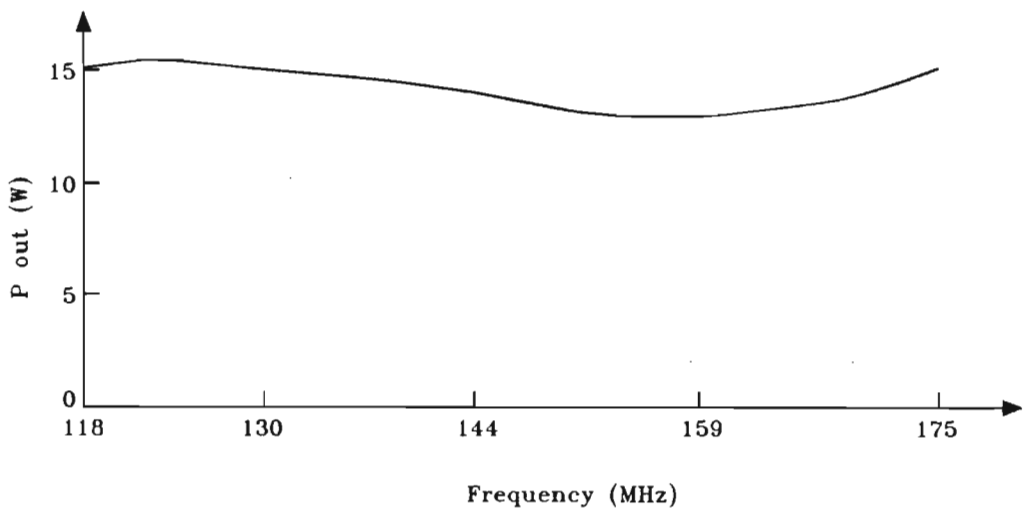


Figure 6.18 Measured output power versus frequency for amplifier after adjustment: P_{in} = 1.05 W

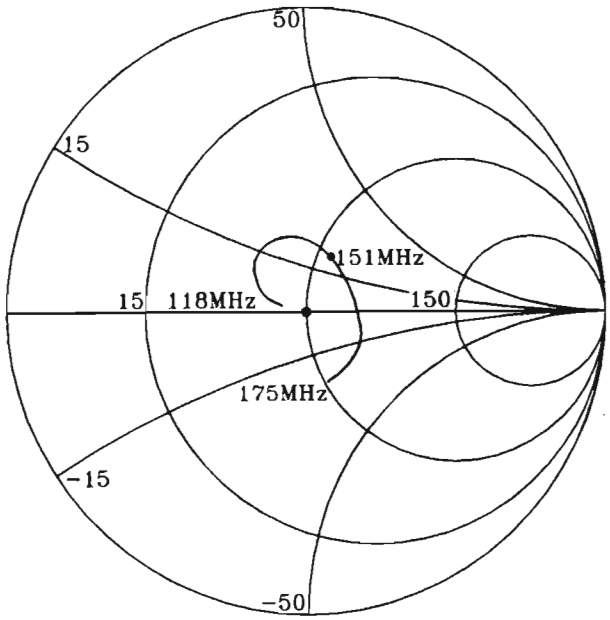


Figure 6.19 Measured input impedance versus frequency for amplifier after adjustment : P_{in} = 1.05 W

There is a large difference between the accuracy of predictions for the amplifier in section 6.1 and this example. In section 6.1, each component is accurately characterised at the fundamental frequencies of the amplifier. For the computer-aided design, average values are assumed for the parasitics and component tolerances are not considered. It is seen in section 4.3 that, even with accurately characterised components, large network impedance errors can occur, due to variations in series lead inductances and other effects.

One method of improving the performance of an amplifier constructed from a computer-aided design is to adjust components so that the network impedances fit those of the computer simulation as closely as possible. However, this technique is limited, as usually only air-cored inductors may be adjusted. Other circuit variables, such as parasitics, are largely fixed by the circuit layout. A refinement to the described design process is therefore proposed.

6.2.4 Modified design philosophy

The proposed design procedure includes two additional steps which are performed prior to the construction of the amplifier. These are to accurately characterise the selected physical components and, using these models, re-optimise the amplifier design. Because accurate component models are used in the final optimisation, the performance of the constructed amplifier will be close to that of the computer-aided design, and only small empirical adjustments may be required.

The complete modified design procedure is as follows. Firstly, an output matching network is designed using linear techniques, to give a drain load impedance which will result in approximately the required output power. Secondly, initial stabilisation networks are chosen, based on computer analysis or practical experience. Thirdly, the input impedance of this circuitry is calculated, using harmonic balance analysis, with the correct output power. Linear synthesis and optimisation programs are used to design a network which transforms this impedance to the desired input value. Fourthly, a nonlinear optimisation of the complete circuit is used to obtain the required performance, with capacitors set to preferred values. Fifthly, physical components are selected for the elements in the computer design and measured both individually and as the designed networks. Models are extracted for each component from the individual measurements. Also, unknown variables, such as lead inductances, may be found by fitting the network models to the measurements. The use of these more accurate component models will normally change the calculated amplifier performance. The penultimate step is thus to perform a second nonlinear optimisation, allowing only some of the component values to change. As the components from this second optimisation will be similar to those previously characterised, the extracted parasitics remain valid. Finally, the amplifier is

constructed using the optimised component values. Due to the residual modelling errors, small component adjustments may be required in order to match the amplifier performance to the design values.

The advantage of the proposed method is that only slight adjustment of the constructed amplifier would be required, leaving the actual circuit optimisation to be done by computer. This is more efficient and powerful than empirical optimisation of a physical circuit, where generally, only one of a limited set of circuit variables can be changed at a time. The technique of optimising only one variable at a time will often not result in the best solution to a problem. The proposed method of computer-aided design thus advocates a continuous interaction between computer simulation and the physical circuit. This, it is believed, will lead to RF power amplifiers with better performance than those which are designed using empirical methods only.

Discussion and conclusions

The computer-aided analysis and design of RF power MOSFET amplifiers is investigated. Modelling procedures are developed for high power RF MOSFETs, as well as for passive components such as resistors, inductors, capacitors and ferrite transformers. Empirical design methods are reviewed and a number of techniques used in computer-aided design are discussed. A 15 W RF power amplifier is analysed using the described modelling procedures and, finally, an amplifier is designed using computer-aided techniques.

It is seen that high power RF MOSFETs have several characteristics which restrict the use of modelling techniques that have been applied to microwave GaAsFETs and other relatively low power devices. A modelling procedure, which is applicable to RF MOSFETs of any power level, is therefore proposed. This is based on the exclusive use of cold S parameters, with $V_{GS} = 0$, and pulsed drain current measurements. As instabilities are not possible, the MOSFET can be connected directly to an ANA, and there is no device heating. The drain current characteristics can be determined at specific device temperatures for high dissipation levels using a pulsed measurement technique. The model parameters are identified in two distinct steps. Firstly, the linearised model is fitted to S parameters measured at different drain voltages. Secondly, an equation describing the drain current characteristics is fitted to measured data.

The goal of the pulsed measurement technique is to measure the MOSFET drain current characteristics under conditions similar to those found during RF operation. It is shown that the full thermal description of an RF power MOSFET is beyond the scope of an equivalent circuit model and that several approximations must be made. The method of thermal control which is proposed consists of applying fixed-length pulses to the gate. Each measurement begins with the device at a specific pre-calculated temperature. Due to the assumption of a constant thermal impedance, the measurement temperature may be in error by up to 7 °C, resulting in a current error of less than 1.5 %. However, if measurements are made without regard to the device temperature, errors of up to 40 % may occur, particularly at low current levels.

Discussion and conclusions

A method of measuring the MOSFET thermal impedance is developed, which consists of repetitively applying two consecutive pulses to the gate. The first pulse heats the device and the second is used to monitor the resulting temperature changes. The accuracy of this method is reliant on the use of several practical techniques, which are given. The resulting measurements are consistent with data sheet values of thermal impedance and the thermal conductivity of silicon.

In the model extraction process, all the S parameters are considered simultaneously, using relative vector errors in a single least p_{th} objective function. The optimisation begins with a random search, to locate a solution near to the global minimum, followed by a gradient optimisation to obtain the final solution. These techniques result in a unique model with physically consistent package element values. For a particular example involving eight frequencies and eight bias points, an average relative vector error of 2.14 % is achieved, with a worst error of 8.27 %. This suggests that the proposed MOSFET model, although relatively simple, represents the device adequately.

The equation which describes the model's nonlinear voltage-controlled current source must be considered as a curve fitting problem. A suitable equation is developed and fitted to measured data, using a least p_{th} objective function to give an acceptable balance between large errors and the average fit. Relative errors, weighted to favour high current regions, are used. For a set of data with drain currents up to 2.4 A and voltages up to 45 V, an average error of 3.2 % is obtained, with only 6 out of 347 points having errors greater than 15 %. These large errors lie within relatively unimportant regions of the drain current characteristics.

In order to verify the accuracy of the proposed modelling procedure, a model is extracted for an MRF136 MOSFET and used to predict the response of the physical device in a well characterised test fixture. Parameters such as output power, DC drain supply current, output harmonics and input impedance are compared for a variety of frequencies and drive levels. The average error for all results is 10 %, with a few errors greater than 25 %. These errors are attributed largely to the MOSFET model. However, it should be noted that the high power measurements

were made over a wide range of device temperatures and that the drain current data did not include points having simultaneously high voltages and currents. A number of improvements can be made, without fundamental changes to the described modelling procedure. These include the use of a slightly more detailed MOSFET model and refinement of the drain current equation. Also, the careful selection of S parameter and drain current measurements will be of some benefit.

The approach taken with passive component models is to use simple topologies which include only the most important effects. Model parameters for resistors, inductors and capacitors are identified by a least squares fitting to impedance data measured over a wide range of frequencies. Although ferrite-cored transformers are nonlinear, this effect is small and, in most cases, a linear model is adequate. A linear autotransformer model, with five parameters, is described. These parameters are identified by fitting the model to two multi-frequency impedance measurements. A similar procedure cannot be applied to transmission-line transformers, where some parameters must be determined by direct calculation from impedance measurements. Commonly used RF analysis packages do not accommodate a full description of nonlinear transformers in terms of magnetic quantities. However, magnetic saturation can be included in a model by means of a nonlinear capacitor. In the modelling of matching networks, relatively small component model errors can have a large overall effect. This is particularly true for capacitors if series inductance forms a significant part of their impedance.

Empirical design methods have a number of disadvantages. Calculated values of drain load impedance and large-signal impedance data provide a starting point, but are of limited value for wideband amplifiers. However, a valuable development tool is the measurement of impedances at high power levels, using a network analyser, external linear amplifier and directional coupler. Computer-aided design techniques have not been used widely with RF power amplifiers, largely due to the slowness of time-domain analysis methods. The harmonic balance technique is dramatically faster and is well suited to the needs of computer-aided design. A minor restriction of harmonic balance is that circuit transients cannot be analysed. Commonly available nonlinear analysis packages allow nonlinear elements, such as capacitors and current

sources, to be defined by the user. Amplifier characteristics, such as DC supply current and input impedance, are easily calculated using these programs, particularly with harmonic balance. Two aspects which are poorly handled by typical software are stability analysis and the optimisation of nonlinear circuits. Solutions to both problems, are, however, described in the literature.

A 15 W amplifier, operating from 118 MHz to 175 MHz, is designed empirically and then analysed using time-domain and harmonic balance programs. The predictions of amplifier output power and DC drain supply current are generally within 10 % of the measured values. However, the input impedance calculations are in error by an average of 31 %, with a maximum of 40 %. These errors can be attributed equally to the MOSFET and matching network models. In this case, due to a limited data set, the particular MOSFET model used in the analysis represents high current regions poorly. Also, it should be noted that the model was extracted for a different device, of the same type, to that used in the physical amplifier.

An amplifier, using an MRF136 MOSFET, is designed using linear and nonlinear analysis programs. The design process involves the selection of matching networks, as well as computer-aided analysis and optimisation, both linear and nonlinear. The performance of the amplifier, as built directly from the computer-aided design, is good in the lower half of the frequency band, but has a large input reflection coefficient at higher frequencies. This is corrected quickly by changing a capacitor value and adjusting the input matching network inductors. The poor accuracy of predictions for this amplifier, compared to those of the previous analysis, is found to result from the use of estimated values of component parasitics. Also, in this case, only the inductor impedances are matched closely to the design values.

A modified design procedure, involving two additional steps, is therefore proposed. This is to accurately characterise the selected components and, using these models, re-optimise the design. The performance of the constructed amplifier would then be closer to that of the design, allowing better use of powerful computer-aided techniques, such as optimisation.

The value of applying computer-aided design techniques to RF power amplifiers can be judged in terms of different engineers' levels of expertise. For those with moderate or little experience, computer-aided design is undoubtedly of benefit, leading quickly to a near-optimal design, which requires little empirical adjustment. However, for highly skilled designers, the advantages are presently not as great. The computer-aided design of nonlinear RF circuits is hampered by the speed of optimisation, model accuracy and the poor stability analysis capabilities of CAD packages. This must be countered by greater reliance on physical measurements than would otherwise be necessary. It can be anticipated that these problems will be addressed in the near future, as a result of rapidly growing computer power and advances in software. Computer-aided techniques are thus a valuable addition to the design tools available for RF power amplifiers and will become increasingly useful.

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